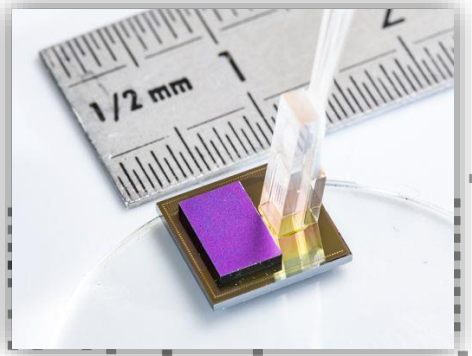
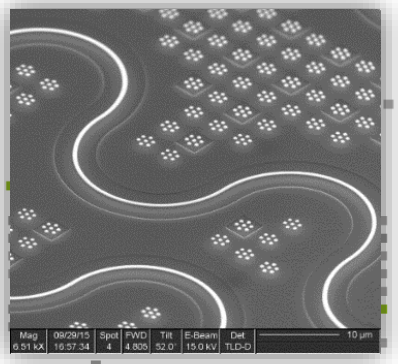


Electronic-Photonic switch matrix



Photonic Integrated Circuit (PIC)

Submicron Silicon core waveguide

LETI MPW OFFER AND CONCLUSION

Leti Innovation Days 2018 workshop

Christophe KOPP | 02/07/2018

SILICON PHOTONICS : TECHNOLOGY OVERVIEW

Silicon Implantation
- Modulator junction formation & activation

Silicon Patterning
- Define all the photonic devices
- Several silicon thicknesses and waveguide architectures

Germanium Epitaxy
- Photodetector patterning
- Germanium selective epitaxy

Germanium Implantation
- Photodetector contact formation

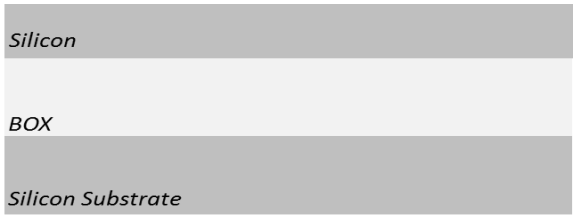
CMOS-based process with photonic dedicated optimizations

Silicidation
- Si Modulator contact silicidation

CMOS standard process

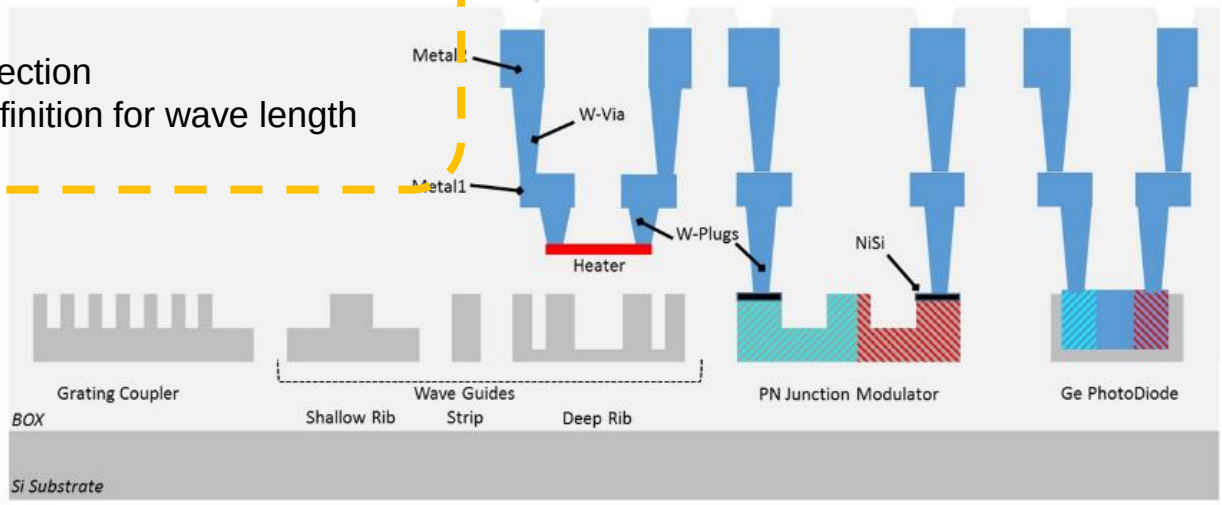
BEOL
- Metal interconnection
- Metal heater definition for wave length tuning

Silicon Photonic Process Flow



Silicon On Insulator (SOI) substrate : ∅8" or ∅12"

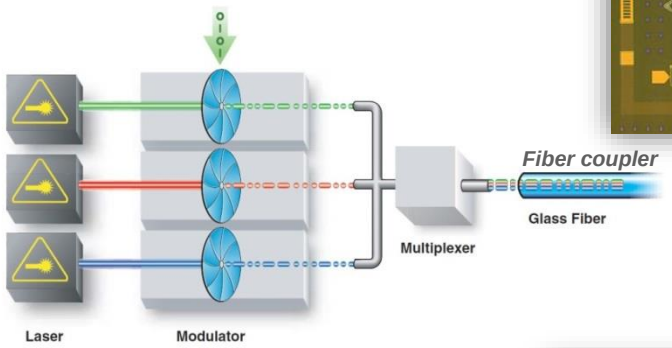
Cleanroom facilities (Leti)

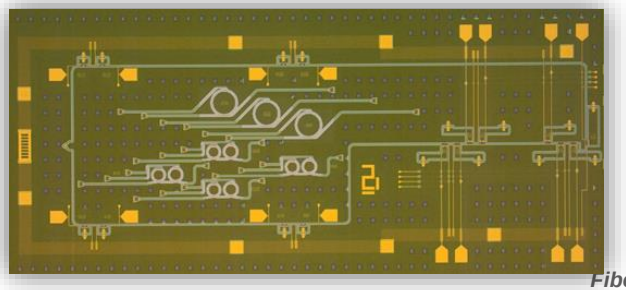


Schematic cross section of a silicon photonic circuit (Leti)

SILICON PHOTONICS : TYPICAL DEVICES

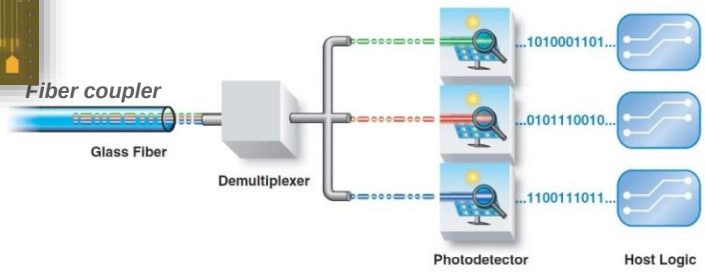
Emitter

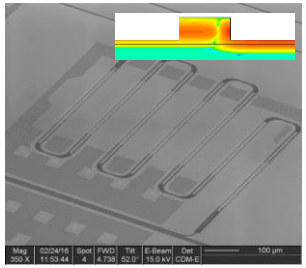




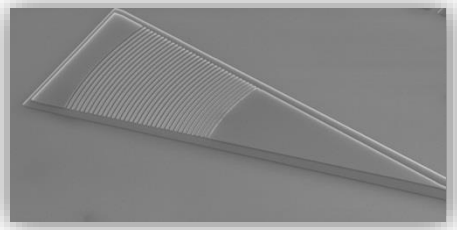
Optical transceiver circuit

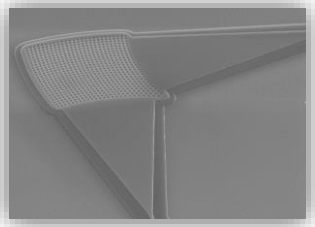
Receiver



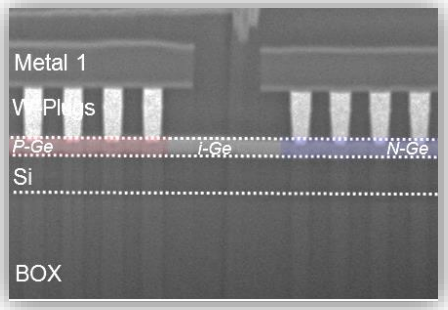


High speed modulator

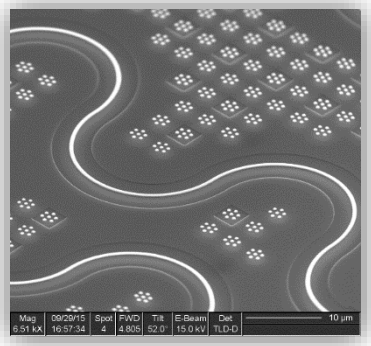


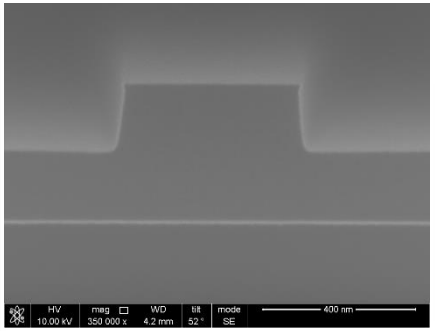


Fibre coupler

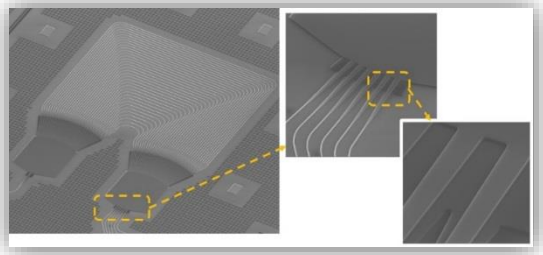


High speed photodetector

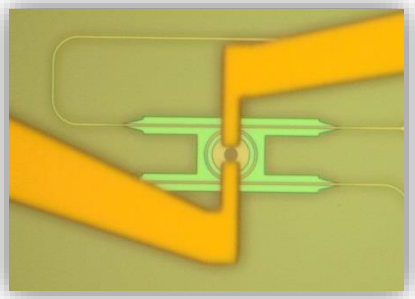




Highly confined waveguides



Wavelength multiplexer



Tunable filter

SILICON PHOTONICS : FOUNDRIES

R&D foundries

- AIM Photonics (US)
- IHP (Germany)
- IME (Singapore)
  - 220nm SOI platform
- IMEC (Belgium)
  - 220nm SOI platform
- LETI (France)
  - 300nm SOI platform
- PETRA (Japan)
- VTT (Finland)
  - 3µm and 12 µm SOI platform

Industrial foundries

- Global Foundries (US)
- INTEL (US)
- Luxtera (Freescale, US)
- Samsung (Korea)
- ST-Microelectronics (France)

R&D MPW offers

- CMC (Canada)
- CMP (France)
- Europractice/Epixfab (EU)
- MOSIS (US)

A. E. J. Lim et al., “Review of Silicon Photonics Foundry Efforts,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 20, no. 4, pp. 405–416, Jul. 2014.

IMEC MPW OFFER

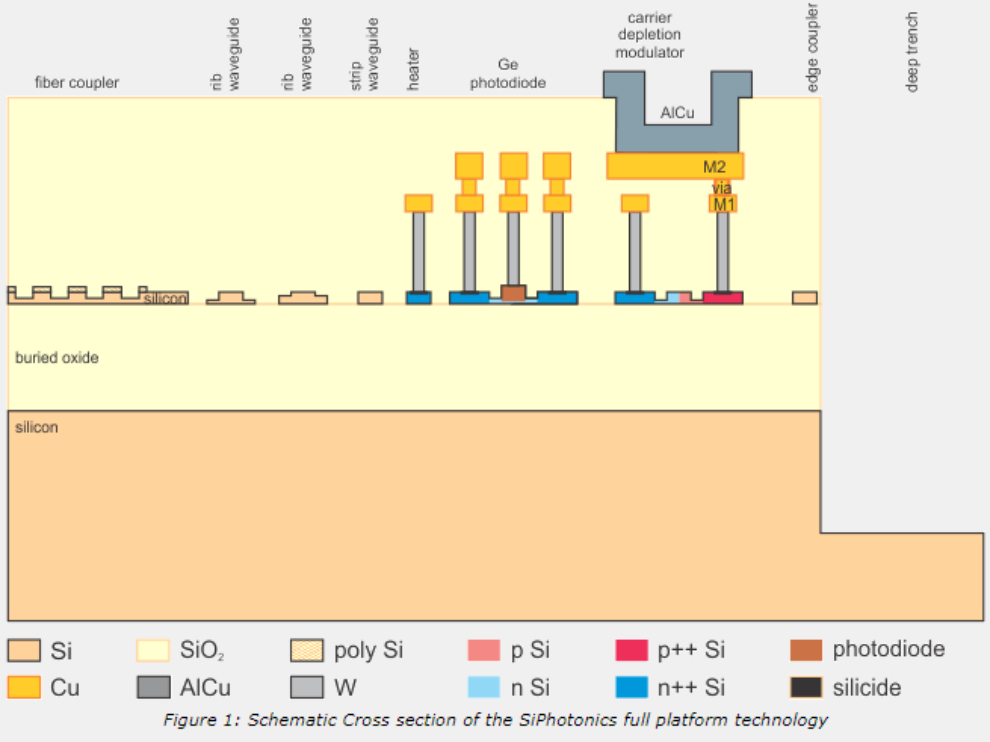


Figure 1: Schematic Cross section of the SiPhotonics full platform technology

imec-ePIXfab SiPhotonics: iSiPP50G

Module	Specification
Substrate	220nm SOI
SOI patterning	3 etch depth levels Minimum line and space: 150nm
Poly-Si	Deposition and patterning
Doping	4-level N and P
Germanium	Photodiodes, electro-absorption modulators
Contacts	W contact plugs on silicide
M1, VIA and M2	Standard CMOS metallization
Bondpads	Standard AlCu bondpads
BEOL openings	Edge couplers

- **SOI 220nm/2µm (BOX)**

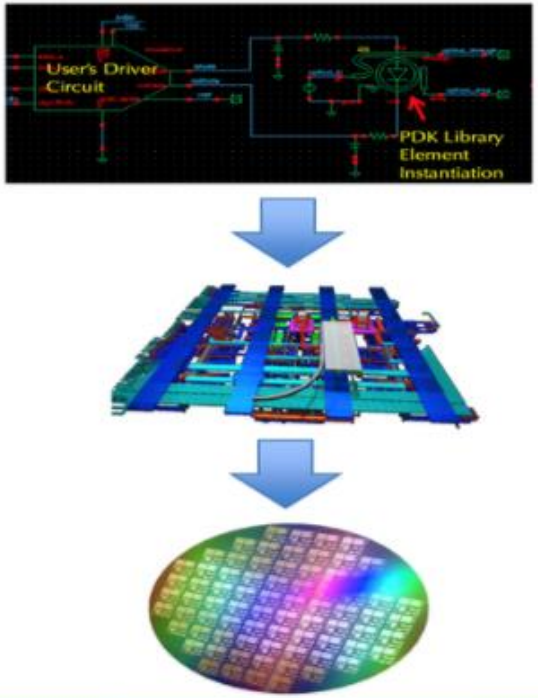
- Substrate: SOI with 220nm Si, 2um buried oxide
- **WG module** (WaveGuide): 220nm full Si etch for strip waveguides, photonic crystals, etc.
- **FC module** (FiberCoupler): 70nm partial Si etch for fiber couplers, rib waveguides, etc.
- **SK module** (Socket): 150nm partial Si etch
- **Poly-Si module**: extra etch-level for efficient fiber couplers
- 4 P and N-type doping levels for **electro-optic modulator** design and heaters for thermo-optic modulation
- **Ge photodiodes** as detectors
- High speed **Ge electro-absorption** modulators
- 2 levels of metal **interconnect**
- **Edge coupler**

AIM MPW OFFER

Silicon Photonics Multi Project Wafer (MPW

- **MPW Fab Runs Planned in 2017**
  - **SUNY Poly 300mm fab line**
  - **3 MPW offerings**
    - Full-Active- 2 planned in 2017
    - Passive Only- 2 planned in 2017
    - Interposer- 1 planned in 2017
  - **Reservations to be a rider can be started at** http://www.aimphotonics.com/pdk-mpw-sign-up/
    - Generates quote with terms
    - 20% down to hold slot; balance invoiced at design submission
- **MOSIS is the MPW Aggregator**
  - DRC clean designs are submitted to MOSIS
  - MOSIS also distributes the PDK
- **MPW Pricing**

FULL	PASSIVE	INTERPOSER
50mm² chips	50mm2 chips	156mm2
$100K AIM members	$30K AIM members	$93.6K AIM members
$120K non-members	$36K non-members	$112.3K non-members
8mm² chips		
$25K AIM members		
$30K non-members		



- **SOI 220nm/2µm (BOX)**

IME MPW OFFER

Institute of Microelectronics
A*STAR

SILICON PHOTONICS MULTIPLE-PROJECTS WAFER

Types of Service:

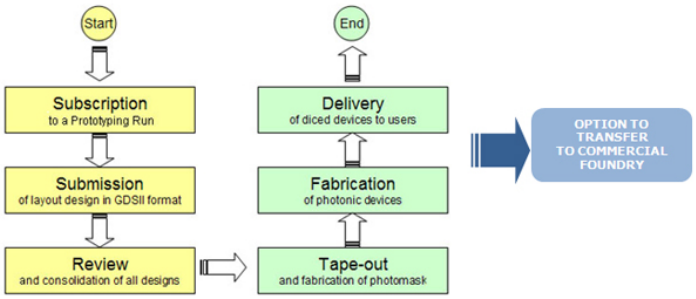
- Shared Prototyping Runs: Participants will share the cost of the prototyping efforts and have the option of using either IME's or their own design, on the proviso that it is within technical specifications.

  Schedule: **January**, **May** and **September** each year.

  To participate in the next shared prototyping run, please contact us for details.

- Customised Prototyping Runs: This service is intended for user whose requirements are beyond the timeline and technical specifications of the Shared Prototyping Runs. For Customised Prototyping, please contact us for more information and to arrange a discussion.

Flow:



MULTIPLE-PROJECTS WAFER (MPW) SERVICES

IME Multiple-Projects Wafer (MPW) is a one-stop solution for low cost prototying and low volume production. Designs from multiple customers are combinedinto one mask set and wafer lot. This allows costs to be shared across a number of program participants and provides a cost-effective method for prototype and proof-of-concept silicon.

Contact person:
Dr. Patrick Lo Guo Qiang
Institute of Microelectronics, Singapore
logq@ime.a-star.edu.sg
Phone: +65-67705705

- **SOI 220nm/2µm (BOX)**

LETI MPW OFFER

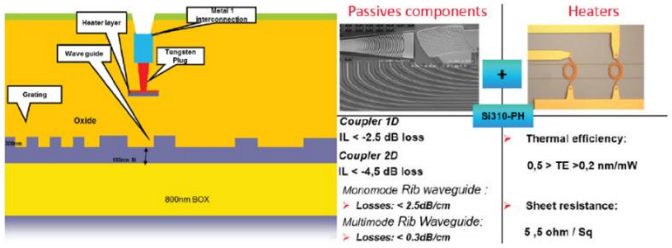
1 Si310-PH: Passif and heaters: friendly packageable

EUROPRACTICE

www.europractice-ic.com / SiPhotonics_technology_LETI_passives_w_heater.php

Key features

- Passive structures (3 mask layers DUV 193nm)
  - CD min 120nm
  - 300nm /150nm -> see cross section 1
  - 150nm /0 -> see cross section 1
- Optional Slab 65nm (Deep Rib)
- Ti/ TiN Heater layer
- W vias
- 1 Metallization for routing
- Final passivation with pad opening



Si310-PH technology

- **SOI 300nm/800nm (BOX)**

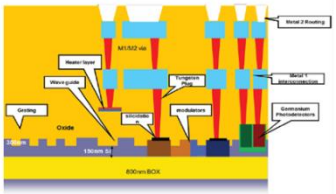
- High performance building blocks
- Compatible with 3D integration
- PDKs available via Cadence, Phoenix software, Mentor Graphics, and Pyxis
- Technology compatible design rules with 300 mm industrial foundry

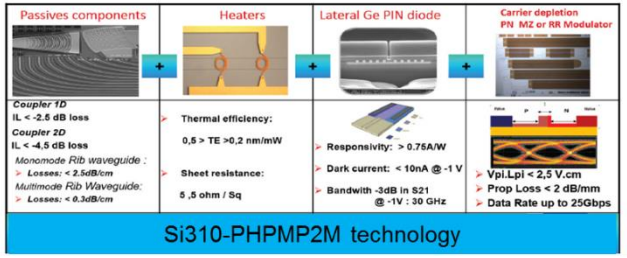
2 Si310-PHMP2M: Full platform: friendly packageable

http://cmp.imag.fr/

Key features

- Passive structures (3 mask layers DUV 193nm)
  - CD min 120nm
  - 300nm /150nm -> see cross section 1
  - 150nm /0 -> see cross section 1
  - Optional Slab 65nm (Deep Rib)
- Ti/ TiN Heater layer
- Germanium PD's fabrication
  - n and p implant level
- MZ and RR Modulators
  - 4 level implants
- Silicidation
- W vias
- 2 Metallization BEOL for routing
- Final passivation with pad opening
- Friendly Packageable
- **Compatible for UBM fabrication for electronic integration**





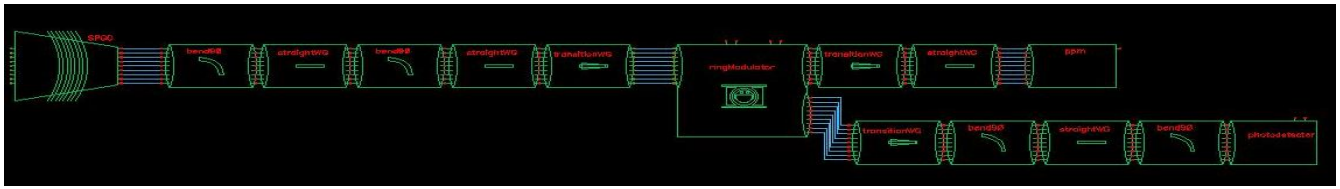
Si310-PHPMP2M technology

CIRCUIT DESIGN KIT AT LETI

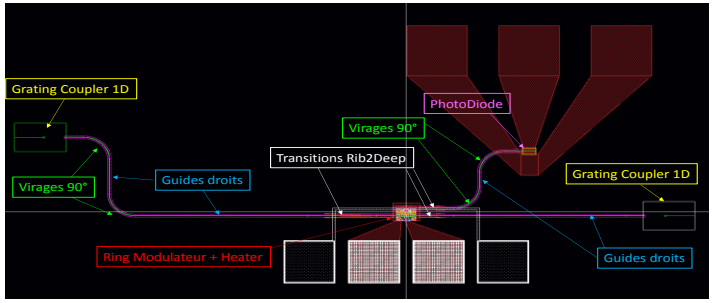
Library of available components

- Cadence/Virtuoso and Mentor/Calibre + Eldo framework
- Phoenix software
- Pyxis/LUMERICAL

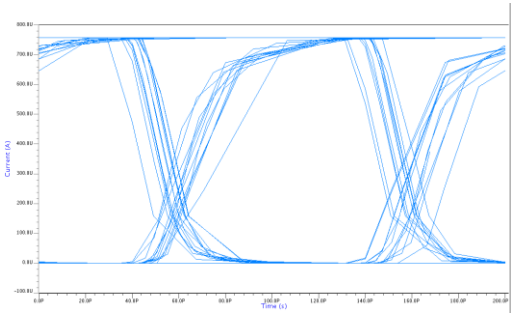
PDK Photonics Models, Schematic circuit simulation, Layout, Verification, Layout finishing



Schematic view



Layout view



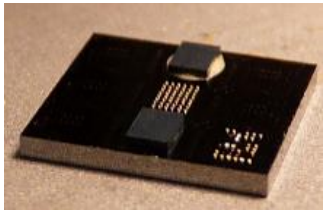
Circuit simulation

"Multiple wavelength silicon photonic 200mm R&D platform for 25Gb/s and above applications", Szelag et al., Photonics Europe 2016
"Verilog-A passive and active components modeling for silicon photonic circuits process design kit (PDK) assembly", Karakus et al., Photonics West 2016

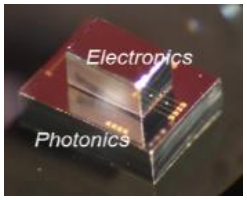
TOWARDS HIGHER INTEGRATION LEVEL

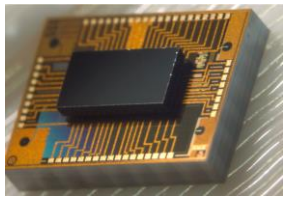
Increasing number of electrically driven photonic devices

Integration/Co-integration level



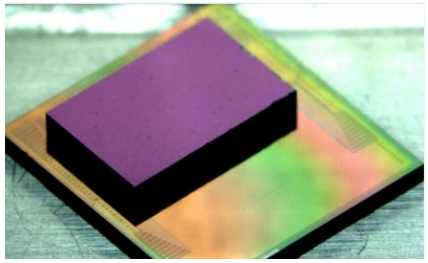
44 Bumps





100 Bumps 144 bumps

484 bumps



2091 bumps

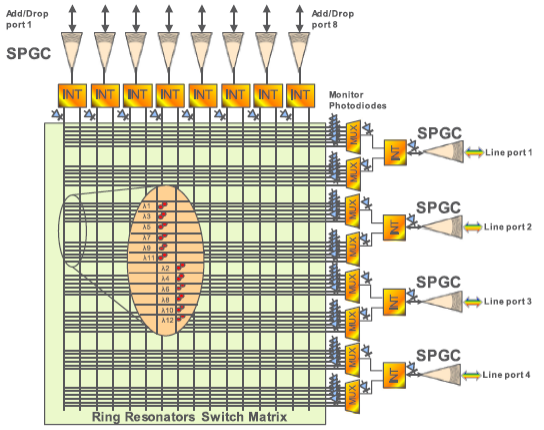


Fig. 2. Architecture of IRIS TPA.

2012	2013	2014	2015	2016	2017	2018

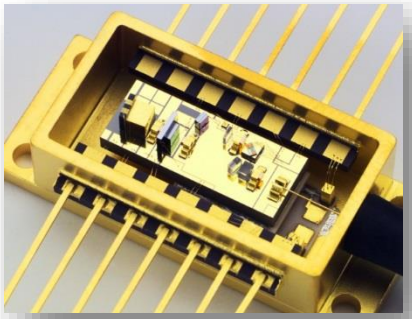
TOWARDS ON CHIP INTEGRATION

Discrete component assembly — 1990

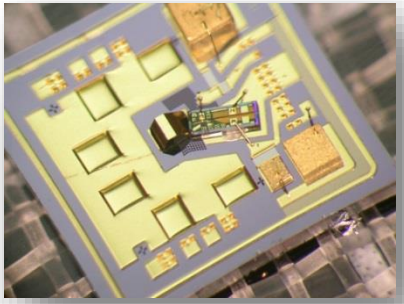
Micro-bench — 2000

Integration and 3D assembly with electronics — 2010

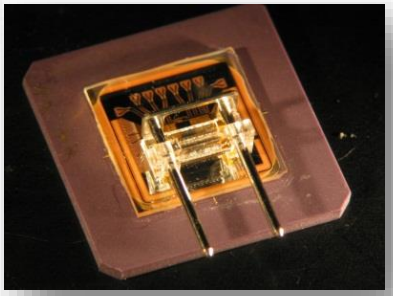
Switch & Network on chip — 2020



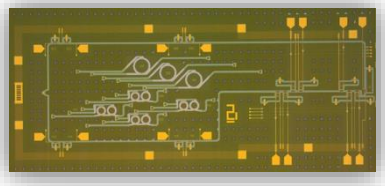
Axsun

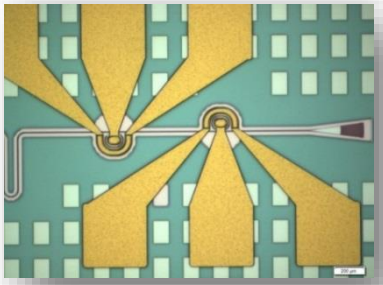


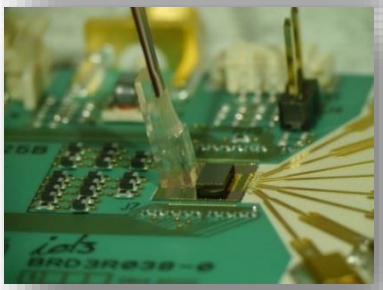
Hymite



Intexys / CEA

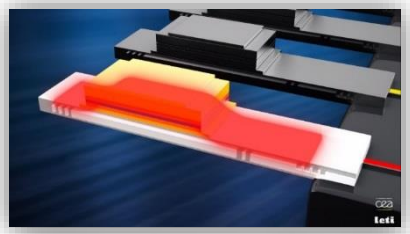




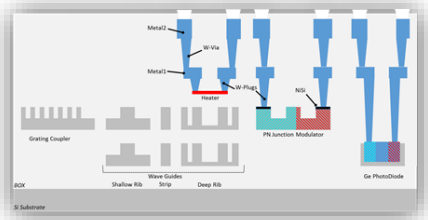


CEA

Network on chip



Heterogeneous integration



Multilayer photonics

C. Kopp et al., “Silicon photonic circuits: on CMOS integration, fiber optical coupling and packaging”, IEEE JSTQE (invited paper), Vol. 17, n°3, pp. 498-509 (2011)
S. Bernabe et al. “A Fully packaged 25 Gbps/channel WDM photoreceiver module based on a Silicon Photonic Integrated Circuit and a flip-chipped CMOS quad Transimpedance Amplifier”, OIC 2016

Leti Innovation Days
July 4-5, 2018

Thank you for your attention

Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
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