III-V/SI LASER INTEGRATION: CHALLENGES AND RESULTS

B. Szelag CEA-Leti

OUTLINE

- CEA-LETI’s Silicon Photonic Overview
- III-V device on Si Photonic – Why & How
- III-V/Si laser integration – Leti’s first results
- Toward CMOS compatible III-V/Si laser integration

LETI, TECHNOLOGY RESEARCH INSTITUTE

Founded in 1967, based in France (Grenoble) / offices in USA and Japan

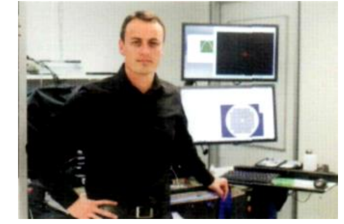
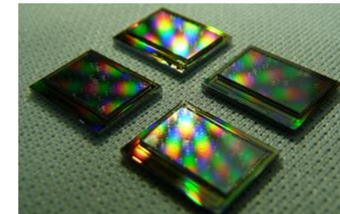
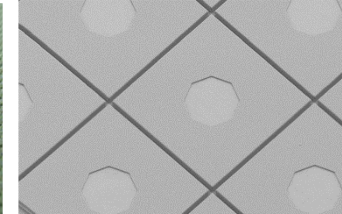
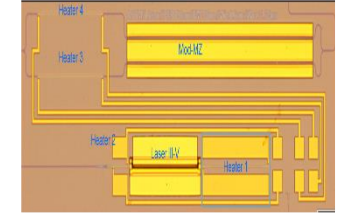
1900
People

60
Startups created

2670
Patents in portfolio

€315
Million budget

Optics and Photonics Division

Created in 1978
300 researchers, engineers and PhD students

500 patents in portfolio
91 new patents in 2017

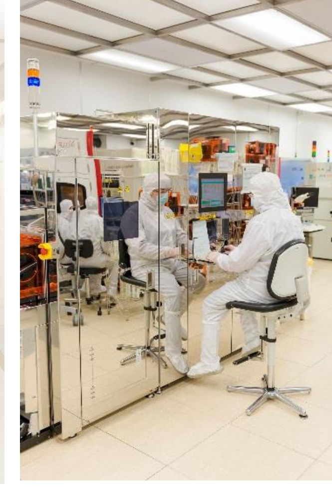
60 M€ budget
90% from external revenue

OUR RESEARCH FACILITIES

NEW in 2017 : PHOTONICS BUILDING

- 12600 square meters incl. offices, labs and clean rooms
- Dedicated clean rooms for III-V and II-VI materials (growth, epitaxy, process and packaging) on versatile substrate geometries up to 150 mm
- Electro-optical test and characterization facilities
- Design and simulation capabilities (process, growth, optics…)

8500m² CLEAN ROOMS for 200mm & 300mm wafers



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OUR BUSINESS MODEL

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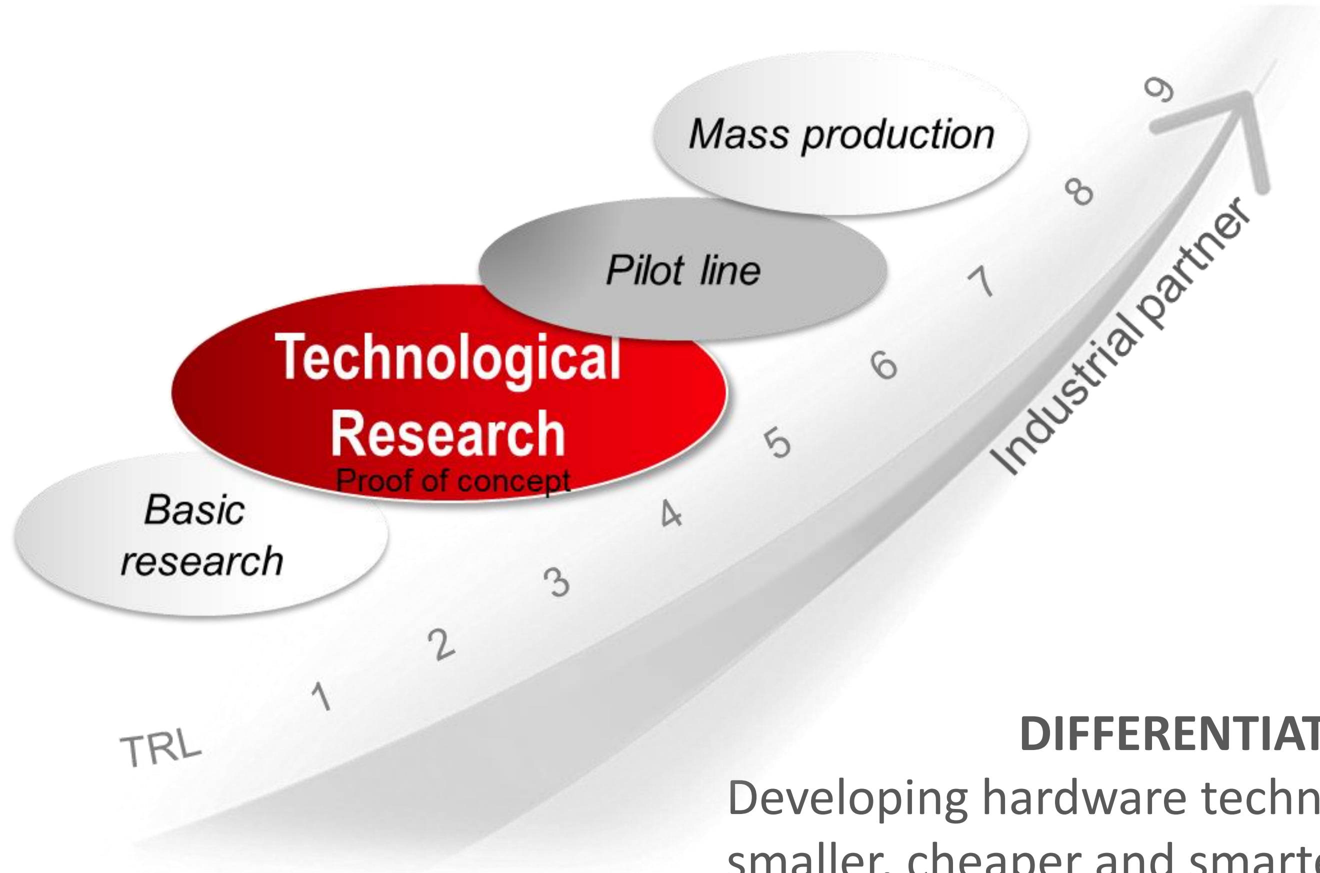
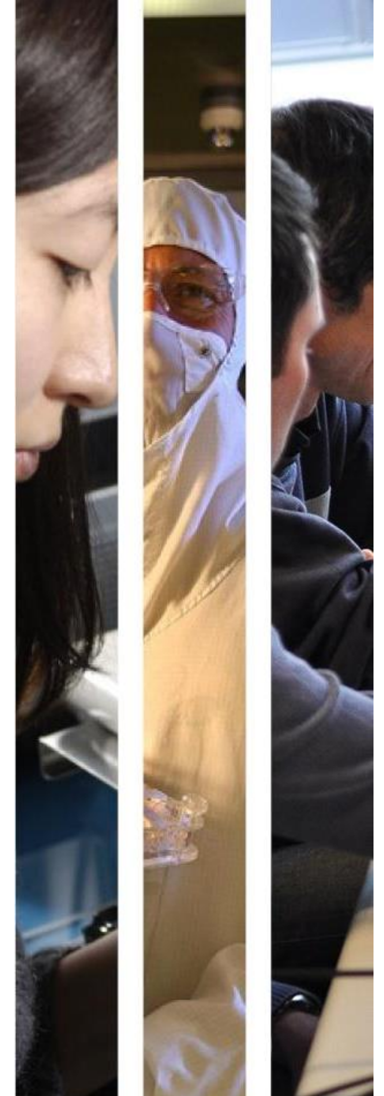
One-to-One collaboration to create and transfer new technologies to our industrial partners



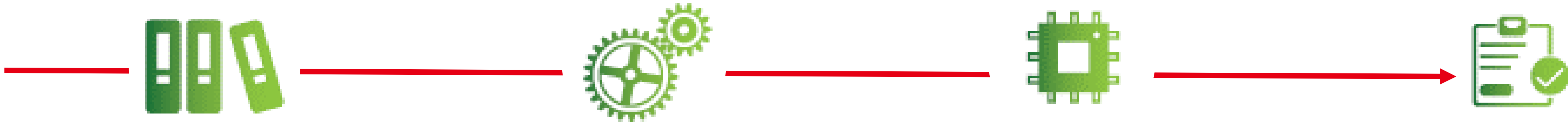


DIFFERENTIATION

Developing hardware technologies to obtain smaller, cheaper and smarter photonic products for our industrial partners.

SILICON PHOTONICS OFFER

A complete toolbox based on Telecoms/Datacoms, Microwave Photonics and Sensor



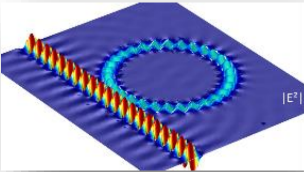
DEVICE LIBRARY

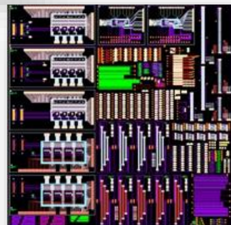
Passive devices O&C-band

- Waveguides
- Surface injection coupler 1D&2D
- WDM Mux/Dmux (100G-LR4)

Active devices O&Cband

- Modulators
- Ge on Si photo detectors
- Heterogeneous III-V on Si lasers

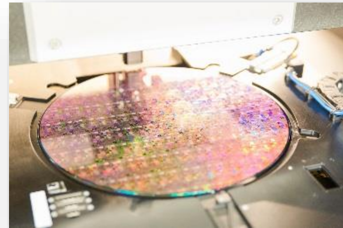




FABRICATION PLATFORM

200mm & 300mm wafers

- Amorphous Silicon, SiNx deposition
- Deep UV 193 nm litho
- Low sidewall roughness – Si and SiNx waveguides
- Ge epitaxial growth
- p-type and n-type ion implantation
- Direct bonding and processing of III-V materials on Si

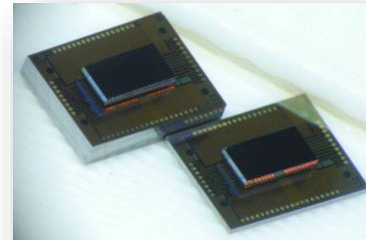


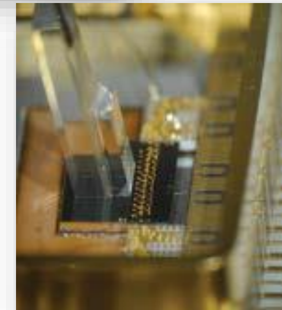
Multi Project Wafer for prototyping

CIRCUITS & MODULES

Circuit design & Packaging tools

- Hybridation of photonic and electronic Ics
- Optical fiber attachment

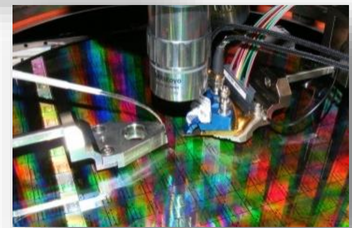




TESTING

Wafer level and module testing

- 4 fully-automated on-wafer probers
- Ambient temperature up to 90°C
- Bit Error Rate measurement NRZ/PAM4 up to 64 Gbaud
- Small signal analysis up to 67 GHz (O/E, E/O, E/E)



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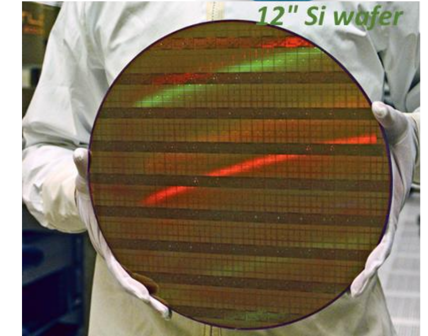
RECALL OF SILICON PHOTONIC BASIS

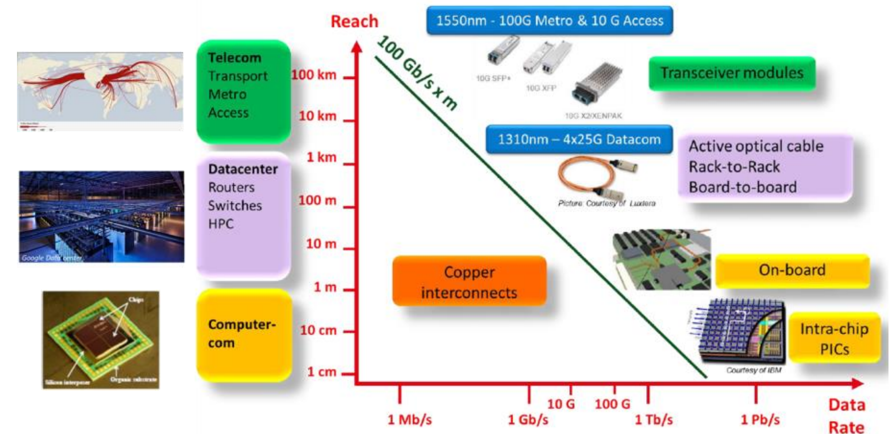
- Silicon photonic aims at integrating in the silicon microelectronic CMOS technology circuits and modules initially based on other technologies (InP, InGaAs, LNbO3, SiO2, …)

- Making photonic integrated circuits on Silicon using CMOS process technology in a CMOS fab.

- Merging photonics and CMOS.

- Expected benefits:
  - Higher integration level
  - Low cost, high volume facilities
  - Access to mature packaging and EDA tools
  - WDM and scaling to >1 Tb/s
  - Solving electrical interconnect limits in Data centers, Supercomputers and ICs with higher capacity, lower cost optical interconnects





SILICON PHOTONIC BUILDING BLOCKS

Silicon Photonic Links

Receiver

Photo-detector:
E to O conversion

De-Multiplexer:
Signal separation

Electrical
Data Out

Optical
Data In

Transmitter

Electrical
Data In

Fiber coupler:
PIC to fiber interface

Optical
Data Out

Modulator:
E to O conversion

Multiplexer:
Signal combining

Driver

Laser λ4
Laser λ3
Laser λ2
Laser λ1

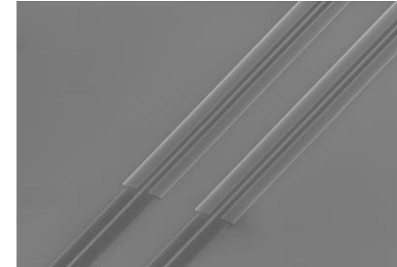
Modulator

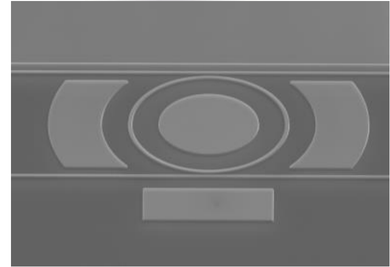
Multiplexer

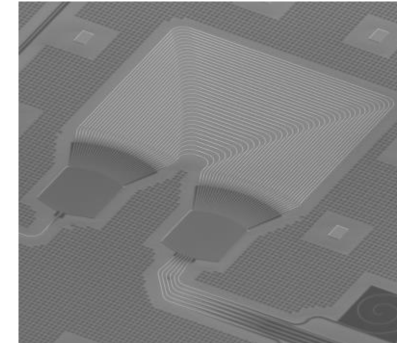
De-Multiplexer

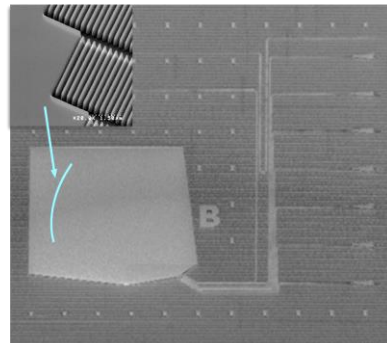
Detector

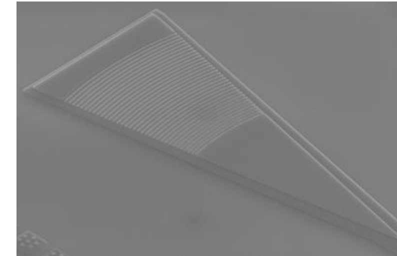
Fiber Coupler

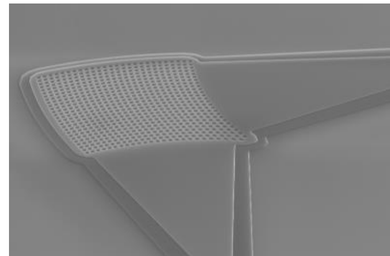


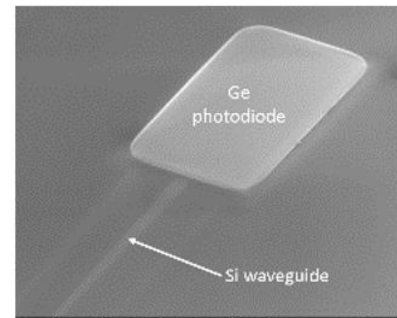






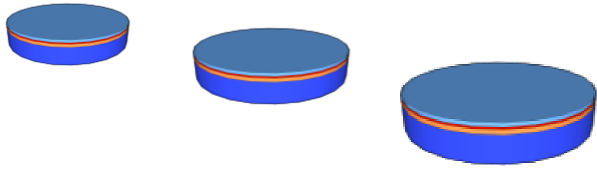






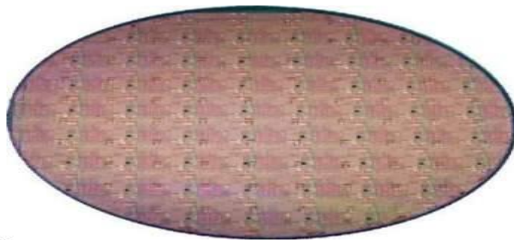
HETEROGENEOUS INTEGRATION FOR SI PHOTONIC

- Growth of the III-V wafers (2'', 3'', 4'')



- Processing of SOI wafers 8'' or 12''

(modulators, detectors, passive devices, etc.)



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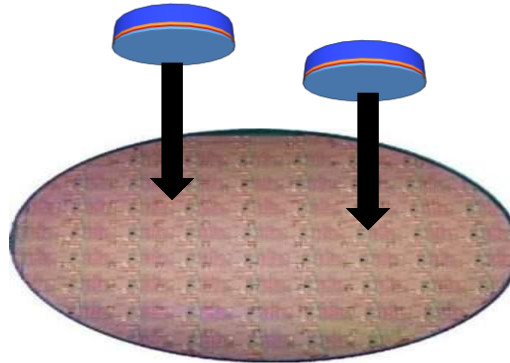
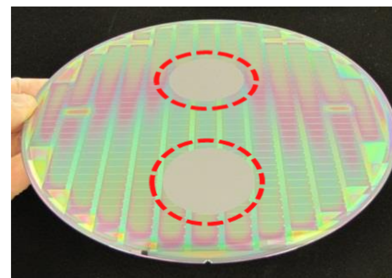
III-V bonding on processed SOI & InP substrate removal





- III-V material patterning,
- Metallization of lasers, modulators and detectors

CMOS fab compatible processes needed to avoid wafer downsizing and maximize the functional SOI wafer surface.

HETEROGENEOUS III-V INTEGRATION

Components

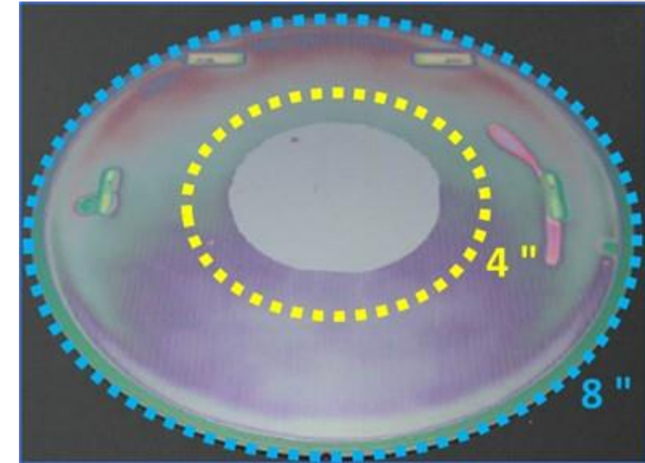
- Laser
- Electro-absorption modulator
- Semiconductor optical amplifier

To use the advantage of each material properties:

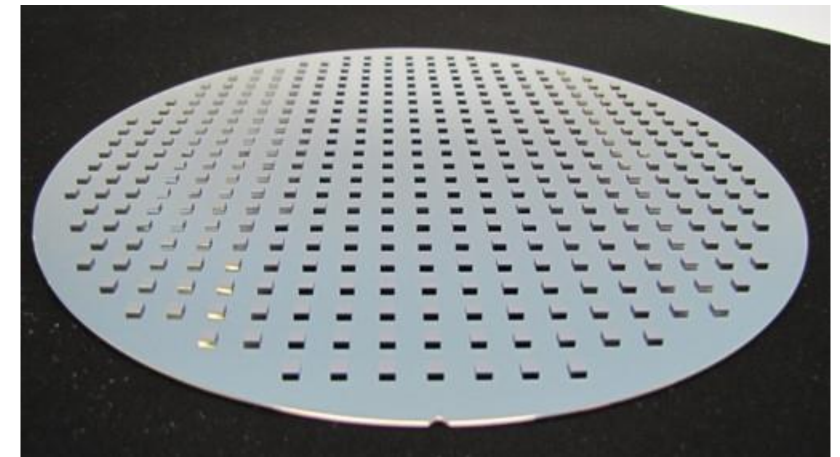
- Optical gain is provided by the III-V (InP/InGaAsP –QWs or AlGaInAs)
- The high resolution laser cavity as well as the PIC is fabricated in a 200/300mm Silicon platform (CMOS planar technology)

To localize III-V by die-to-wafer bonding

- Highly flexible approach (multiple laser-λ in the O+C+L bands / PD / EAM)
- Equivalent to multiple localized epitaxies



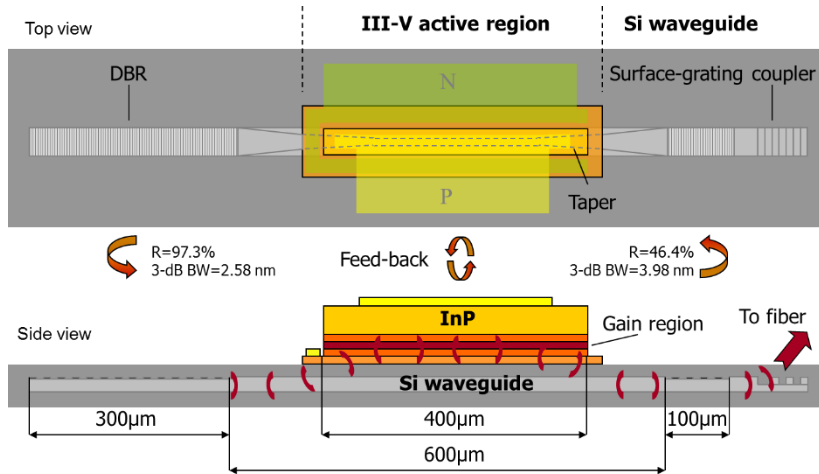
III-V wafer bonding

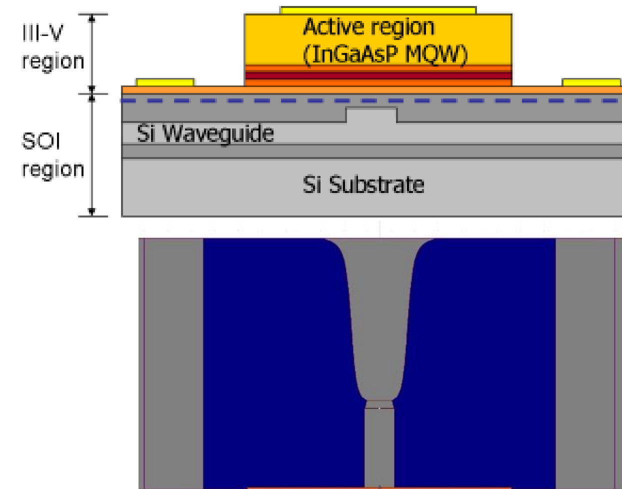


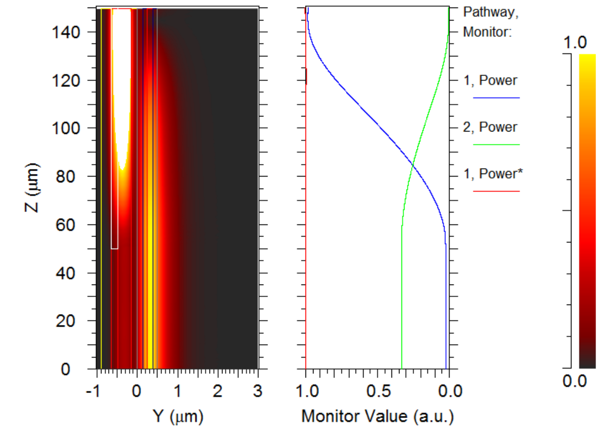
Die bonding

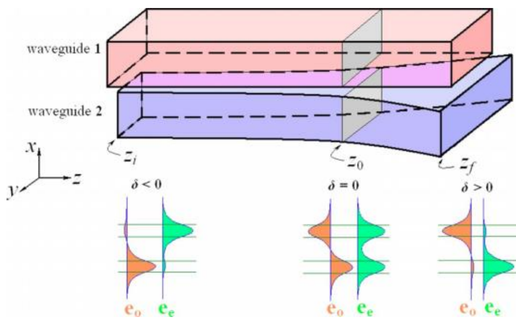
ADIABATIC COUPLING FOR HYBRID III-V/SI DEVICE

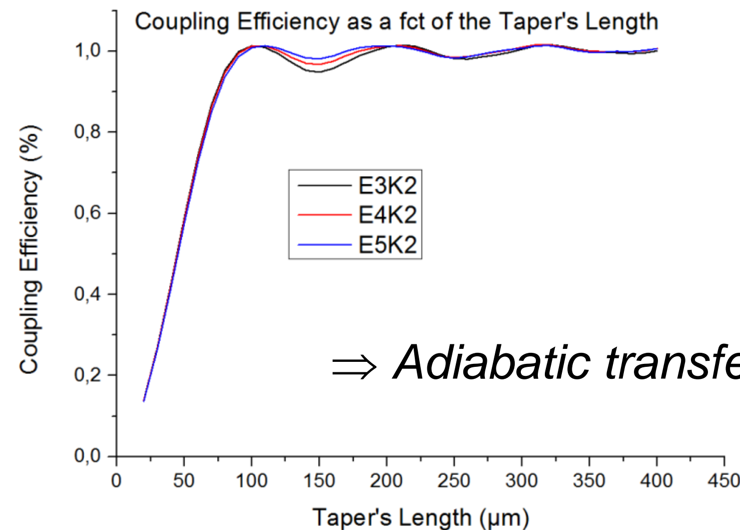
- **Hybrid III-V on silicon lasers design**
  - Adiabatic coupling [1]











$\Rightarrow$ *Adiabatic transfer reached after 100µm*

[1] X. Sun, H.-C. Liu, and A. Yariv, Opt. Lett., 34, 280-282 (2009).

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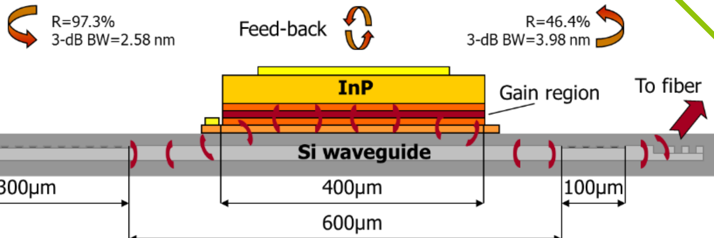
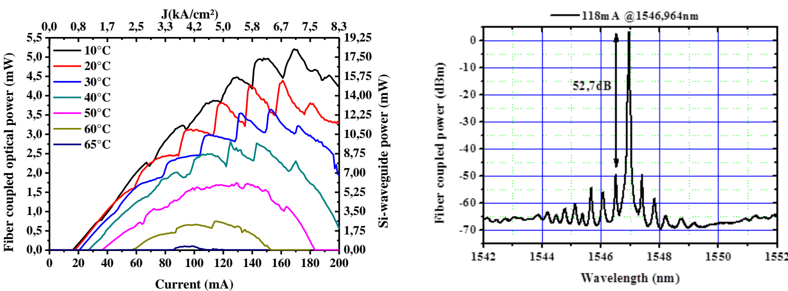
INTEGRATED HYBRID III-V/SI LASER PAST RESULTS

Hybrid DBR @ 1,55µm

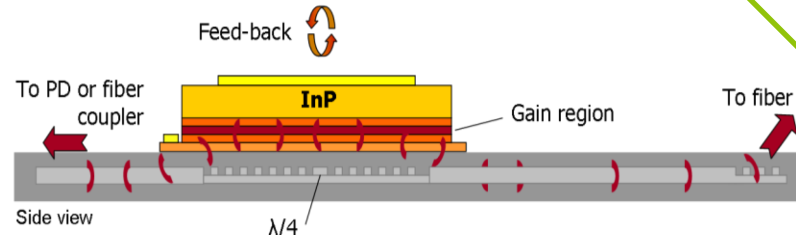


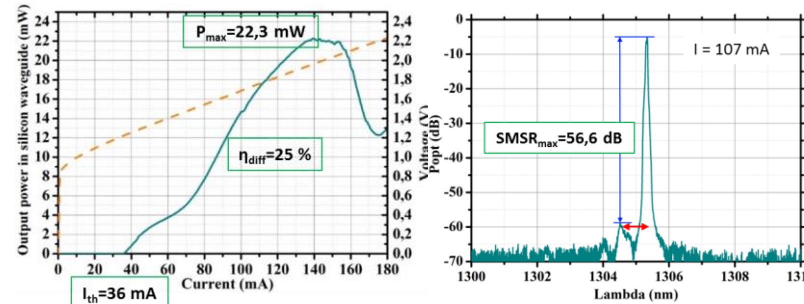


- CW operation (>60°C)
- I_{th}: 17-60mA (0.8-2.5 kA.cm^{-2})
  - for T: 10 to 60°C
- Rs= 7.5 Ω
- Lasing turn-on voltage : 1.0 V
- **P**$_{\text{-Si-waveguide}}$ > 14 mW (20°C)
- **P**$_{\text{-fiber}}$ > 4 mW (20°C)
- SMSR > 40 dB

A.Descos *et al.*, ECOC 2013

Hybrid DFB @ 1,31µm

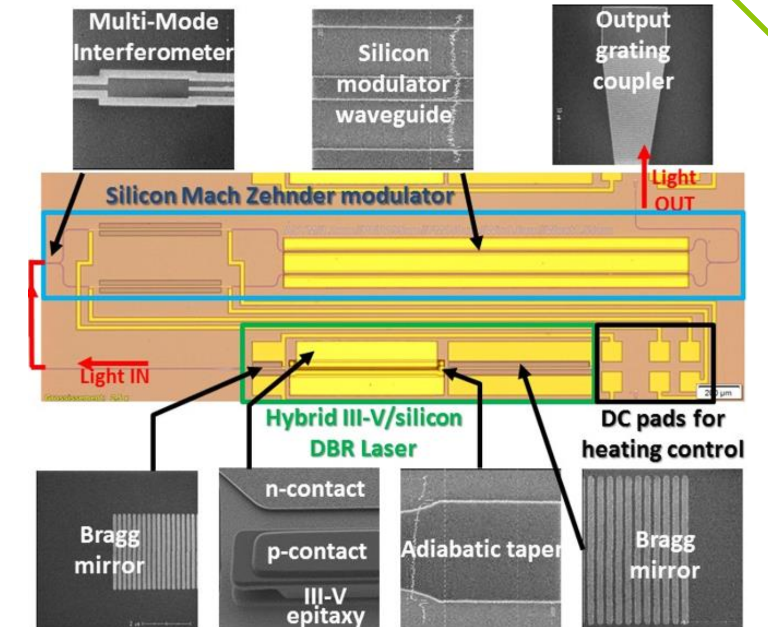


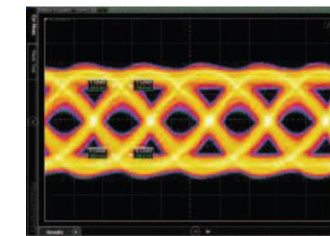


- CW operation (>55°C)
- Ith: 30-50mA
- Rs= 15 Ω
- Lasing turn-on voltage : 1.2 V
- P-Si-waveguide > 20 mW (20°C)
- P-fiber > 3 mW (20°C)
- SMSR > 40 dB

H. Duprez *et al.*, Opt. Express 23(7), 8489 (2015)

25Gb/s laser + MZM transmitter





- Co-integration hybrid IIIV/Silicon DBR laser + silicon Mach-Zehnder modulator.
- 25Gb/s transmission at 1.3µm up to 10km.

T. Ferrotti et al. , SSDM, (2016)

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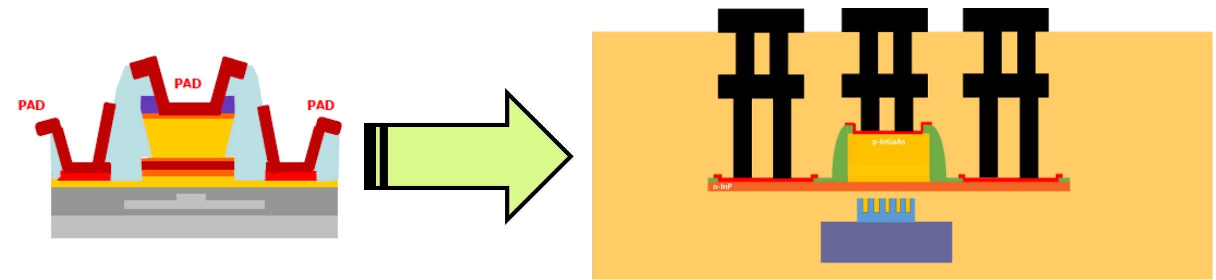
HYBRID INTEGRATED LASER: FROM III-V FAB TO CMOS FAB

1. Process & Materials
   - Patterning
   - Contact on III-V
   - Multi level BEOL
   - III-V Die Bonding



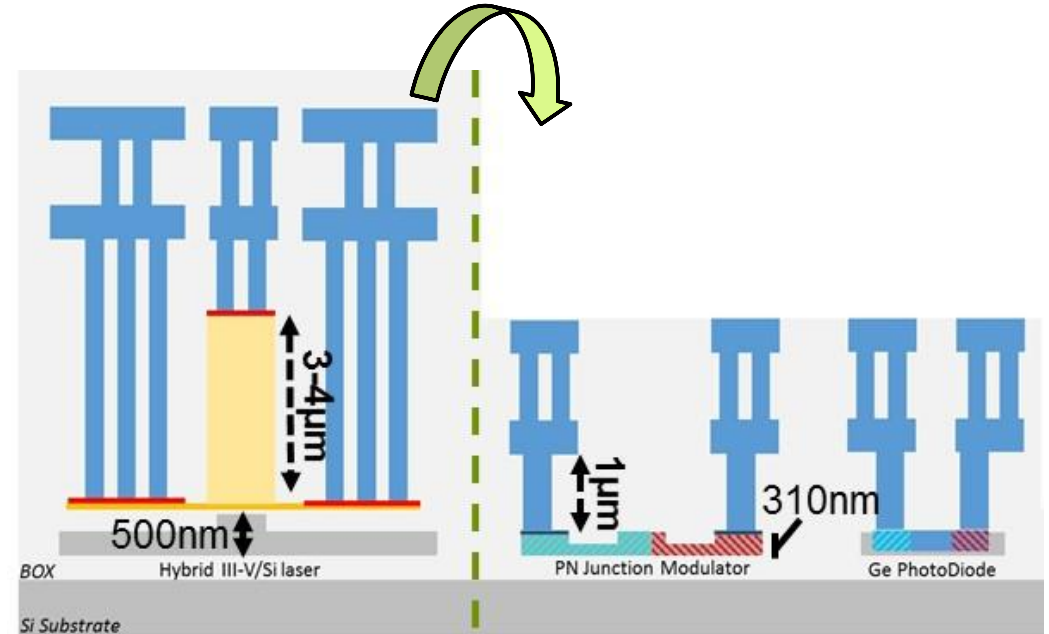
2. Laser Topography

   III-V stack thickness=4µm
   vs.
   PMD thickness=1µm

3. SOI Substrate

   SOI for laser: 500nm
   vs.
   SOI platform: 310nm

4. Laser integration impact on other devices



HYBRID INTEGRATED LASER: FROM III-V FAB TO CMOS FAB

1. Process & Materials

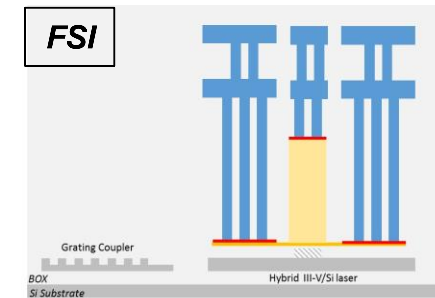
- Laser process steps cmos compatible process:
  - No noble metals
  - Conventional patterning steps (no lift-off)
- Planarized multi-metal level BEOL
- Collective die bonding

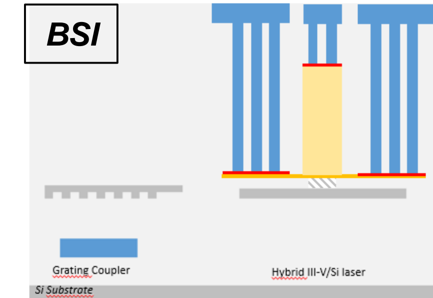
2. Laser Topography

- Thick PMD for laser front side integration (FSI)

Or

- Laser back side integration (BSI)

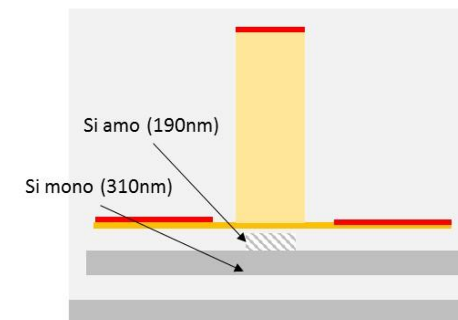




3. SOI Substrate

- Localized Si thickening on 310nm SOI:

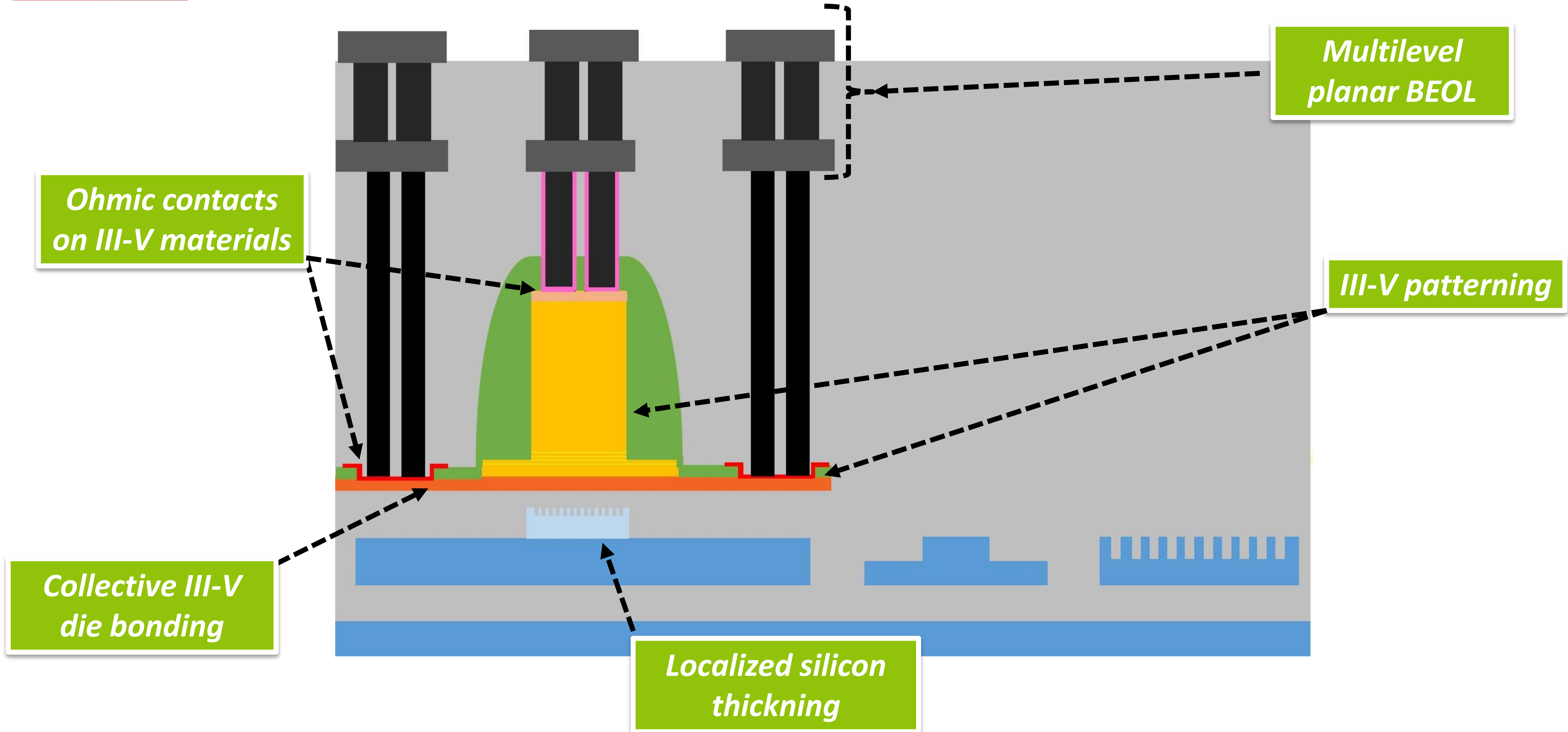
Damascene process with Si-Amo (FSI or BSI) or selective Si-epi (FSI only)



4. Laser integration impact on other devices

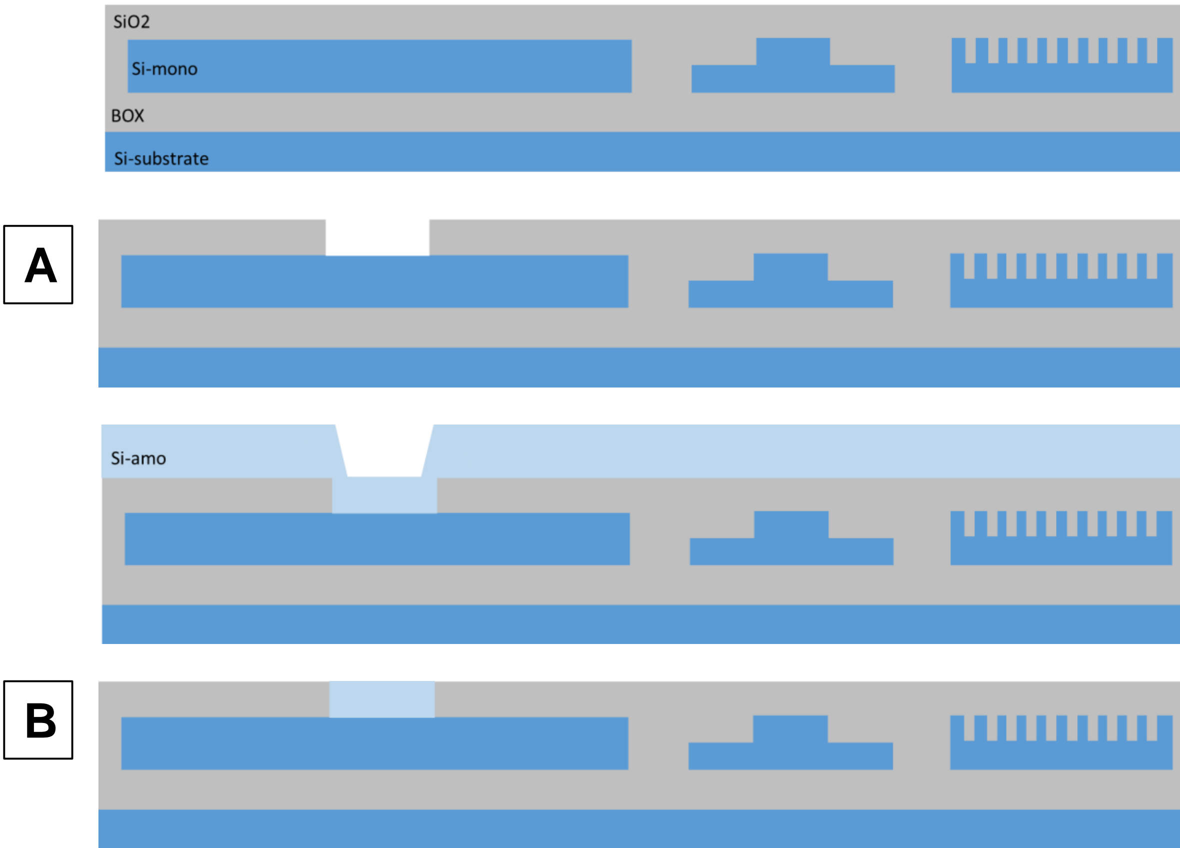
- Additional thermal budget due to laser integration < 600°C

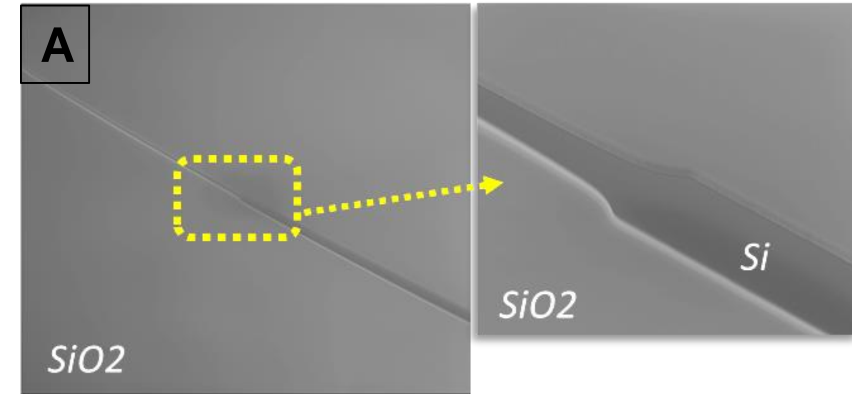
LARGE SCALE INTEGRATION CMOS FRIENDLY PROCESS

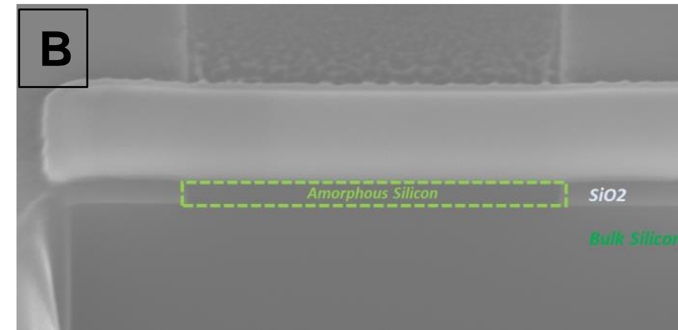


B. Szelag *et al.*, IEDM 2017

LOCALIZED SILICON THICKENING MODULE



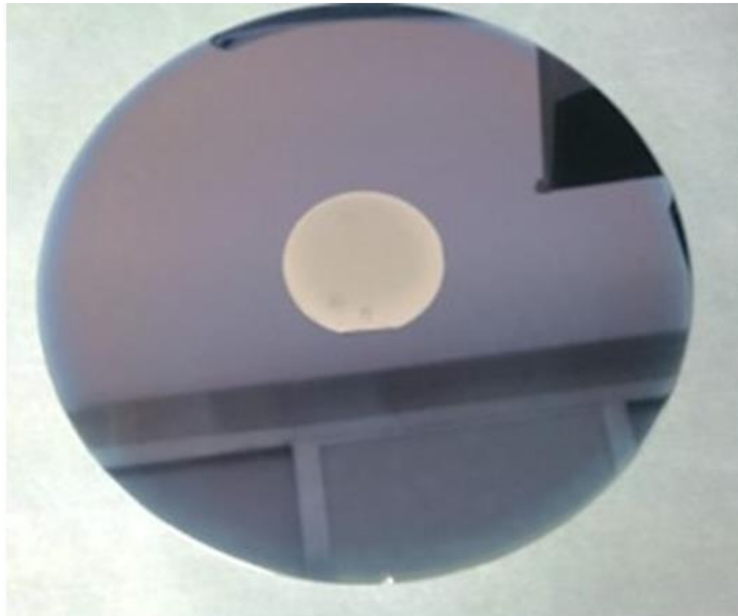




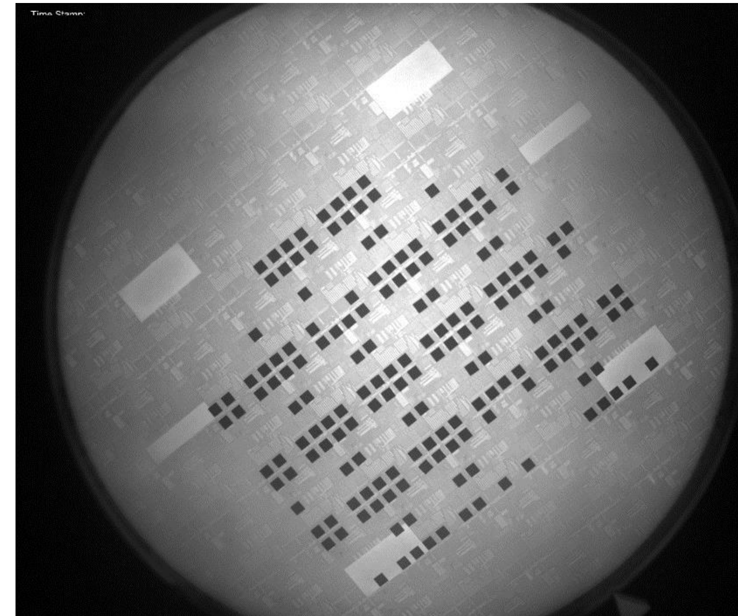
Localized silicon thickening – no changes in the photonic core process

III-V WAFER/DIE BONDING ON SILICON

- III-V wafer/die bonding
- InP Substrate removal

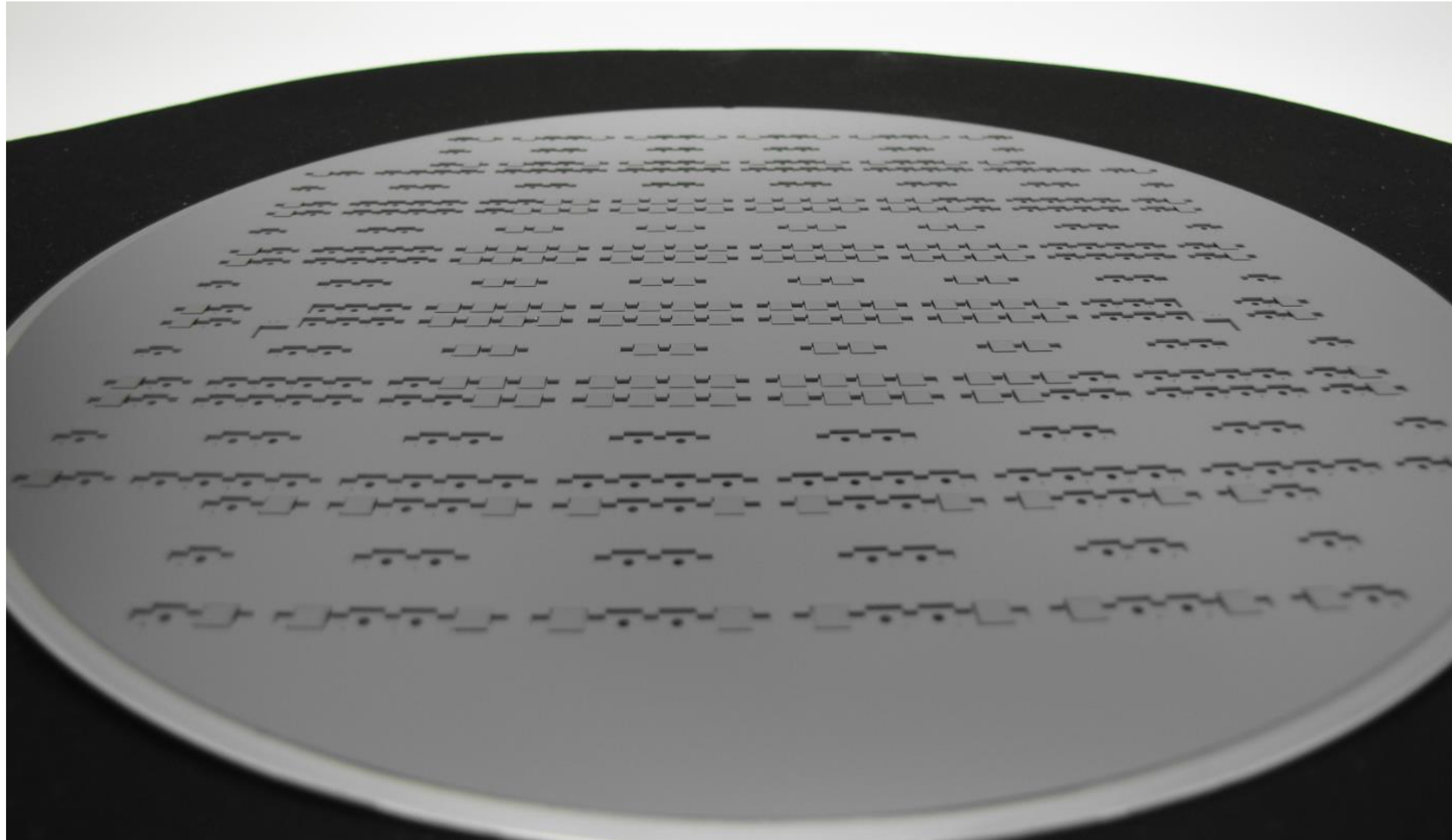


2" III-V wafer bonding on SOI



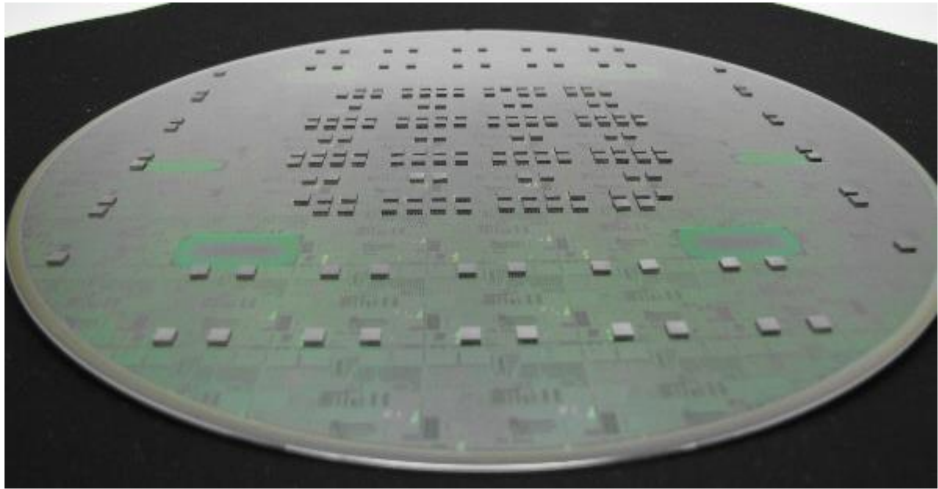
Localized III-V die bonding on SOI

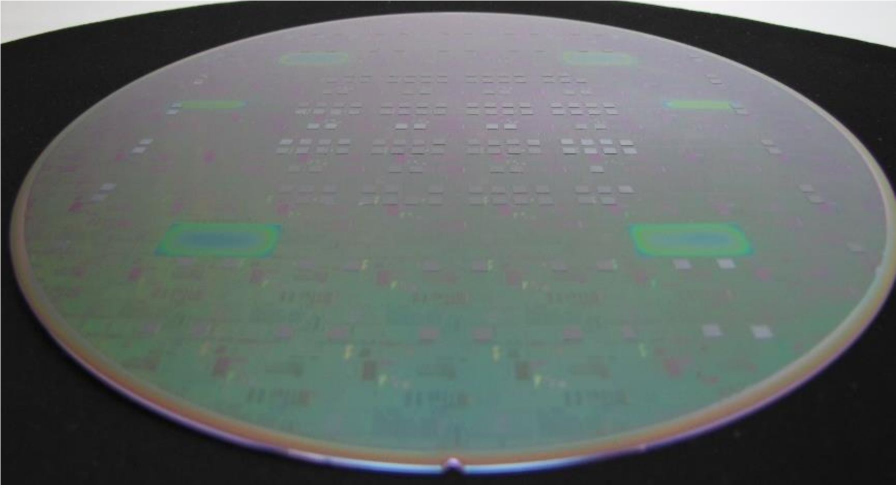
COLLECTIVE DIE BONDING WITH SILICON HOLDERS

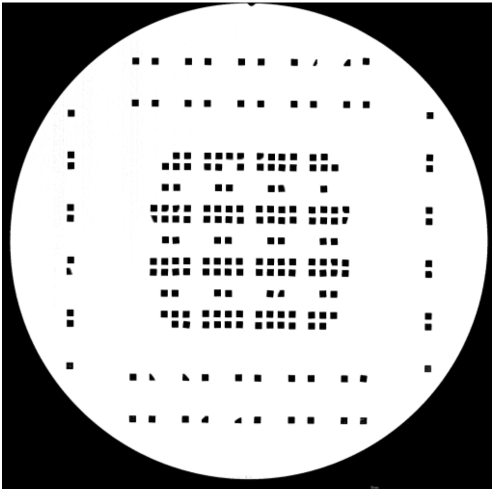


- \+ Efficient cleaning
- \+ Very high transfer rate >95%
- \+ Bonding Yield~100%
- \+ CAD2MASK Holder mask generation during PIC design
- \- Additional cost for holder fabrication

COLLECTIVE DIE BONDING WITH SILICON HOLDER - EXAMPLE

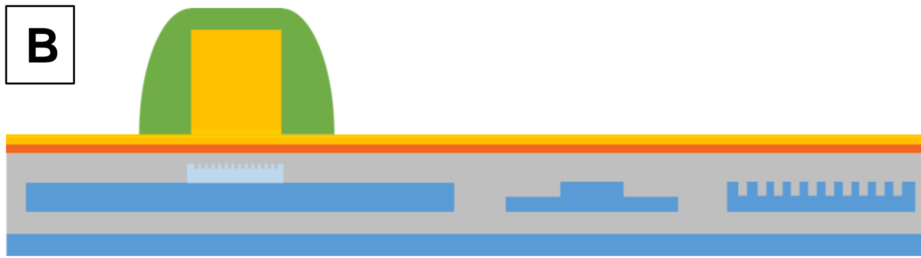

After die Bonding

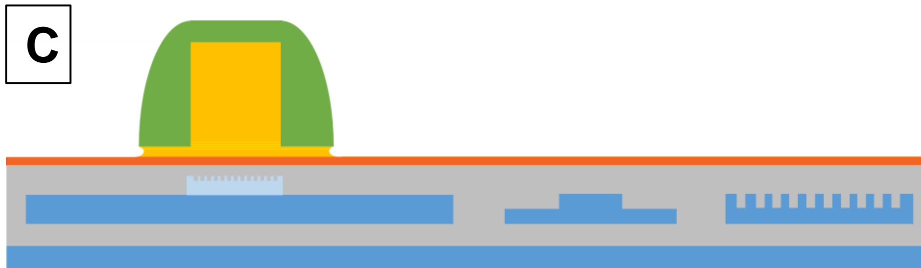

After InP grinding

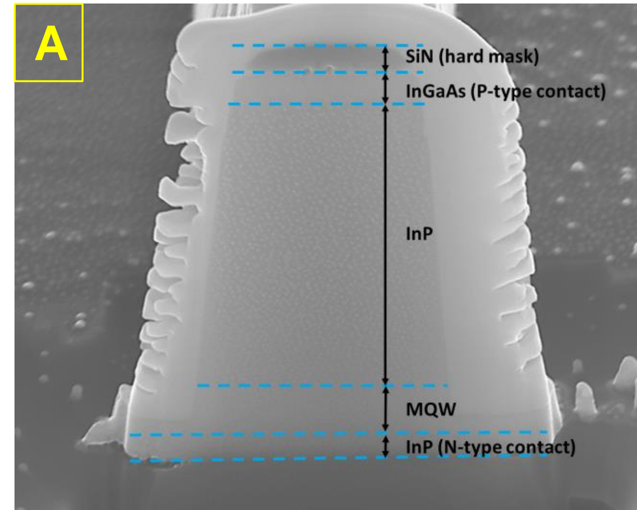

Acoustic characterization

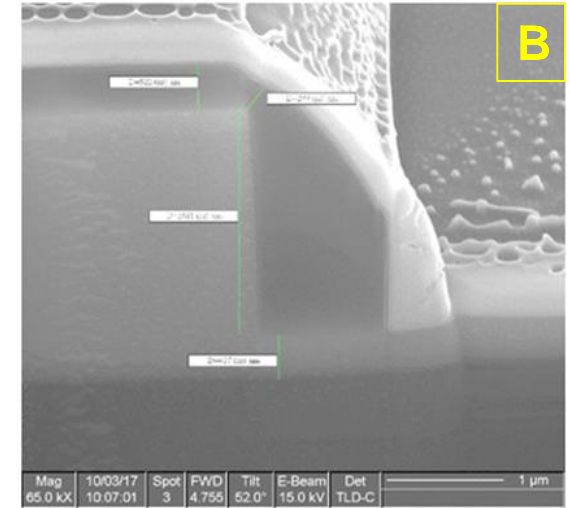
	P01	P02	P03	P04
○ Transferred die:	99 %	99%	99%	70%
○ Transferred die without defects:	75 %	73%	73%	52%
○ Transferred die & bonded on more than 99% of their surface:	87 %	84%	88%	62%
○ Transferred die & bonded on more than 95% of their surface :	91 %	85%	90%	64%

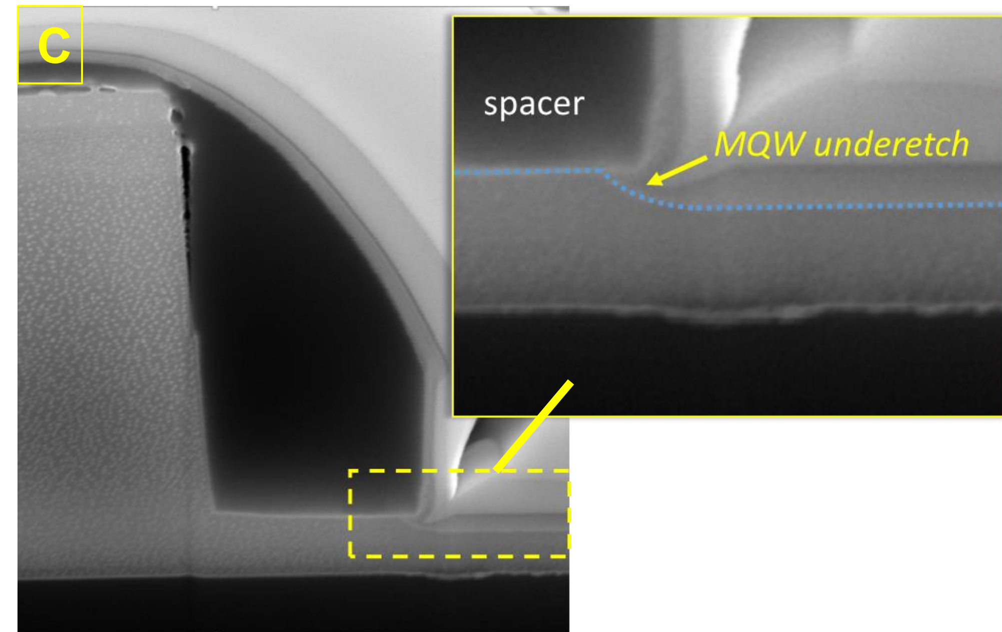
III-V PATTERNING – GAIN AREA DEFINITION



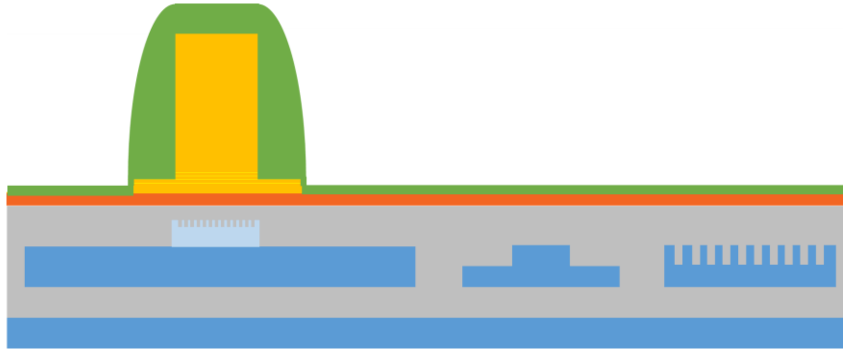




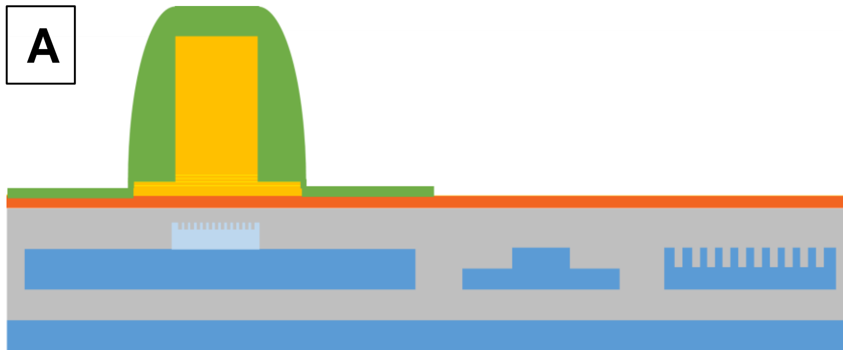




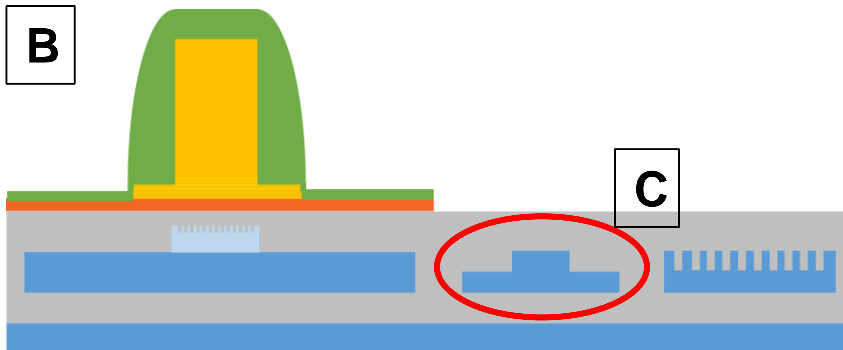
III-V PATTERNING – MESA AREA DEFINITION

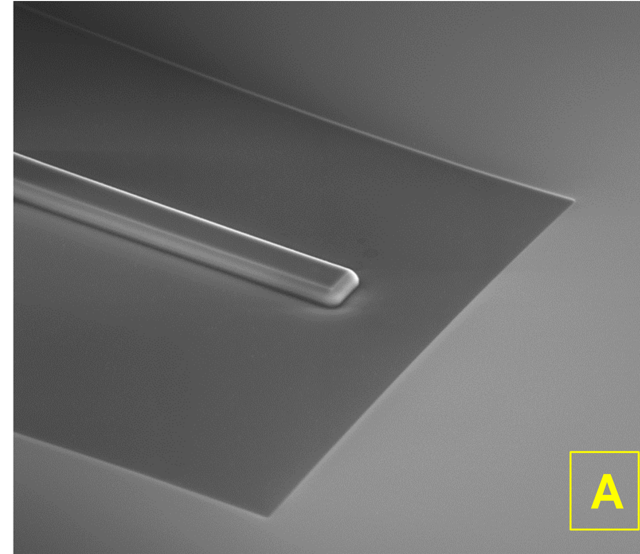


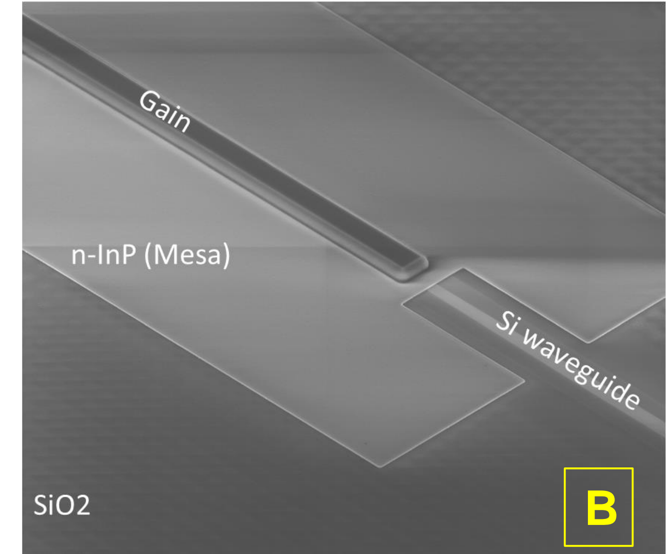
A

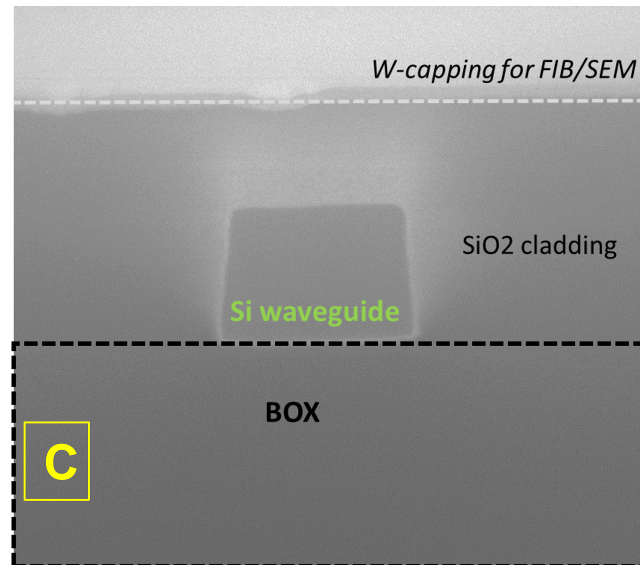


B

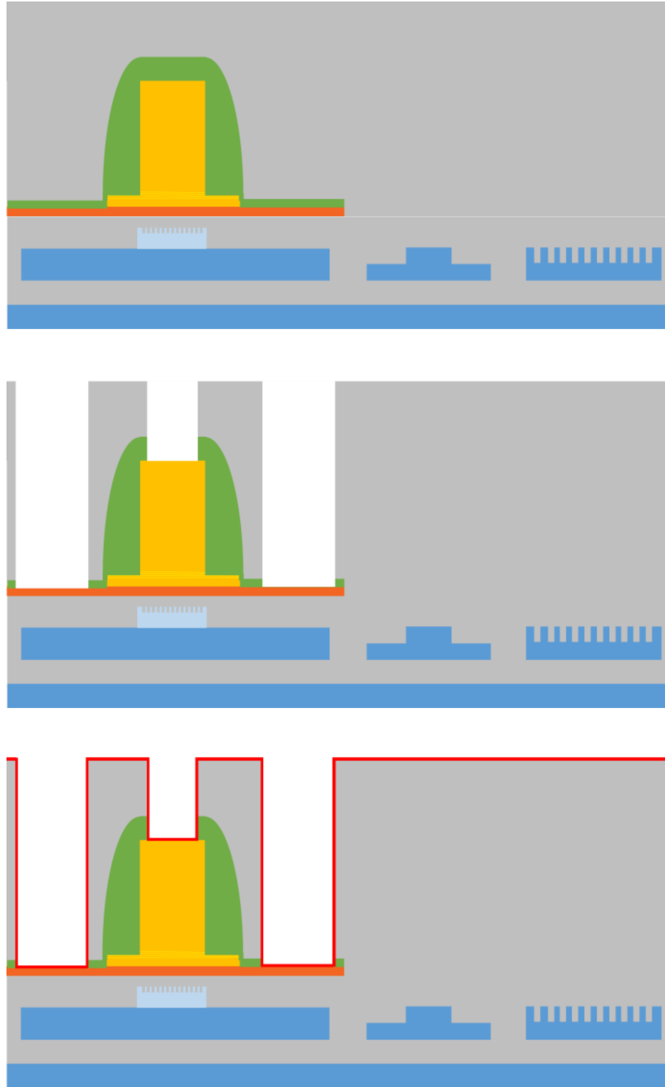


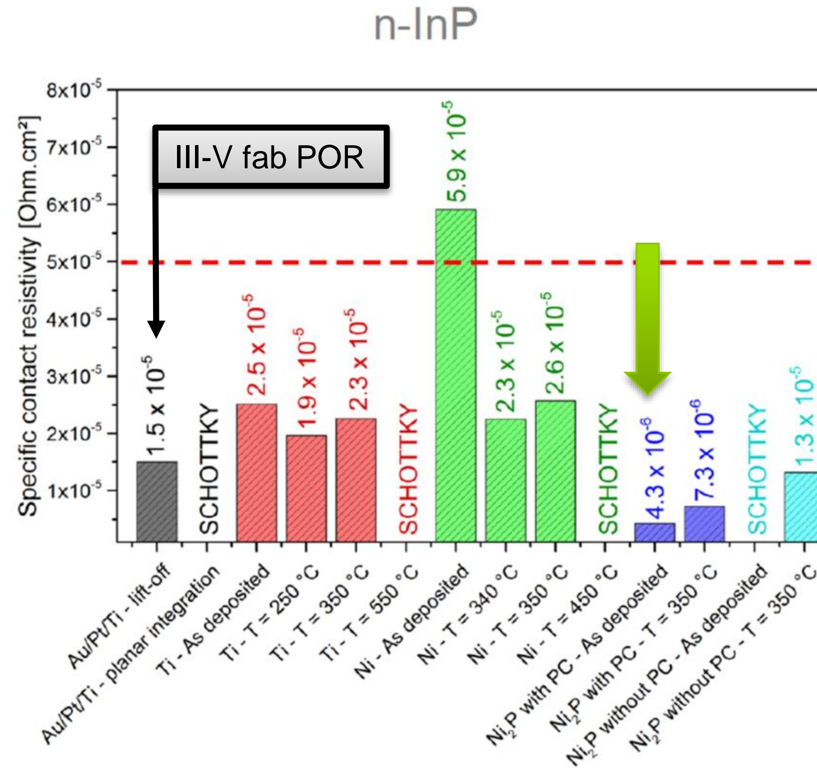


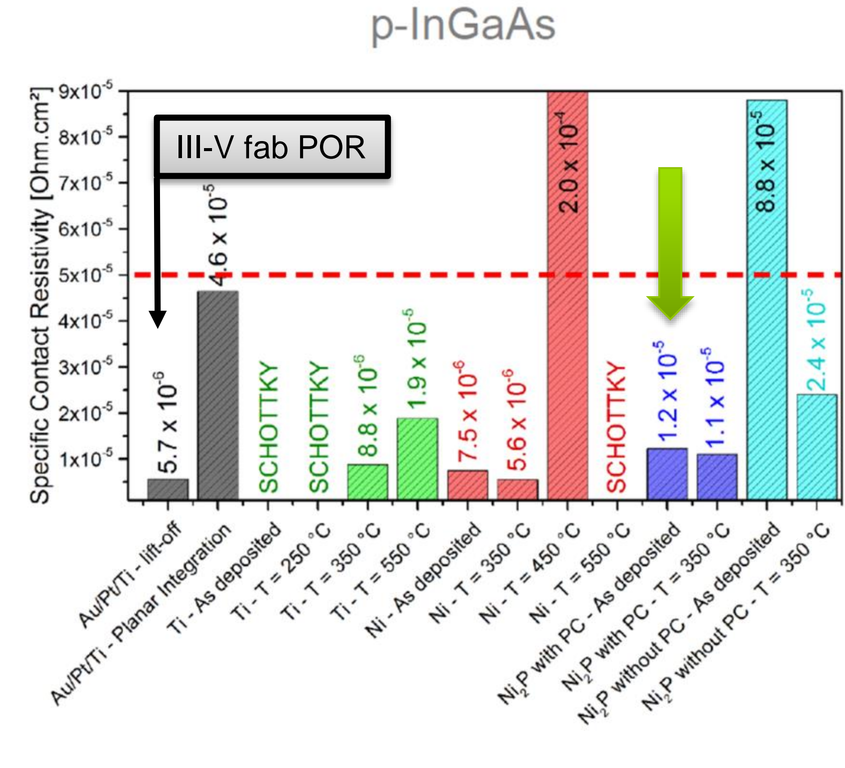




CMOS COMPATIBLE CONTACTS ON III-V

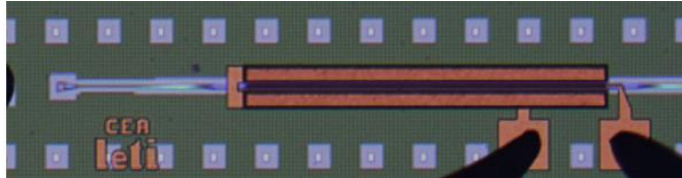


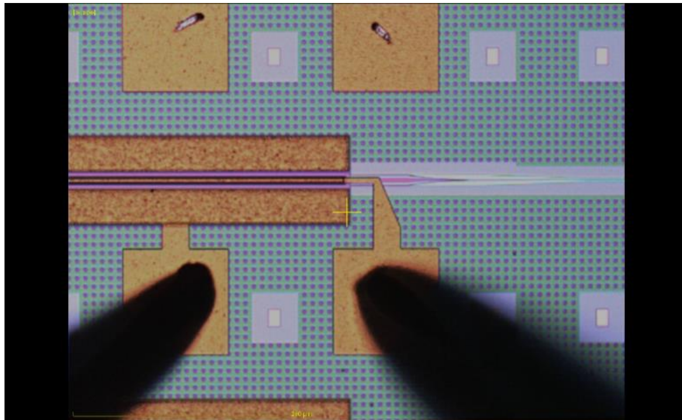




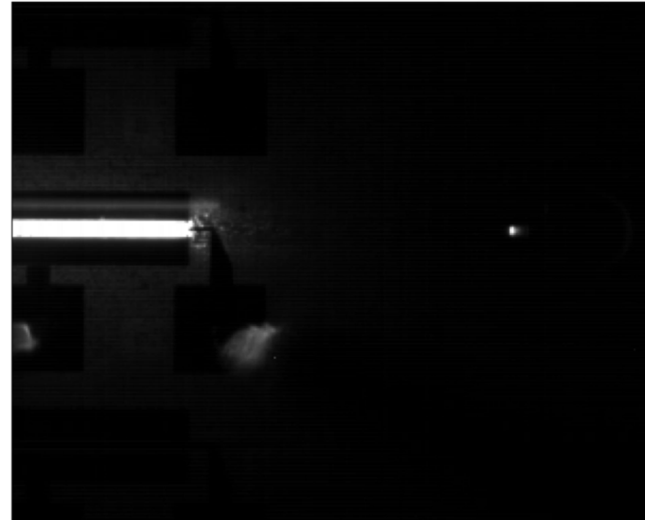
- Best choice:
  - On n-InP: Ni2P wo annealing
  - OnP-InGaAs: Ni with 350°C annealing

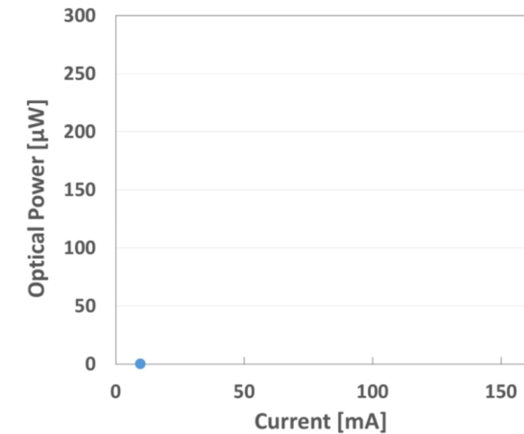
FIRST DEMO ON 200MM SOI WAFER OPTICAL CHARACTERIZATION

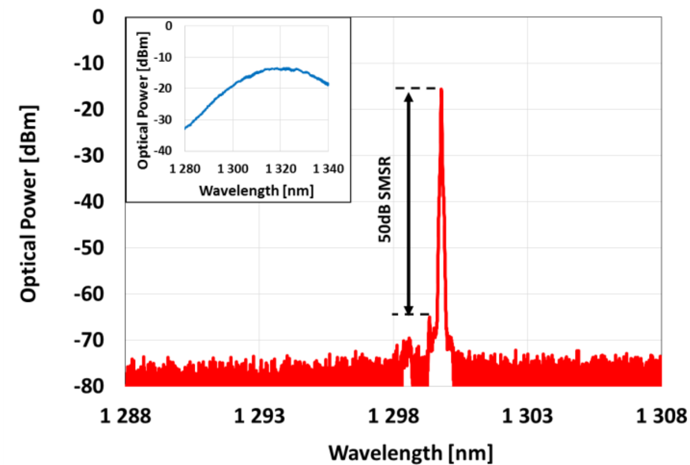




- Only 1 metal layer for this design
- Ni-based N & P contacts



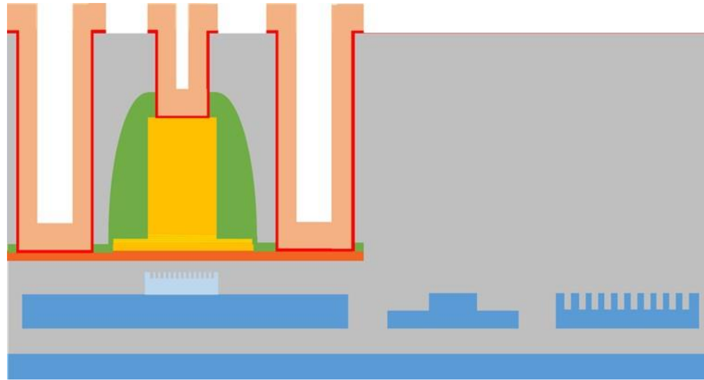


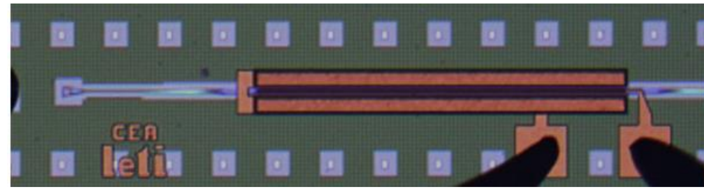


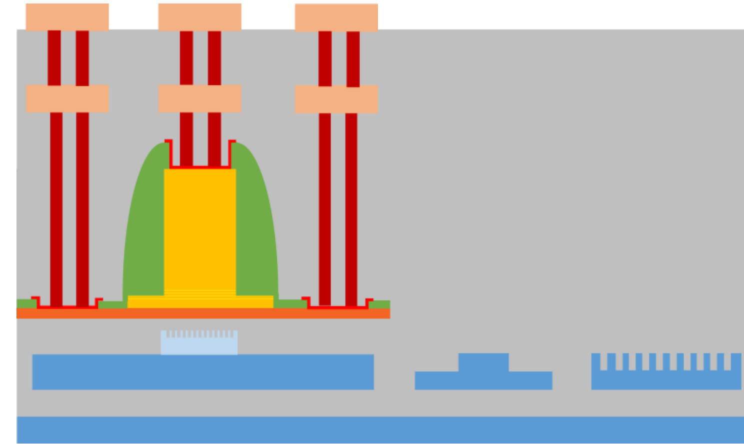
- Ith: 55-65mA
- Rs= 10 Ω
- Max P-Si-waveguide > 3 mW
- Max P-fiber ≈ 1 mW
- SMSR > 40 dB (best 50dB)

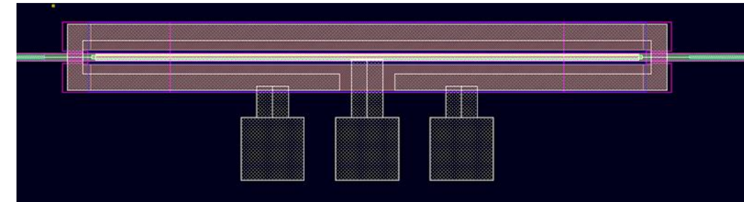
@room temperature

MULTILEVEL PLANAR BEOL

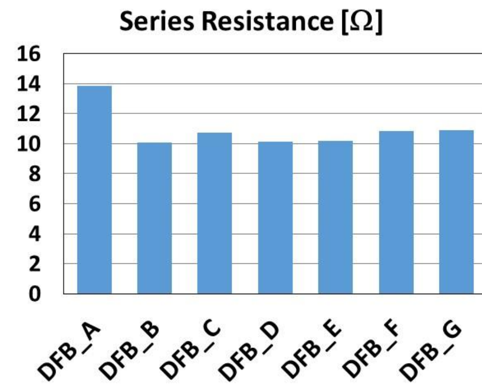




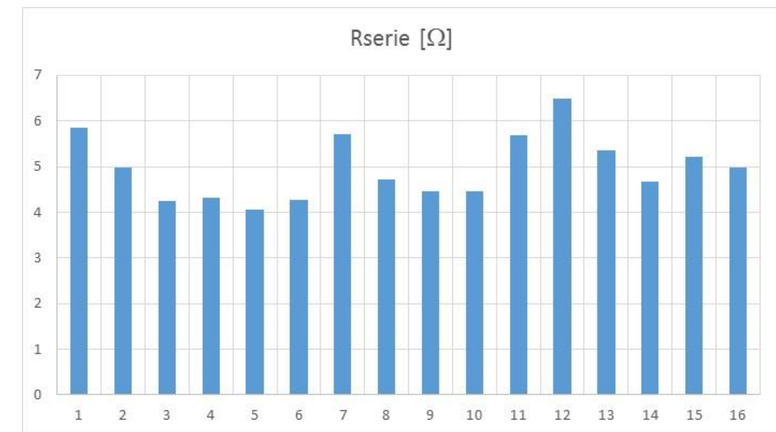




Rserie = [10W-14W]



Rserie = [4W-6.5W]
Mean 4.95 W



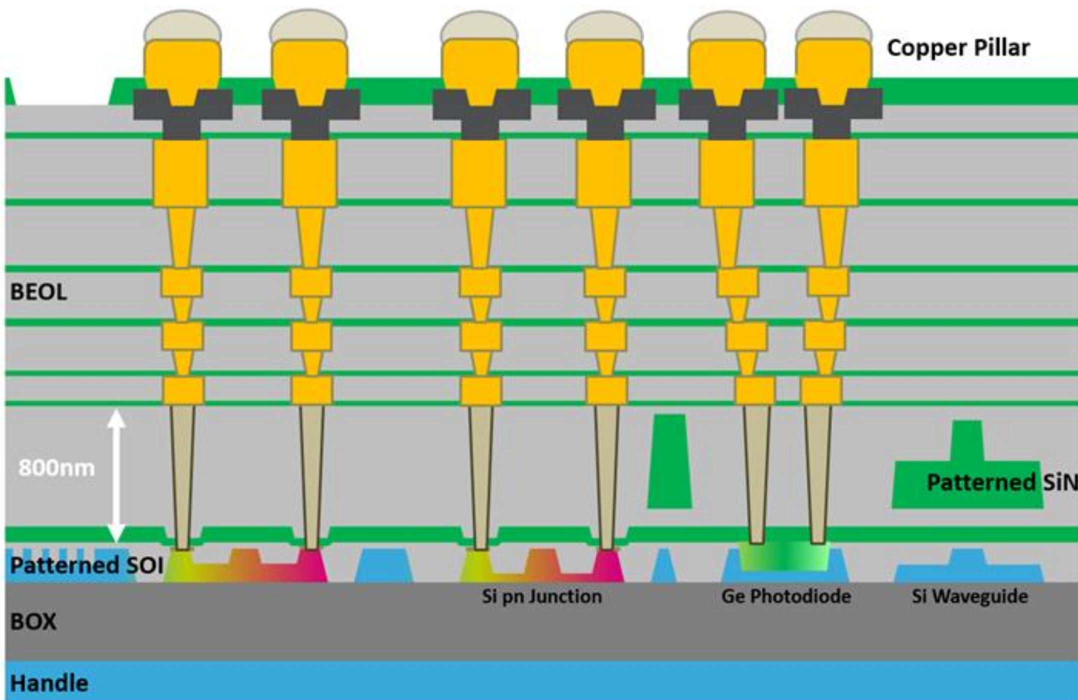
BACKSIDE INTEGRATION (BSI) CONCEPT

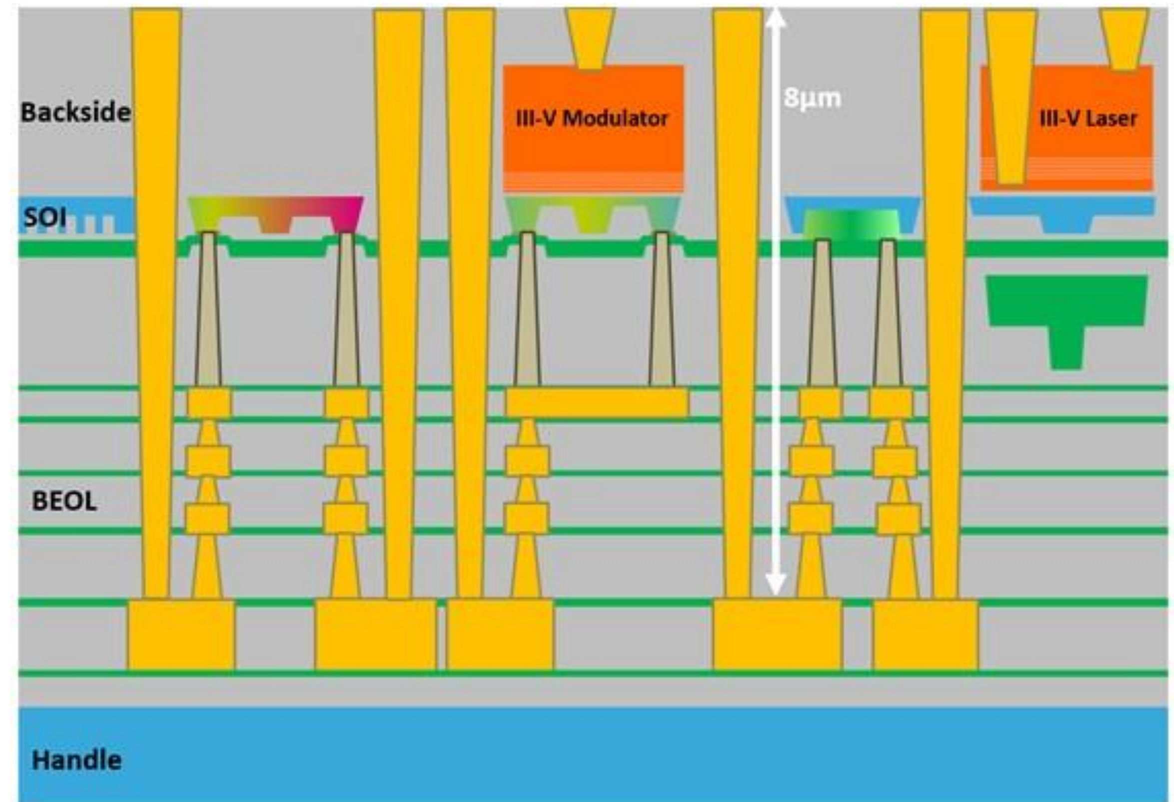
Problems:

1. III-V based device integration with not change on the baseline photonic platform (BEOL)
2. III-V based device integration compatible with a co-integration of SiN devices

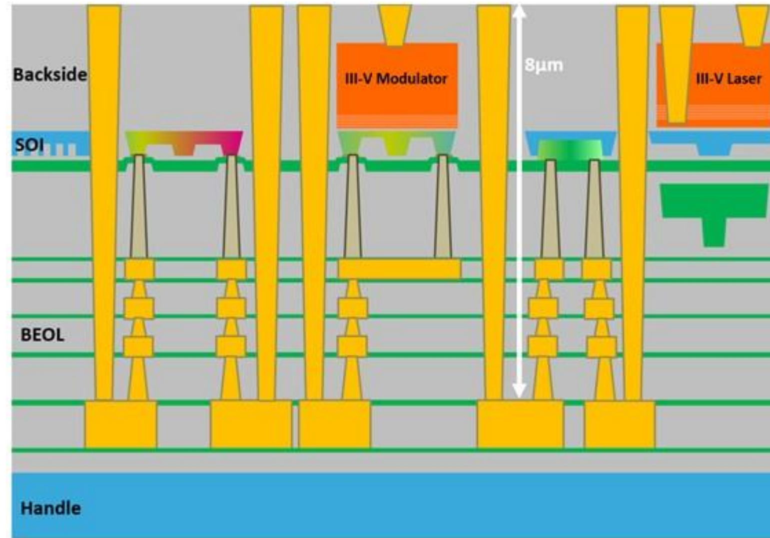
Solution:

⇒ **III-V post processing on the backside of the full silicon photonic platform**

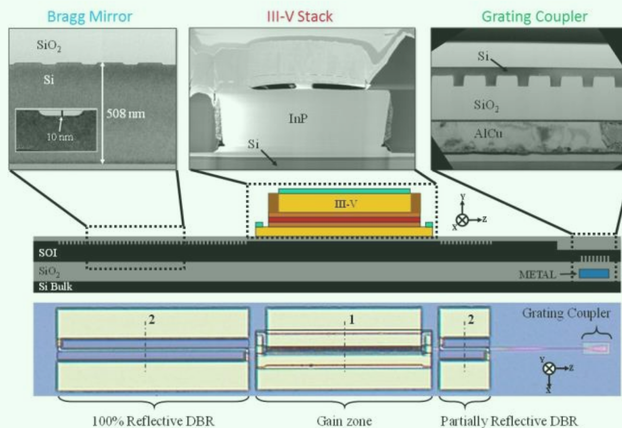


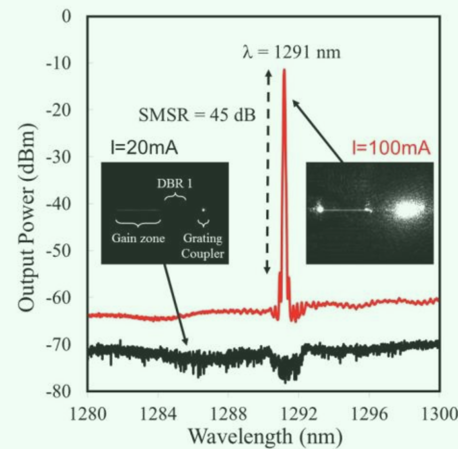


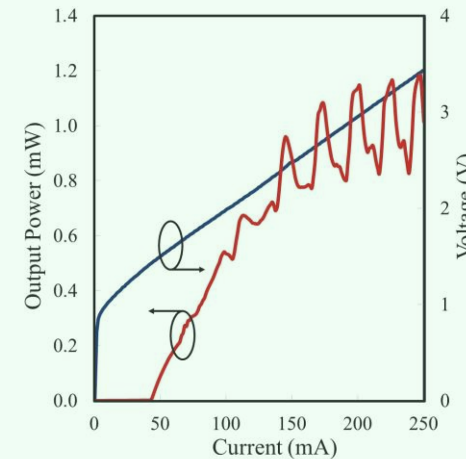
HYBRID LASER BSI DEMONSTRATION

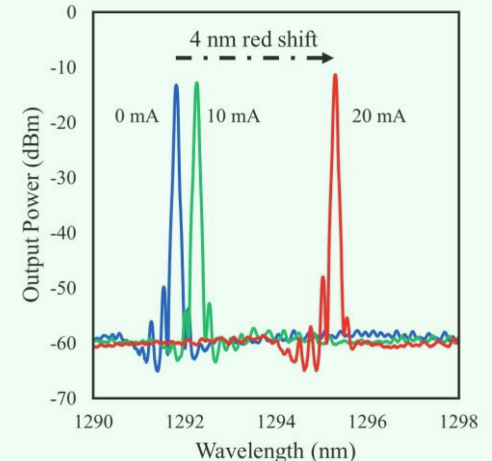


- Integration scheme compatible with any photonic platform
- No impact on the Silicon photonic platform
- Modular integration
- Si photonic platform and laser integration can be done in 2 different fabs
- Only way to have '3D photonic' (SiN or Si level on top of SOI) and laser on the same die
- EIC and Laser @ opposite sides of the PIC
- Demo: Passive + BSI DBR laser done with 100mm process (J. Durel et Al, IEDM 2016)









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SUMMARY

NANOELEC.

- Hybrid III-V/Si laser integration on silicon photonic platform has been extensively demonstrated in CEA-LETI
- III-V die bonding is a key process module for large scale integration of III-V based device
- CMOS compatible process Hybrid III-V/Si laser integration on 200mm and 300mm SOI silicon photonic platform is currently developed
- Backside integration concept allows the convergence of Si, SiN and III-V based device on the same wafer/platform

AKNOWLEDGEMENTS

- LETI’s silicon photonic labs
- LETI’s silicon technology integration department
- STMicroelectronics silicon photonic group

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Thank you

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