D43D Workshop 2018, Grenoble

From 2.5D to 3D Layout Design Environment: Status & Future Challenges for Advanced 3D Packaging

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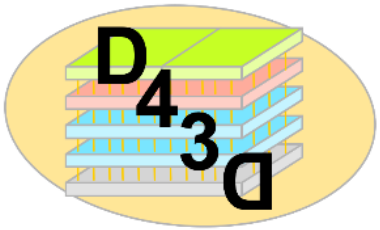


infineon

Acknowledgement

Parts of presented chip package co-design environment have been developed inside the following EU funding projects:

› MEDEA+ CoSiP
Chip/Package/System Co-Design
An Enabler for Compact System-in-Package Solutions

› CATRENE SiPoB-3D
Co-Design for System-in-Package-on-Board.
Managing Complexity and Diversity to Create Novel 3D Compact Systems.

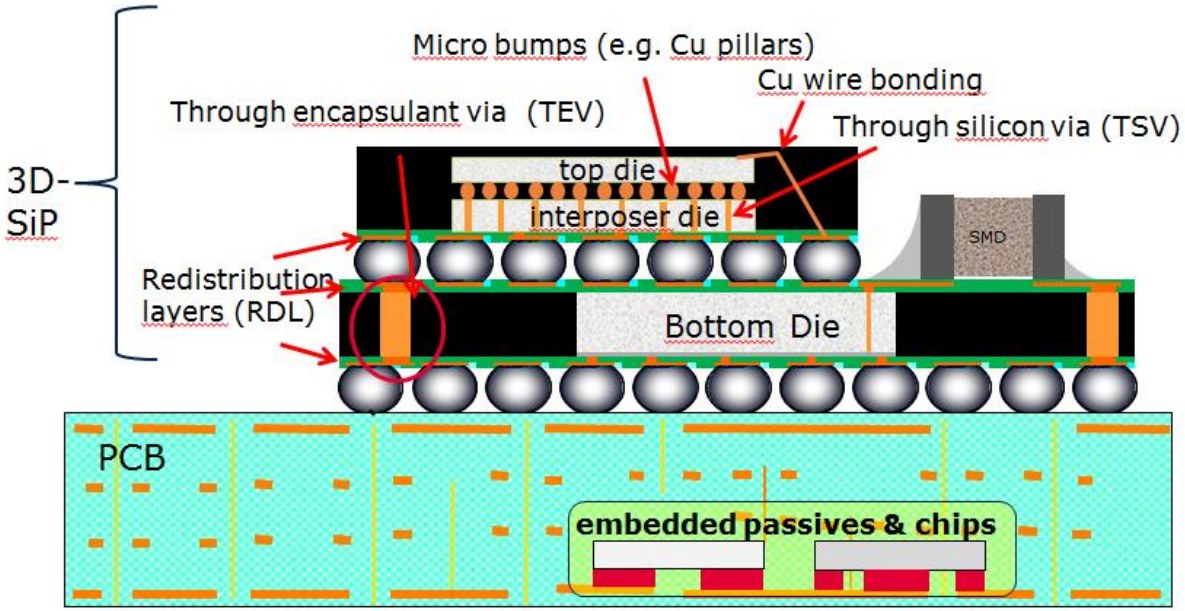
Agenda

1. Challenges for 2.5D & 3D co-design methodology
2. Assembly Design Kits
3. Common chip-package layout design environment
4. Structured, efficient co-design data exchange
5. Future challenges

Agenda

1. Challenges for 2.5D & 3D chip-package-(PCB) co-design methodology
   - Design complexity
   - Distributed design teams
   - Communication
2. Assembly Design Kits (ADKs)
3. Common chip-package layout design environment
4. Structured, efficient co-design data exchange
5. Future challenges

Degrees of Freedom in IC/PCB System Design



Additional degrees of freedom like

- exploitation 3rd dimension → miniaturization, increase of electrical performance
- mix of chip technologies → choose the best in terms of cost & performance
- re-use of existing chips → faster time-to-market
- mix of devices of different vendors → vendors can focus on their core competence
- …

are available for overall system optimization for a given application

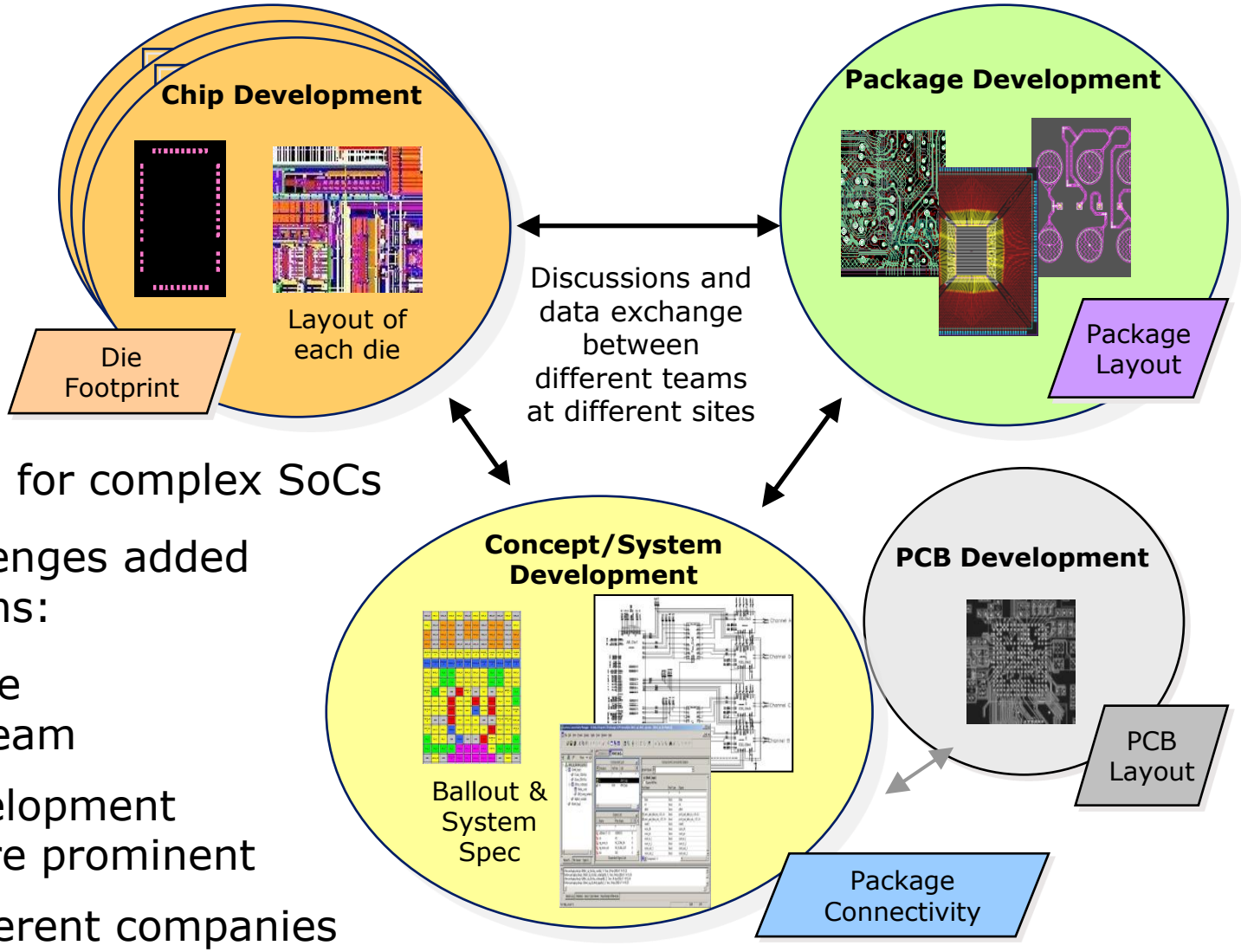
→ advantages for customer – and concept engineers

→ challenge for design engineers

Engineering Roles in Complex System Design

- Complex 3D-SiP (+PCB) products require much more interaction during design here …

Distributed Design Teams



- Already existing for complex SoCs
- Additional challenges added in 3D-SiP designs:
  - More than one chip design team
  - Package development becomes more prominent
  - Teams in different companies

Communication is a Must

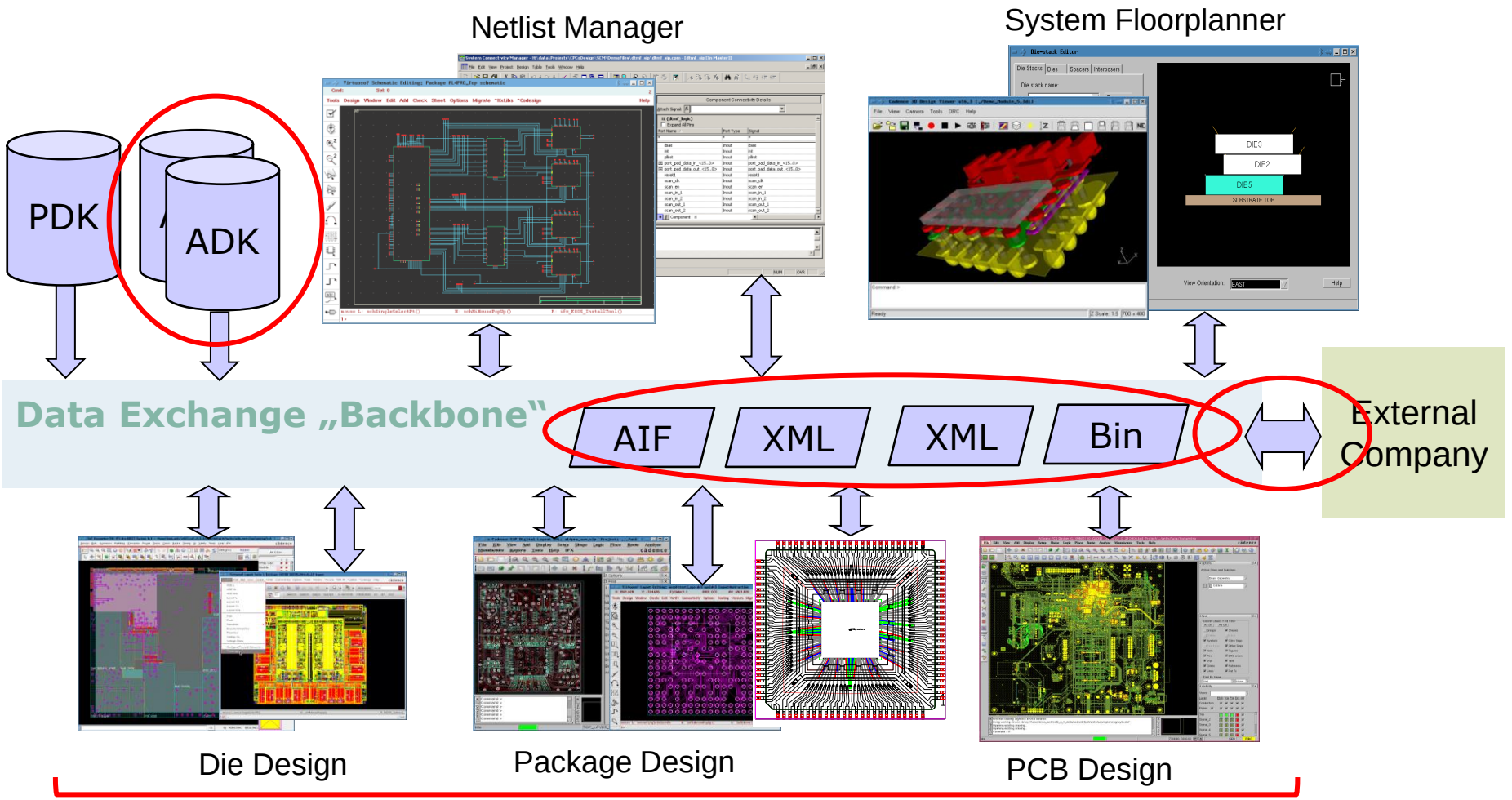
- Management tasks: Coordination, alignment, project planning, …
- Design tasks – "Engineering Change Order" (ECO) loops
  - Technical alignment & discussions → human centric tasks
    Design Methodology can help by
    - defining clear workflows
    - defining clear roles & responsibilities
  - Design data exchange → software tool centric tasks
    Design Methodology can help by
    - providing novel automation features (EDA)
    - defining easy-to-use tool flows
    - defining easy-to-use & complete file data formats

Improving Chip-Package-(PCB) Co-Design Methodology

- Goal: Make design tasks less error prone and faster
  - → Simplify ECO loops
  - → Reduce number of ECO loops

- Several solutions have been developed in EU funding projects CoSiP and SiPoB-3D
- and have been rolled out successfully within Infineon:
  - Assembly Design Kits (ADK)
  - Common chip+package layout environment
  - Structured, efficient co-design data exchange
    - within the same semiconductor company → "CoSiP Backbone"
    - between different companies → "SiPoB-3D Gateway"

Infineon SiP Codesign Environment

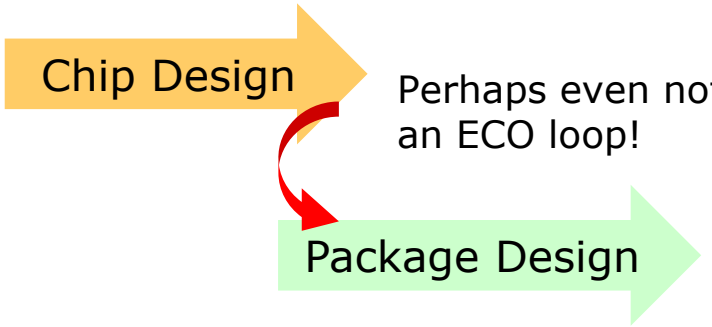


Agenda

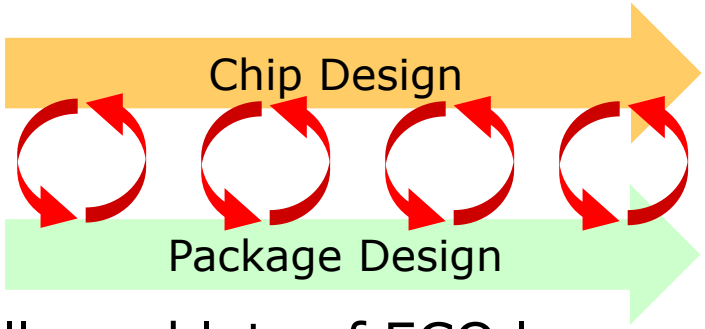
1. Challenges for 2.5 & 3D co-design methodology
2. Assembly Design Kits (ADKs)
   - Parallel development
   - Learning from chip design:
     PDK (frontend process design kit) → ADK
   - Infrastructure & content
3. Common chip-package layout design environment
4. Structured, efficient co-design data exchange
5. Future challenges

Reduce Number of ECO-Loops (1)

- Typical human approach: Reduce number of ECO loops and focus on local optimization
  - → Overall product not optimized
  - → Sequential design steps



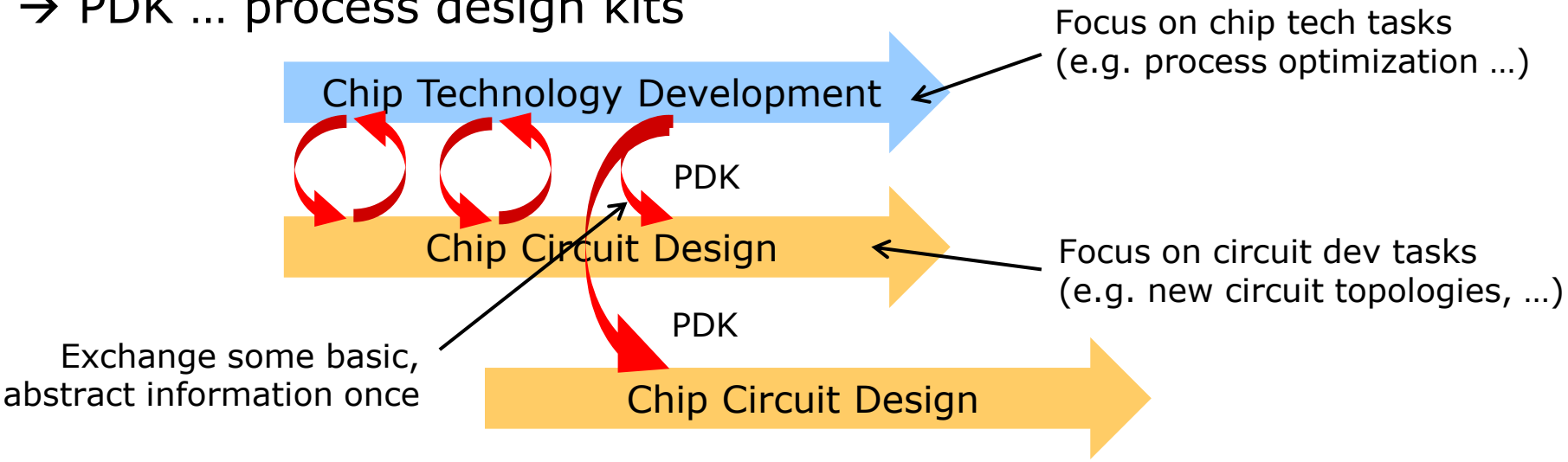
- What would we like to achieve?
  - → Parallel design
  - → Global optimization



Disadvantage: It seems that we will need lots of ECO loops. Difficult to organize in distributed teams.

Reduce Number of ECO-Loops (2)

- How to enable teams to work in parallel, but with less ECO loops?
- Let‘s learn from other areas in semiconductor industry …
  → PDK … process design kits



  - Decoupling of chip technology development and chip circuit design
  - Most efficient, if PDK can be re-used in further chip circuit designs

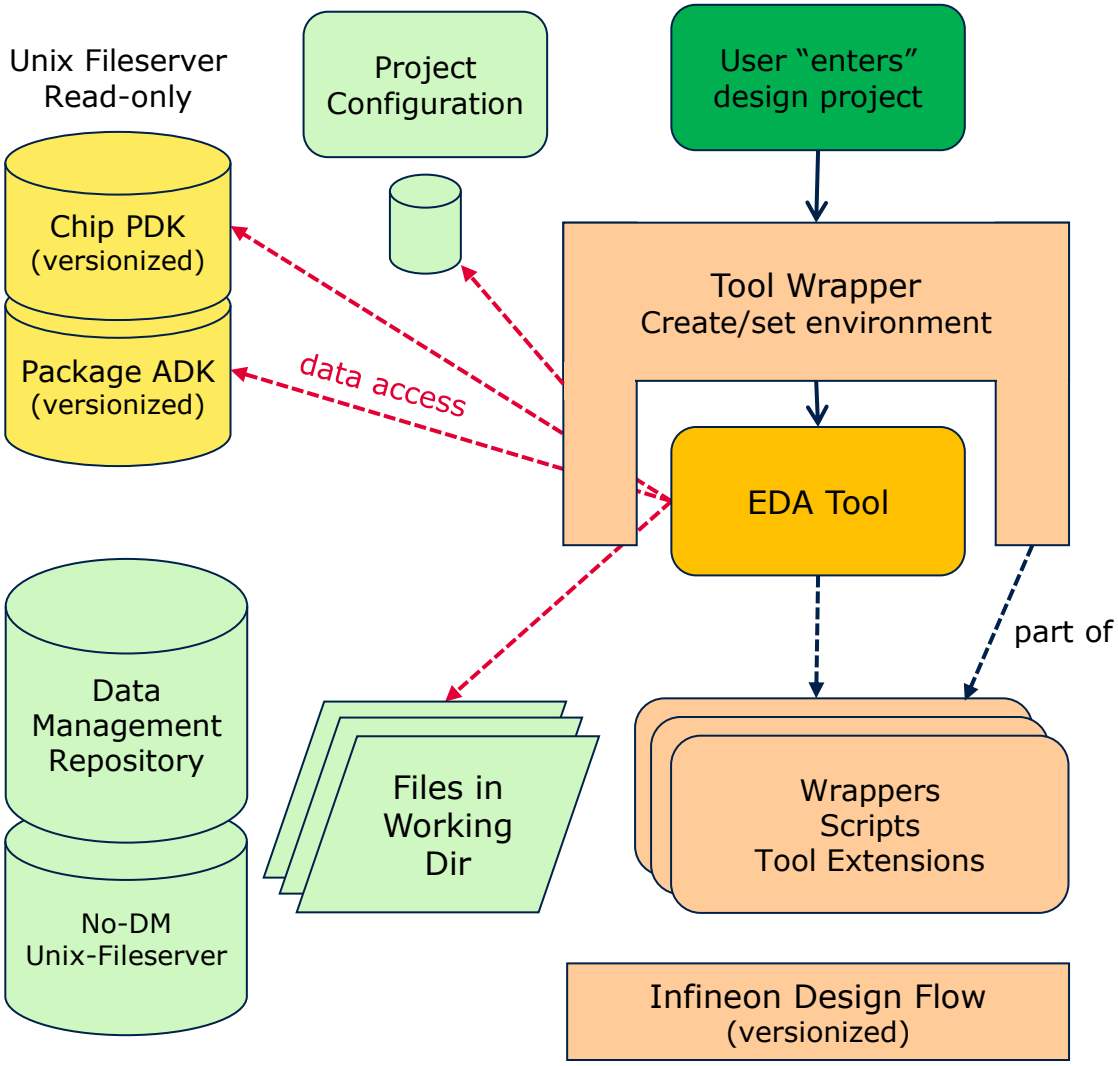
The Idea of ADK is Born!

- ADK … Assembly Design Kit
  - Abstraction of assembly technology specific information and constraints like design layers, rules, materials, …
  - Should be defined and compiled by
    - In-house assembly / packaging / backend department
    - Assembly subcon (just like a PDK is offered by chip foundry)

- Obstacles for ADK introduction:
  - No common foundation like a common design tool landscape – because of big differences in assembly technologies
  - Additional effort for some contributors. Examples:
    - Need to express assembly design rules in a more abstract way
    - Less flexibility after the release of an ADK

Design Infrastructure Including ADKs

- Project configuration
  - PDK
  - One or more ADKs
- Traceability by
  - Read-only project configuration
  - Design flow version
  - PDK + ADK versions

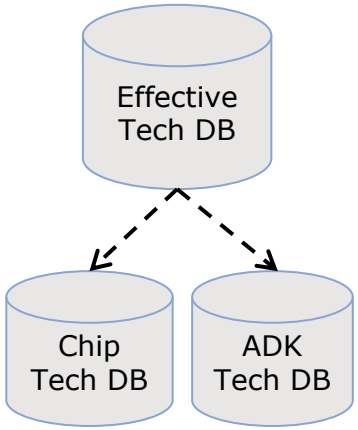


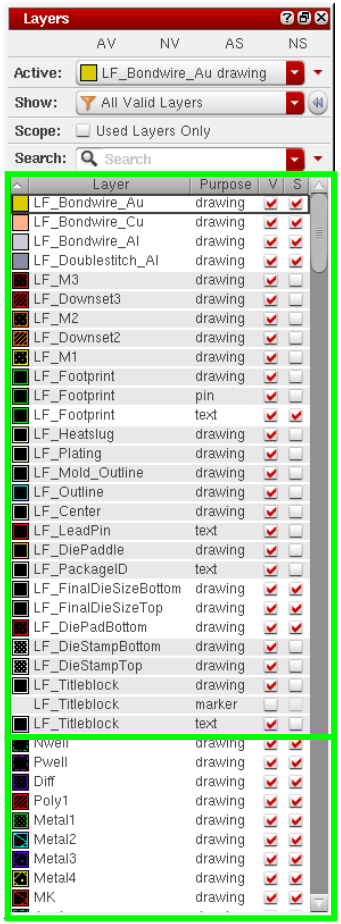
ADK Content – Examples (1)

- Layer definition & layer mapping (support of different layout design tools)

Virtuoso Layerstack (chip + package layers combined together

Based on incremental technology database)

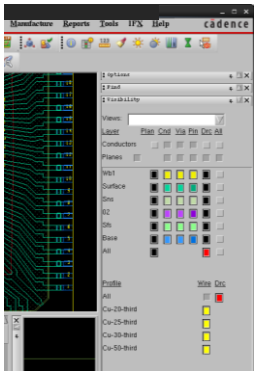




ADK

PDK

Layers in CDNSIP

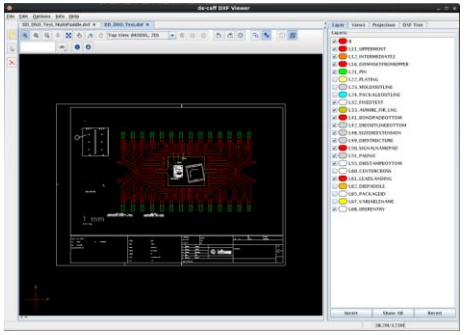


Layers in other files

Gerber

GDS

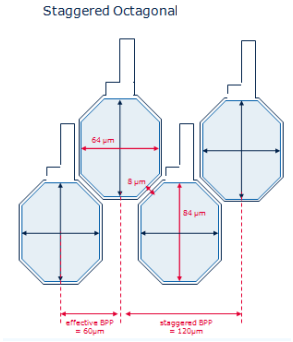
Layers in AutoCAD/DXF



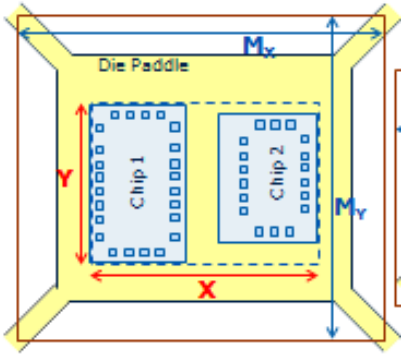
ADK Content - Examples (2)

› Assembly Design Rules

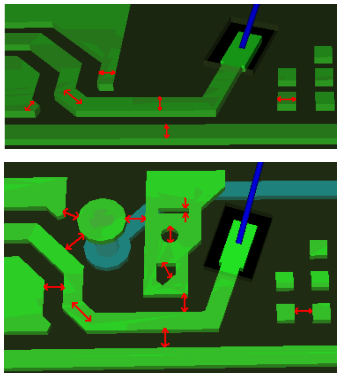
Chip related



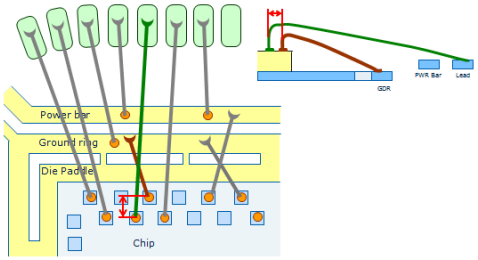
Chip Placement



Package related



Bondwire related



› Different rule checking engine in use:

- On-line checks, if available (e.g. in CDNSIP)
- Mentor Calibre based (programmable)
- RAVEL based (engine available in CDNSIP)
- Checks in Skill code

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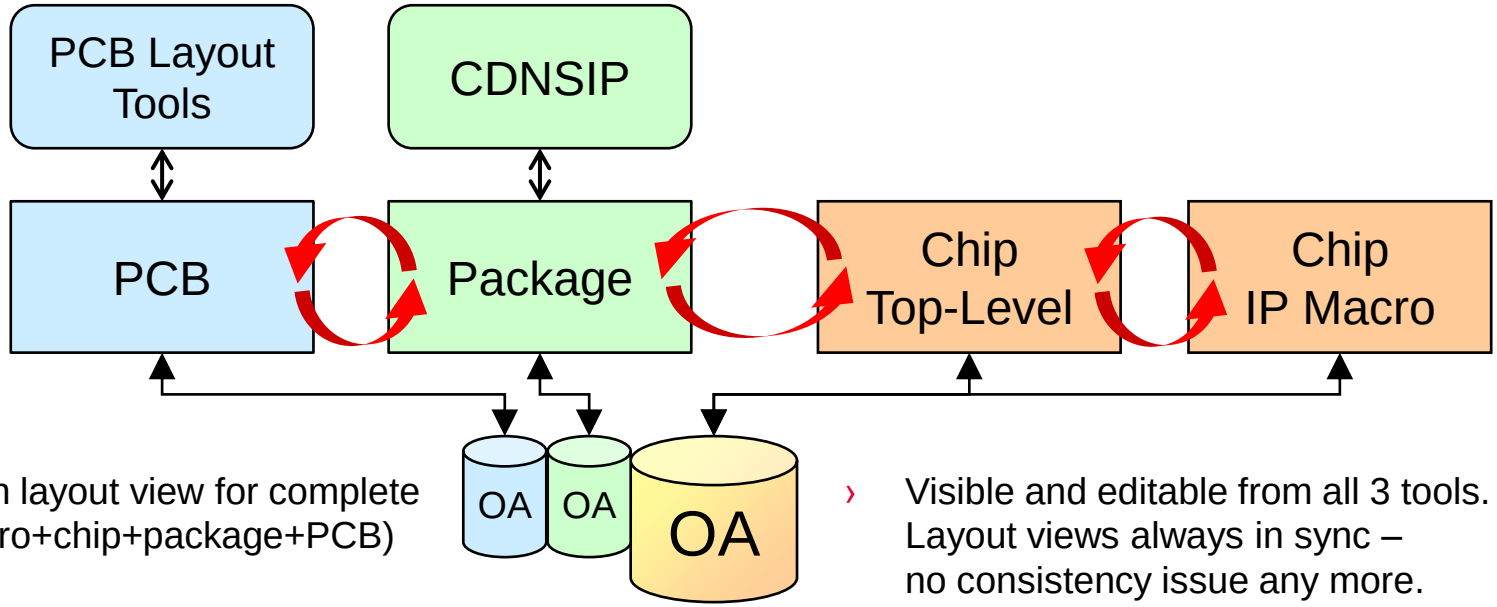
2. Assembly Design Kits (ADKs)
3. Common chip-package layout design environment
   - Proof-of-concept: Exploitation of existing 2.5D software
4. Structured, efficient co-design data exchange
5. Future challenges

Common Layout Environment

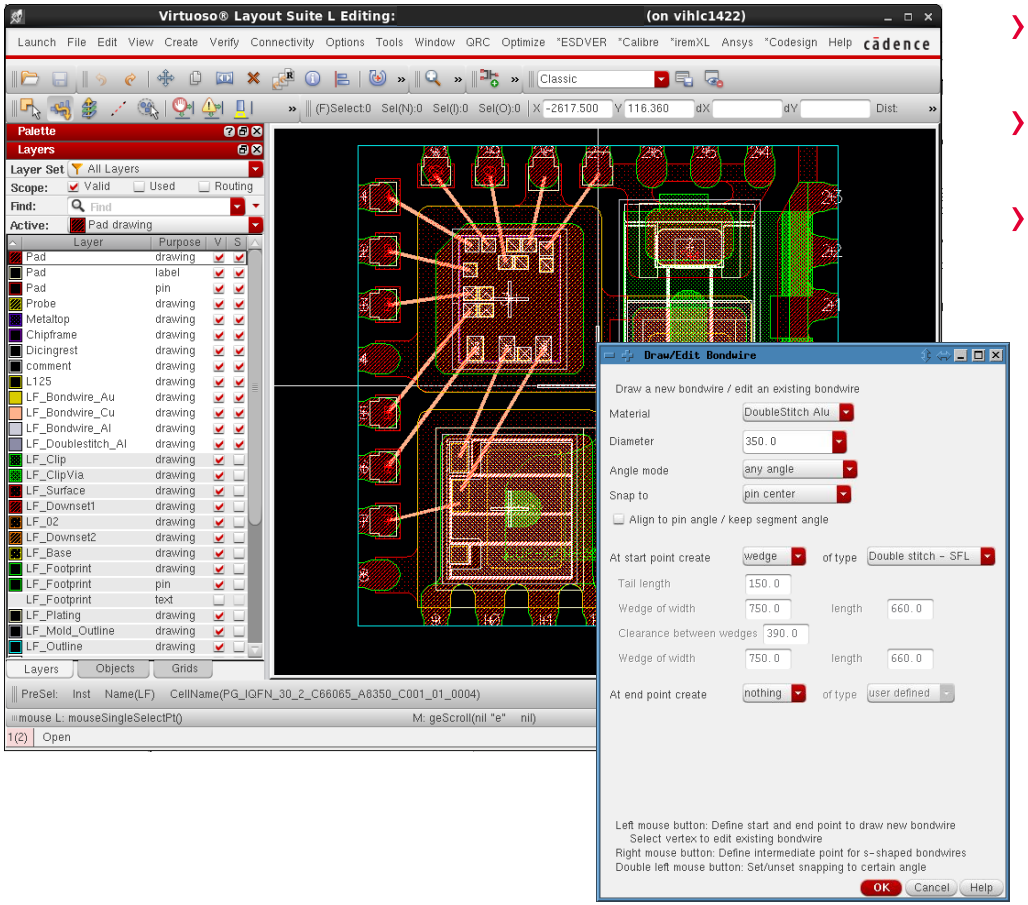
- Current situation: **Different layout tools** in place for chip, package layout and PCB
- ECOs and other design tasks become easier and faster, if design could be shared in **one common layout environment**
- We decided for OA database & Cadence Virtuoso for a prototype because
  - it can store the complete chip layout
  - our biggest internal design community is using it



- One common layout view for complete system (macro+chip+package+PCB) inside OA
- Visible and editable from all 3 tools. Layout views always in sync – no consistency issue any more.

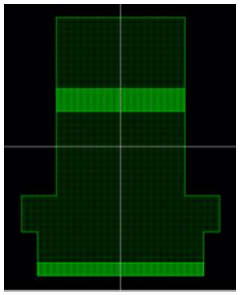
Layout Design with Bondwires

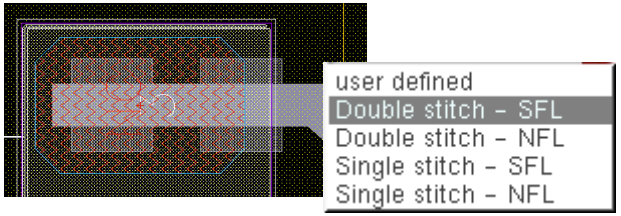
- Already in use for several package technologies like QFP, QFN, DSO, TO, SO, …



Support of

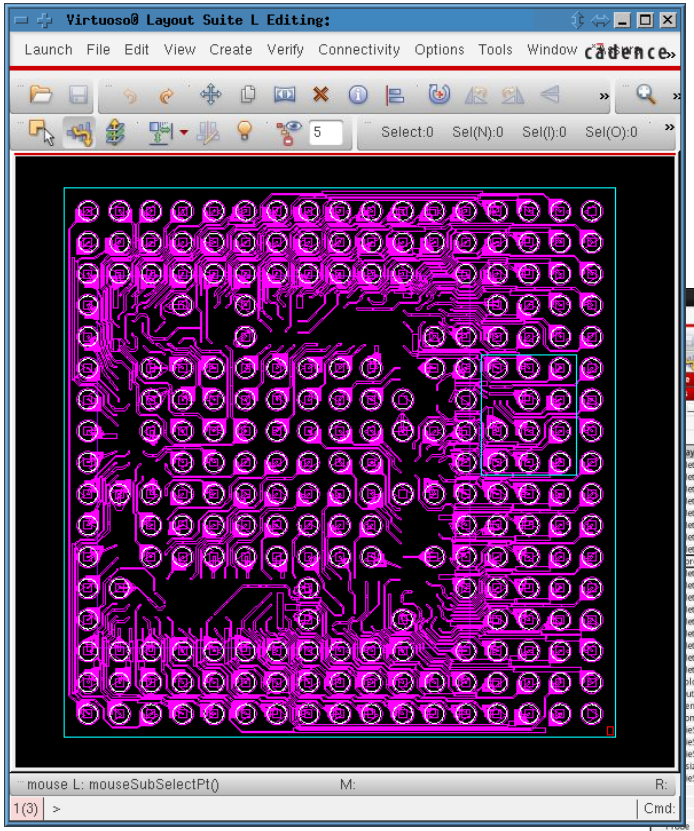
- SiP (several chips)
- Clips
- Bondwire Design
  - Material, bondwire profile
  - Different end-points
    - Double stitch
    - Nailheads
    - Wedge-on-bump

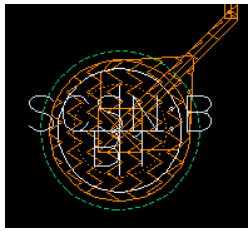


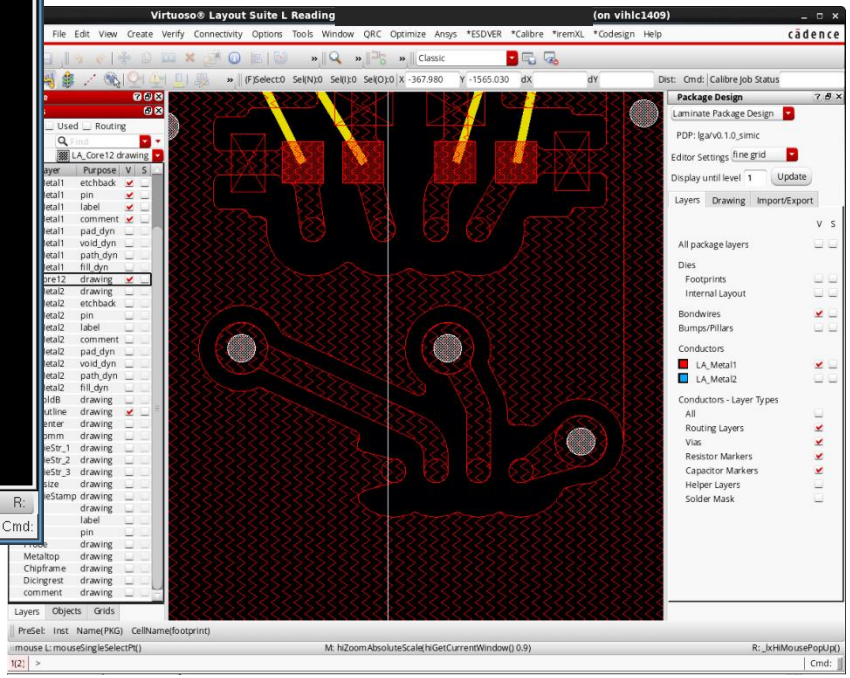


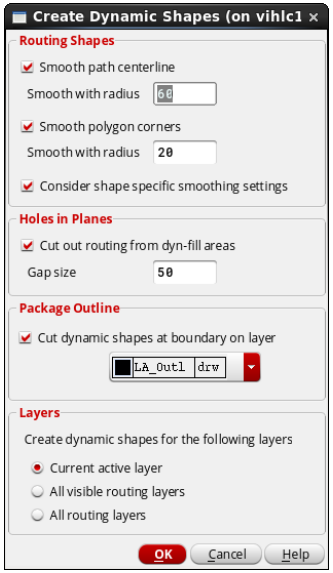
Laminate & eWLB Design

- Virtuoso can also be used for eWLB & laminate design, but requires some extensions, like
  - Ballout generator
  - Automatic tear drop generation
  - Padstack editor
  - Automatic smoothing & plane cutting









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1 Challenges for 2.5 & 3D co-design methodology

2 Assembly Design Kits (ADKs)

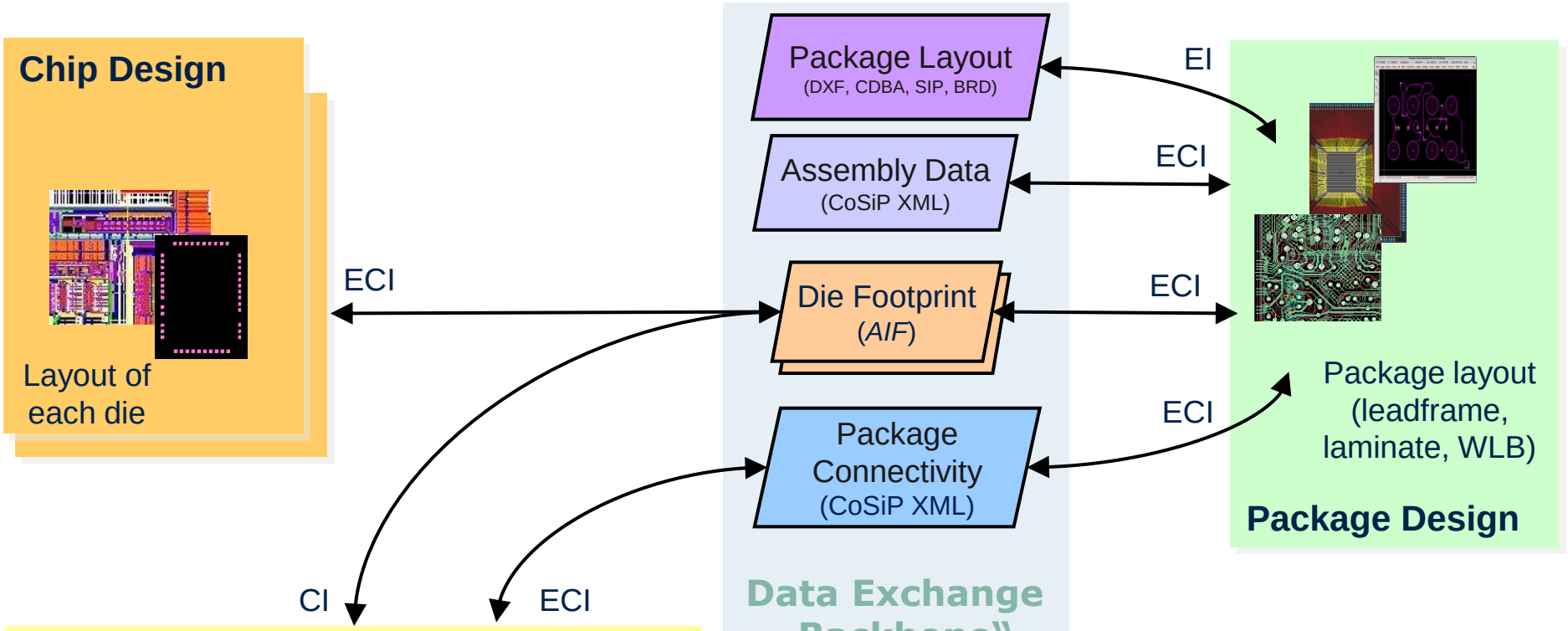
3 Common chip-package layout design environment

4 Structured, efficient co-design data exchange

- within the same semiconductor company: "CoSiP Backbone"
- between different companies: "SiPoB-3D Gateway"

5 Future challenges

Versatile File-Based Codesign

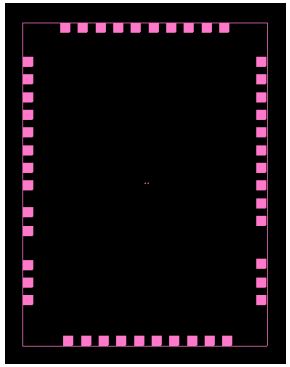


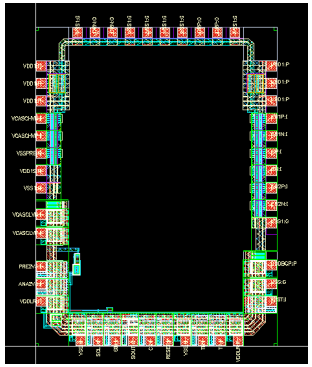
Tools have been enhanced with necessary interfaces:

- E=Export, C=Compare, I=Import
- Scripts in Skill, Tcl, Perl, and Java

Common Data Formats - Example Die Footprint

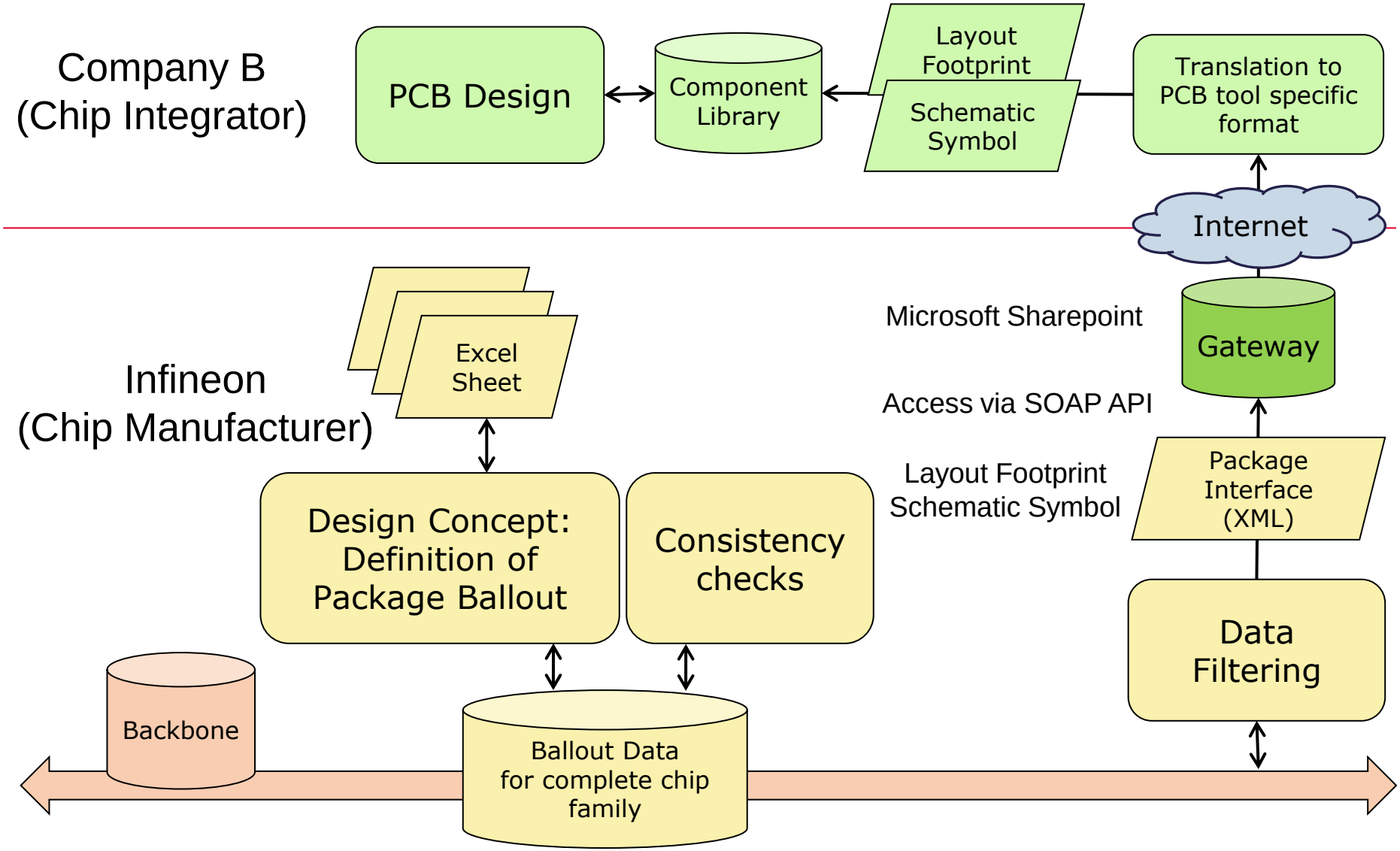
- Die Footprint
  - Die size (incl. scribe line)
  - Pin (= pad/bump/ball)
    - number
    - name from chip point of view
    - x/y coordinates
    - shapes & sizes
  - Additional shapes and properties ('constraints', like no-route regions, comments for some regions etc.)





- Potential file formats
  - AIF: proprietary (www.artwork.com), but ASCII
  - DDX: IEC 62258-2 (last update 2011), standard for KGD business, no focus on design
  - LPB: IEEE 2401 (2015), XML, mainly used in Japan today

Inter-Company Data Exchange "SiPoB-3D Gateway"



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1 Challenges for 2.5 & 3D co-design methodology

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3 Common chip-package layout design environment

4 Structured, efficient co-design data exchange

5 Conclusion & Future challenges

Conclusion & Future Challenges (1)

- Main challenge for chip-package-PCB co-design methodology is optimization of communication between design teams

- Assembly Design Kits:
  - ADKs have been introduced successfully for package technologies in Infineon design environment
  - Future plans & challenges:
    - Exploit modular ADK concept for further applications like probing technologies and PCB design
    - Further productivity improvement would be visible, if assembly subcon/OSAT could provide ADK + “reference design flows” on their own

Conclusion & Future Challenges (2)

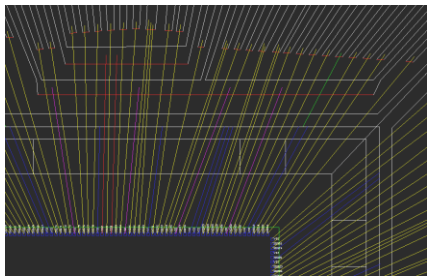
- Common layout environment in Cadence Virtuoso
  - Productive SiP design in leadframe, laminate, and eWLB technologies can be carried out in a common layout environment limited to 2.5D, showing advantages by
    - speeding up ECO loops between design teams
    - ensuring that overall layout keeps in sync & defining latest version
    - acting as a source for final physical sign-off checks (and electrical simulation as well)
  - Infineon had to add several features (by Skill scripts) on its own

→ In some cases feature performance limits the size of SiP

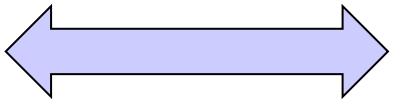
→ EDA vendors could offer solutions also fitting to biggest SiPs

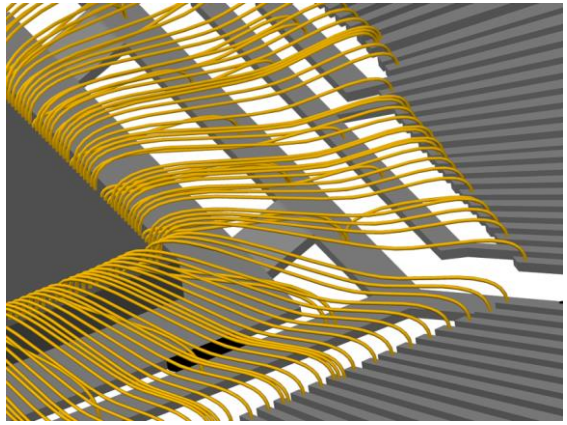
Conclusion & Future Challenges (3)

› Tighter link between mostly 2.5D/2.75D (electrical) E-CAD and true 3D (mechanical) M-CAD environments



2.5D E-CAD with layers
2.75D with additional properties





True 3D M-CAD tools

– Data exchange:
  – Today: Typically unidirectional E-CAD→M-CAD and geometrical data only
  – Future: Bidirectional including additional "electrical properties" like materials, electrical nets, …

Part of your life. Part of tomorrow.

Infineon