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Wireline Communication in 2.5- and 3-D ICs

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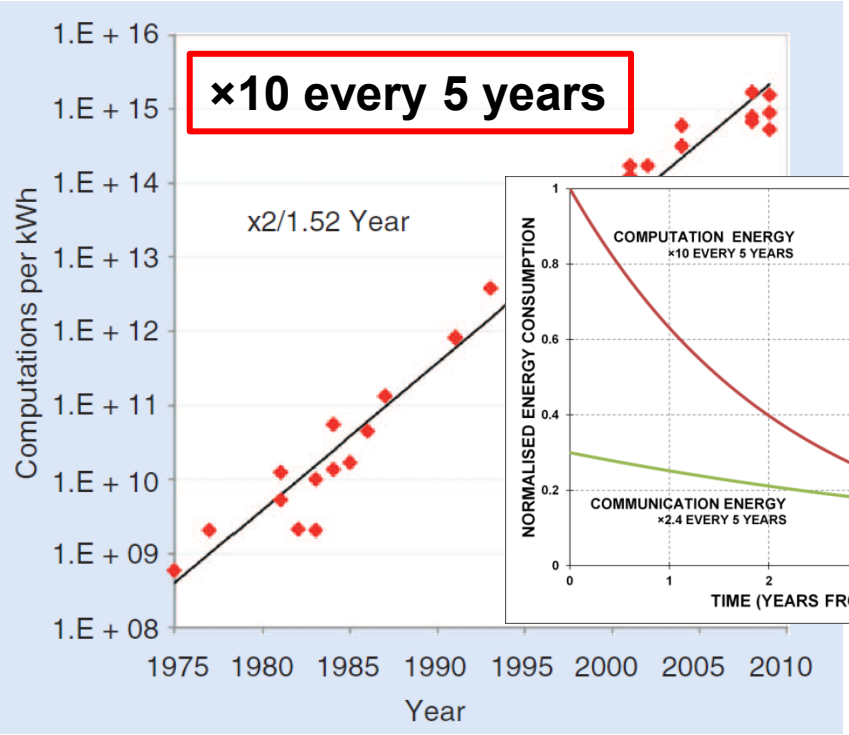
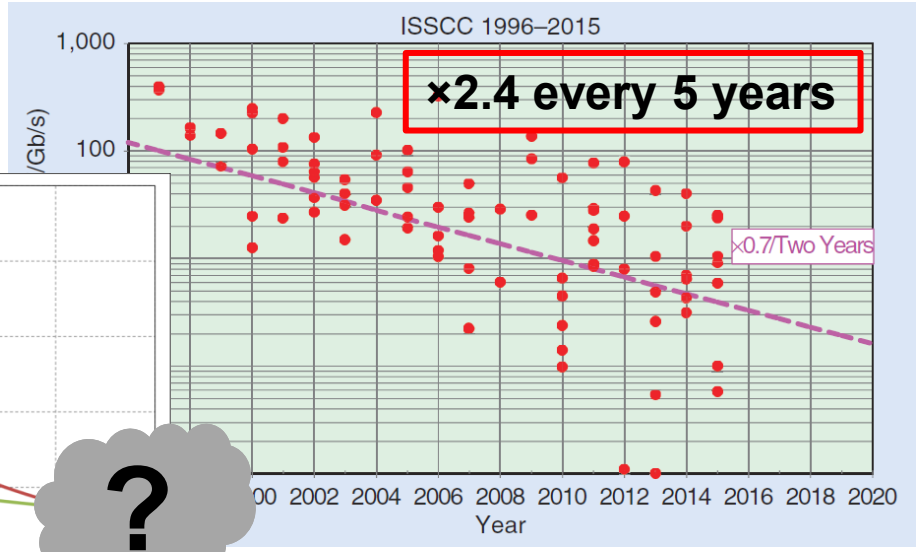
Why Communication Matters?

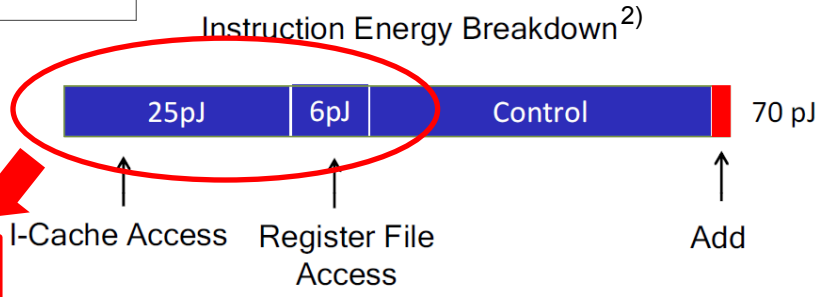
Computation energy efficiency trend [1)]



Communication energy efficiency trend [1)]



Instruction Energy Breakdown [2)]



~30% of energy for communication

[1)] H. Tamura, "Looking to the Future: Projected Requirements for Wireline Communications Technology," IEEE Solid-State Circuits Magazine, Vol. 7, No 4, pp. 53 – 62, 2015.
[2)] M. Horowitz, "Computing's energy problem (and what we can do about it)," IEEE International Solid-State Circuits Conference, pp. 10 – 14, Mar. 2014

Communication in Ubiquitous Computing

The envisioned ubiquitous computing ecosystem[1)]

- **20 pJ/Operation**
- **ADD Op. of two 64-bit operands**
- **30% energy for communication**

- **Total budget: 0.31 pJ/bit**
- **Communication: 0.1 pJ/bit**

[1)]S. Borkar, "Role of Interconnects in the Future of Computing," IEEE Journal of Lightwave Technology, Vol. 31, No. 24, pp. 3927 – 3933, Dec. 2013.

Why wireline on short distances?

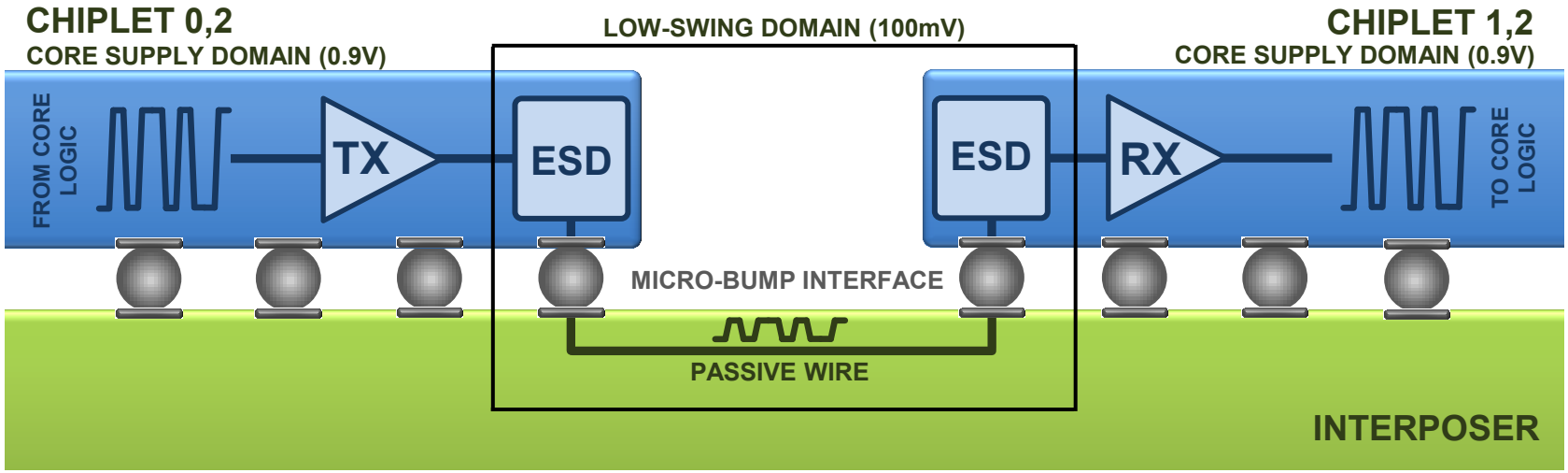
- **Wireless (RF)**
  - Antennas are large for on-chip use
  - Energy efficiency: 55 pJ/bit[1)]
- **Wireless (Optical)**
  - Requires laser
  - Energy efficiency: 1.3 pJ/bit (15 pJ/bit including laser)[2)]
  - Bandwidth density: 300 Gb/s/mm^2
  - Latency: ~100 ns
- **Wireline**
  - Size limited by BEOL rules
  - Latency per 1 mm length: ~7 ps (0.5 c in copper wires with SiO_2 dielectric)
  - Throughput: 10^{16} bit/s (1.25 PB/s, limited by skin effect and dielectric loss)[3)]
  - Bandwidth density: 5 Tb/s/mm^2 (ExaNoDe)
  - Latency: ~1 ns (ExaNoDe)

[1)] T. Tikka, et al., "A 40 GHz wireless link for chip-to-chip communication in 65 nm CMOS," Journal of Analog Integrated Circuits and Signal Processing, Springer, Vol. 83, No. 1, pp. 23-33, Apr. 2015.

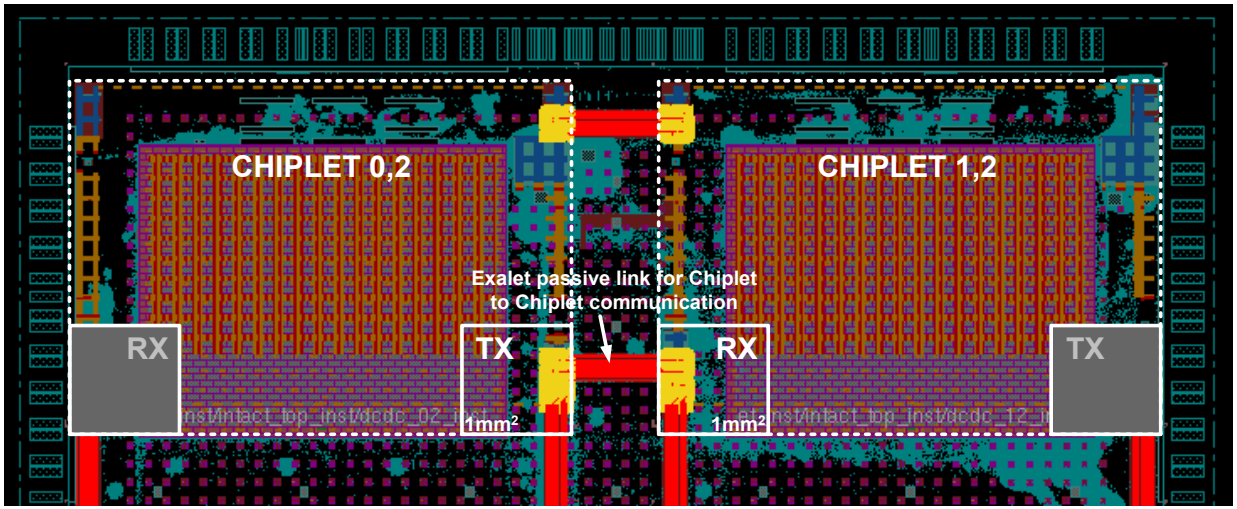
[2)] C. Sun et al., "Single-chip microprocessor that communicates directly using light," Nature, vol. 528, no. 7583, pp. 534–538, 2015

[3)] D. A. B. Miller, H. M. Ozaktas, "Limit to the Bit-Rate Capacity of Electrical Interconnects from the Aspect Ratio of the System Architecture", Elsevier Journal of Parallel and Distributed Computing," Vol. 41. No. 1, pp. 42 – 52, Feb. 1997.

Chip-to-Chip Communication Link in ExaNoDe

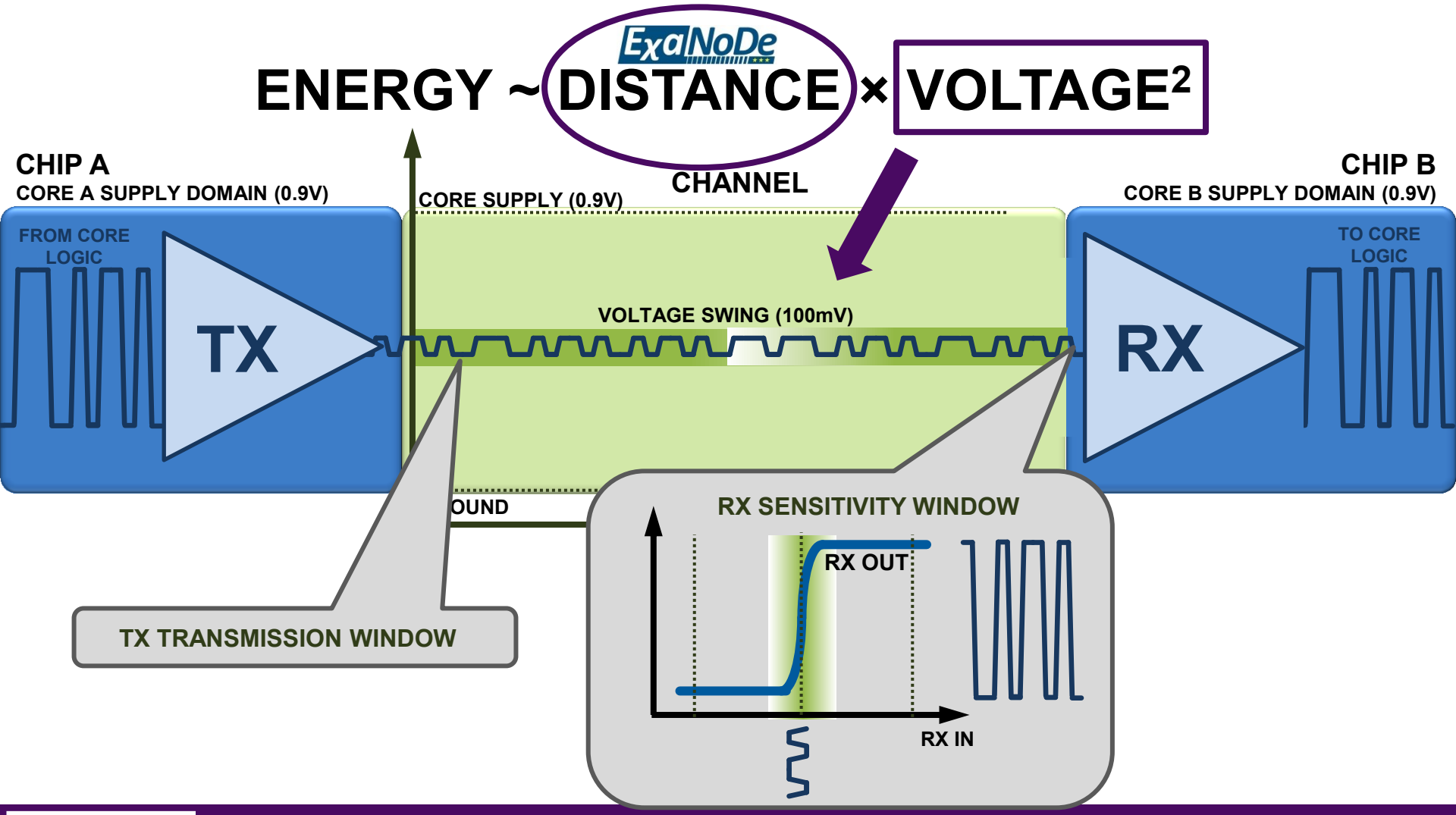


Cross section of the interconnect with single-ended low swing I/O interface

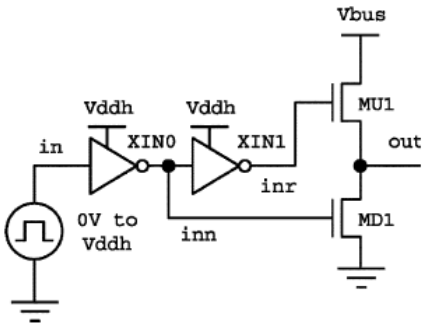


Physical view of the interposer with the projected location of the transceiver and the passive link

Low Swing Signaling Scheme

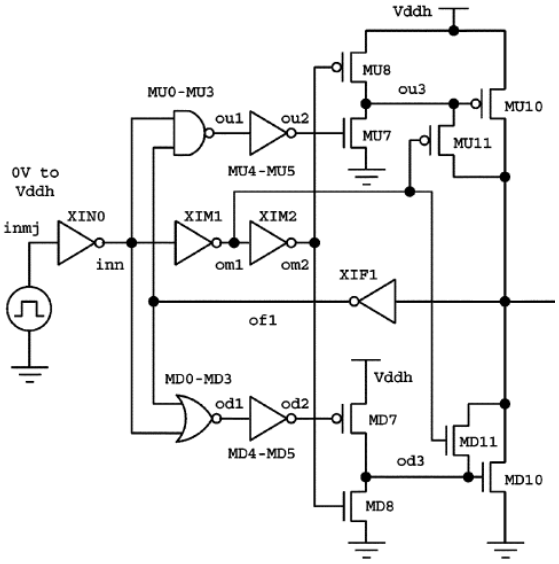


State-of-the-Art Low Swing Transmitters



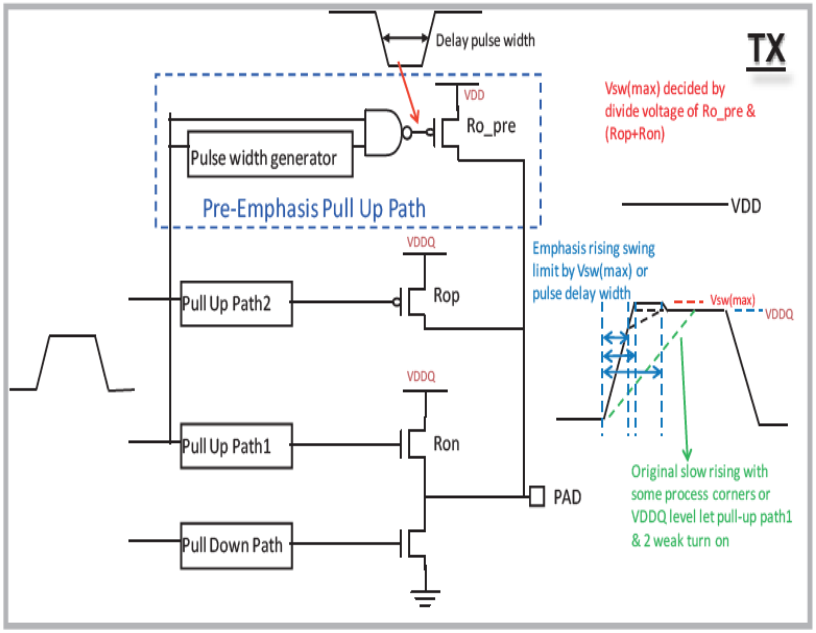
Threshold voltage based asymmetric buffer[1)]

- ✔ Compact design
- ✘ Two voltage domains



Threshold voltage based symmetric buffer[1)]

- ✔ One voltage domain
- ✘ “Large” low swing



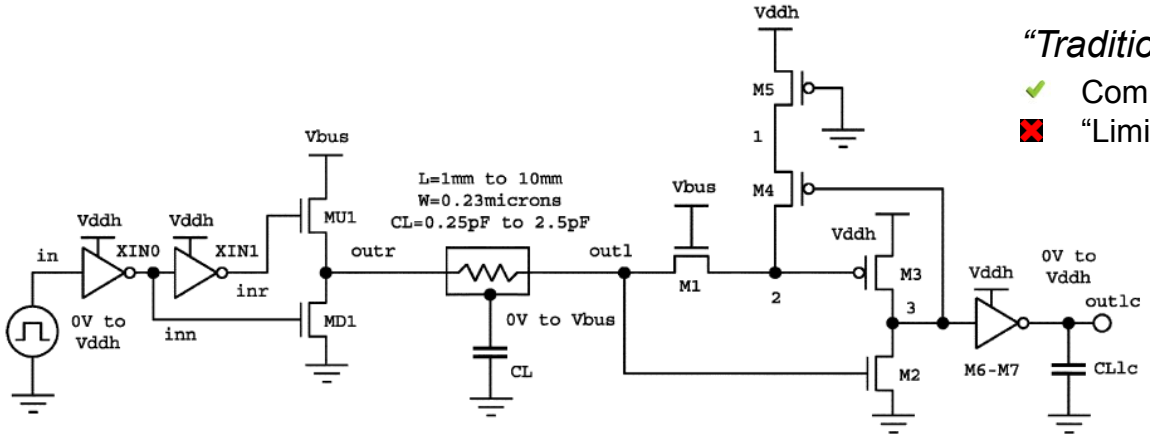
Self-timed delay based buffer[2)]

- ✔ One voltage domain
- ✔ Adjustable output swing
- ✘ Requires bus weak keepers
- ✘ Sensitive to parameter variability

[1)] J. C. Garcia Montesdeoca, “CMOS Driver-Receiver Pair for Low-Swing Signalling for Low-Energy On-Chip Interconnects,” IEEE Transactions on VLSI Systems, Vol. 17, No. 2. Feb 2009

[2)] M. S. Lin, et al., “An extra low-power 1Tbit/s bandwidth PLL/DLL-less eDRAM PHY using 0.3V low-swing IO for 2.5D CoWoS application,” IEEE Symposium on VLSI Technology, Jun. 2013

State-of-the-Art Low Swing Receivers

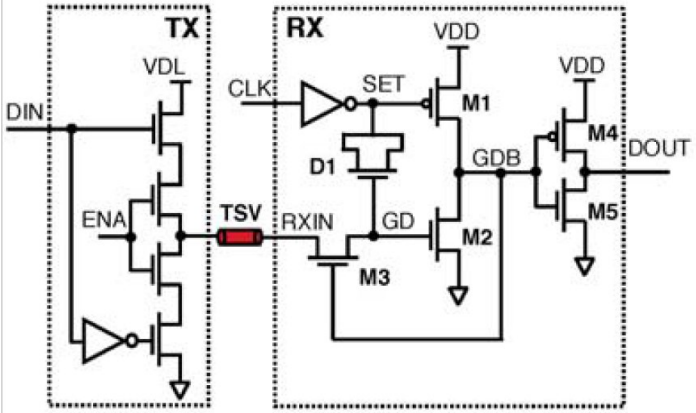


"Traditional" level shifter[1)]

- ✔ Compact design
- ✘ "Limited" low swing (min V_{TH} of M2)

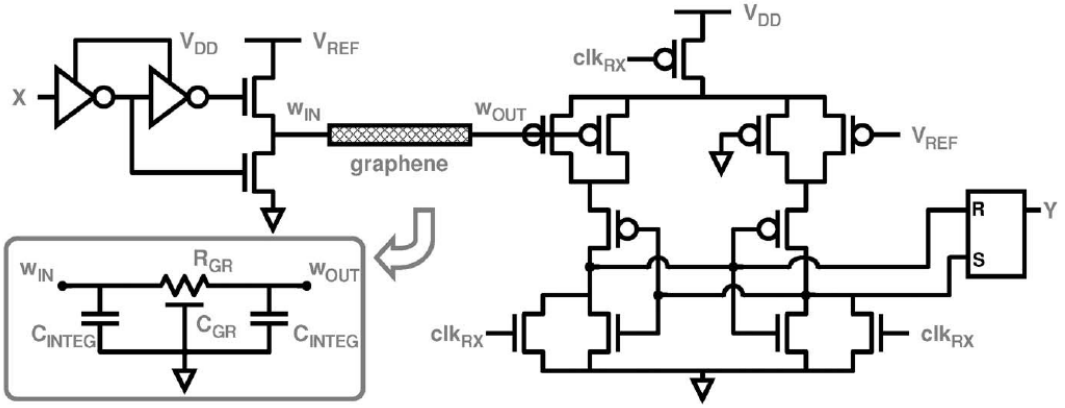
Comparator-based RX[3)]

- ✔ Differential operation
- ✔ High sensitivity and speed
- ✘ Requires clock and reference



Diode-gated sense amplifier shifter[2)]

- ✔ Compact design
- ✘ Requires precise clock alignment
- ✘ Sensitive to parameter variability

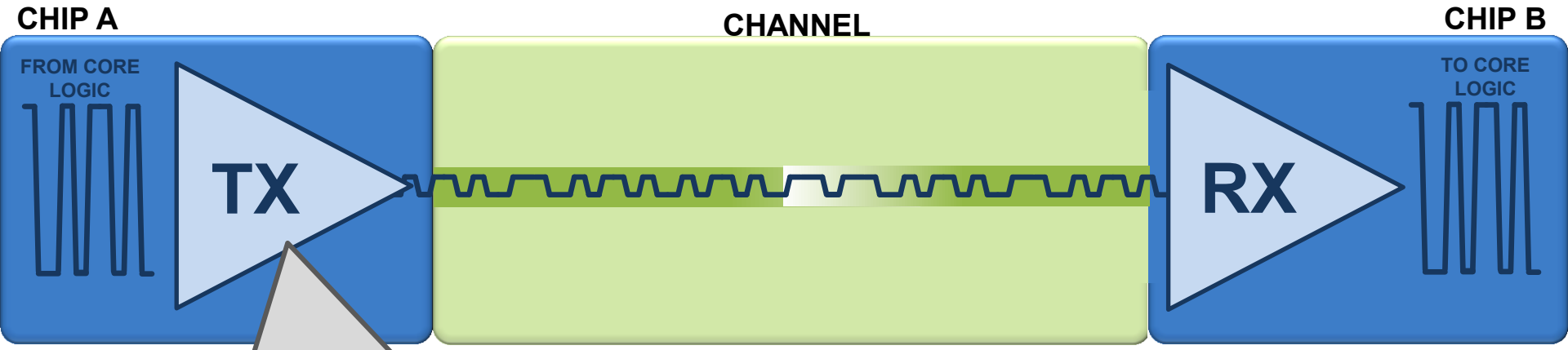


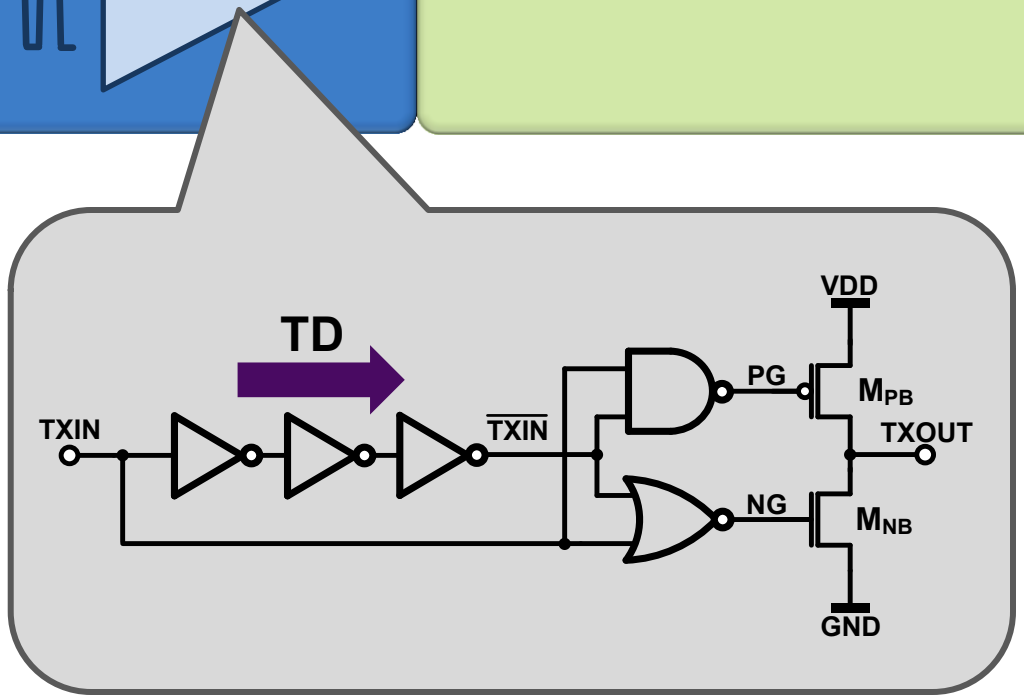
[1)] J. C. Garcia Montesdeoca, "CMOS Driver-Receiver Pair for Low-Swing Signalling for Low-Energy On-Chip Interconnects," IEEE Transactions on VLSI Systems, Vol. 17, No. 2. Feb 2009

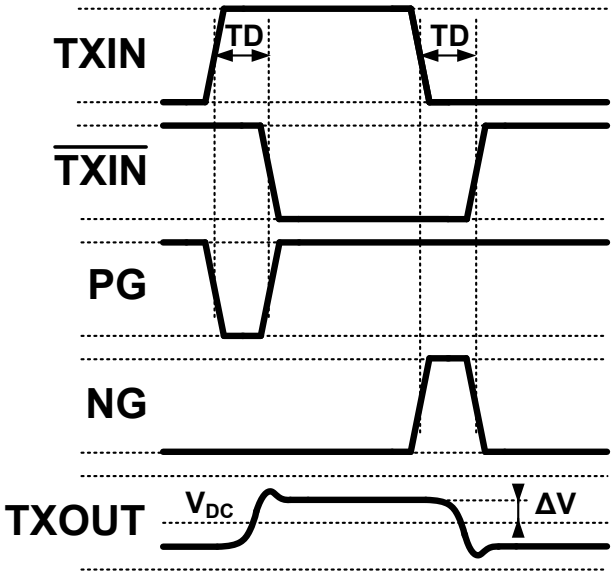
[2)] Y. Liu, et al., "A Compact Low Power 3D I/O in 45nm CMOS," ISSCC 2012

[3)] K. J. Lee, et al., "Low-Swing Signaling on Monolithically Integrated Global Graphene Interconnects," IEEE Transactions o n Electron Devices, Vol. 57, No.12, Dec. 2010

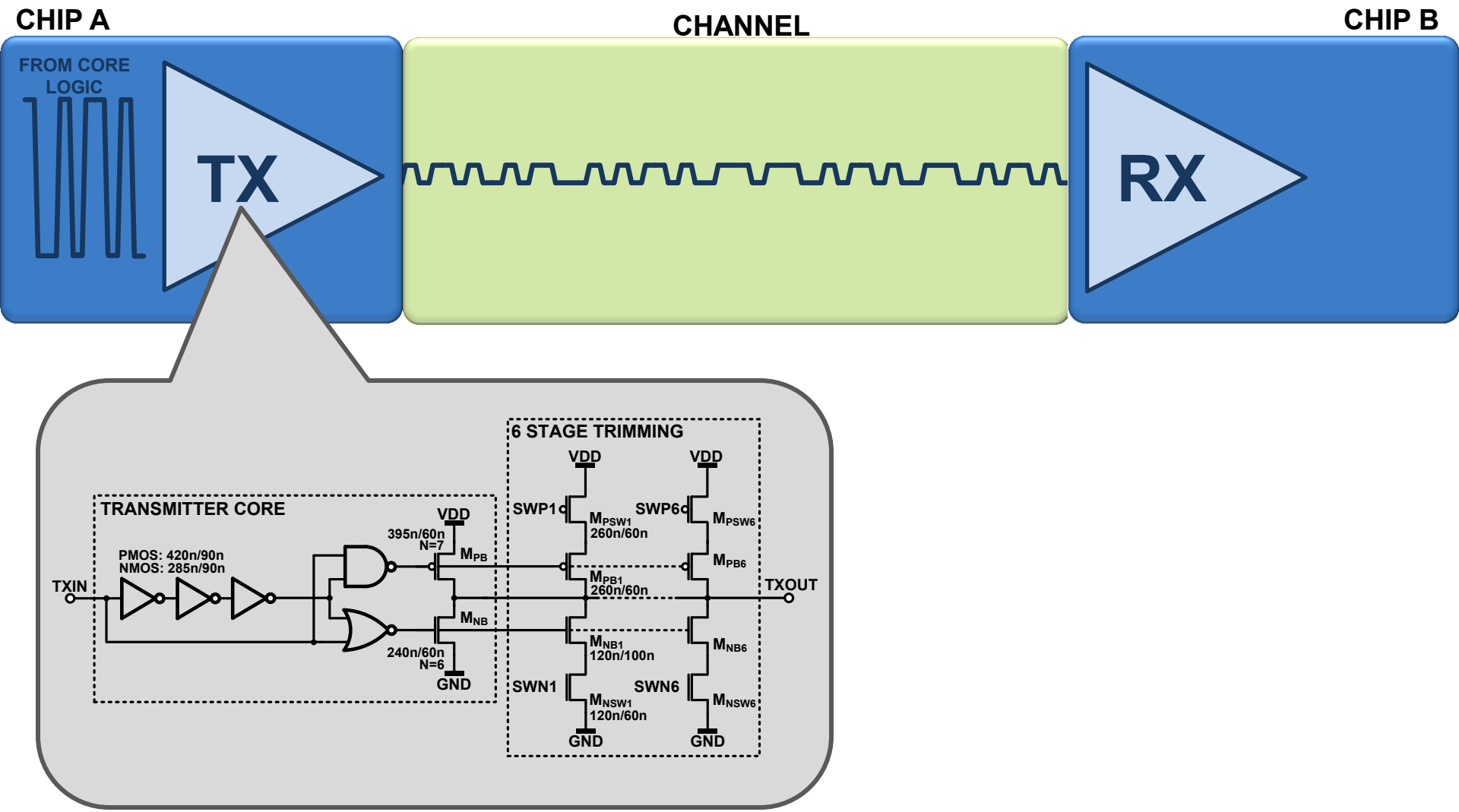
Proposed Low Swing Transmitter



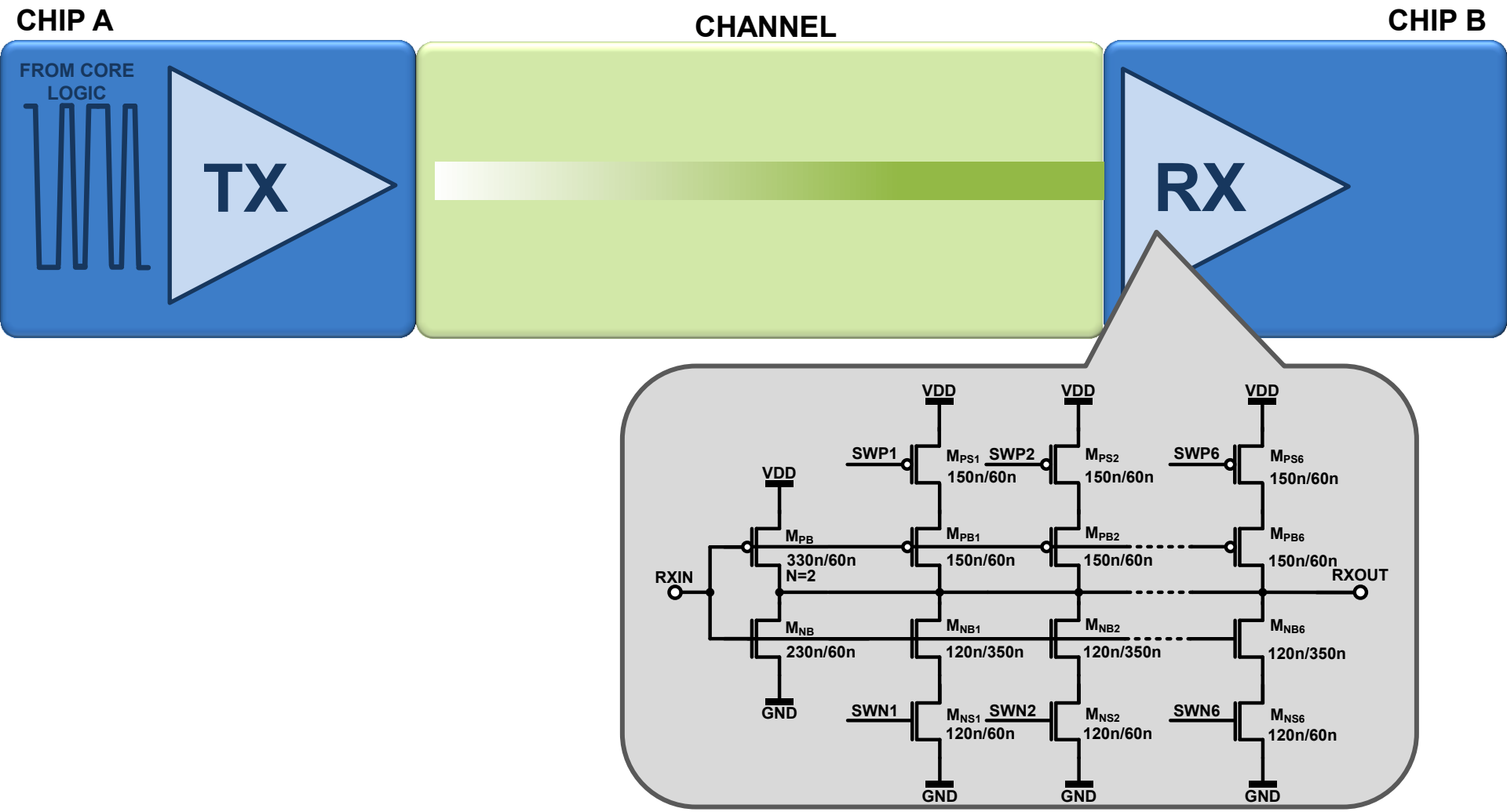




Variability Compensation in TX

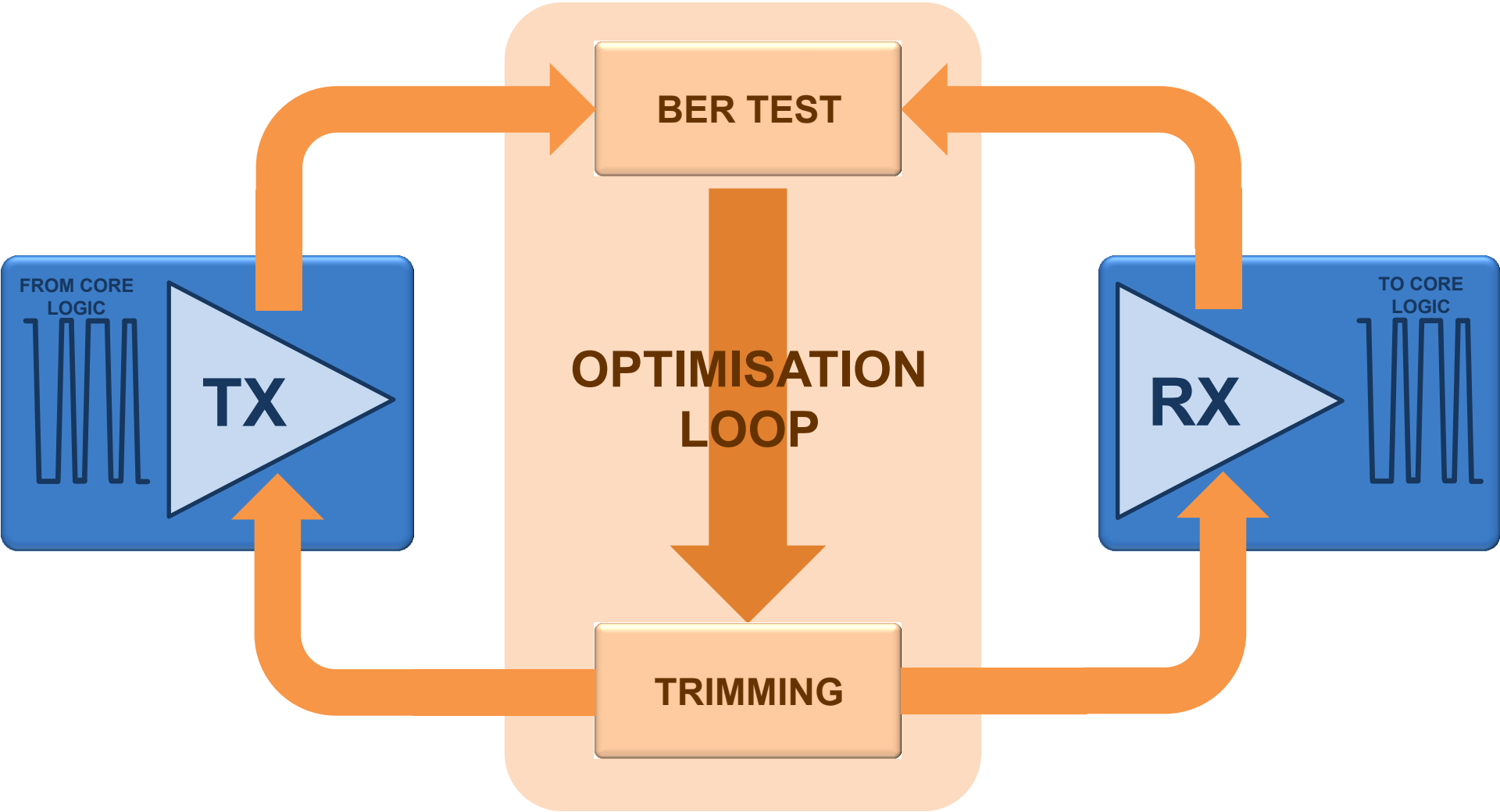


Variability compensation in RX

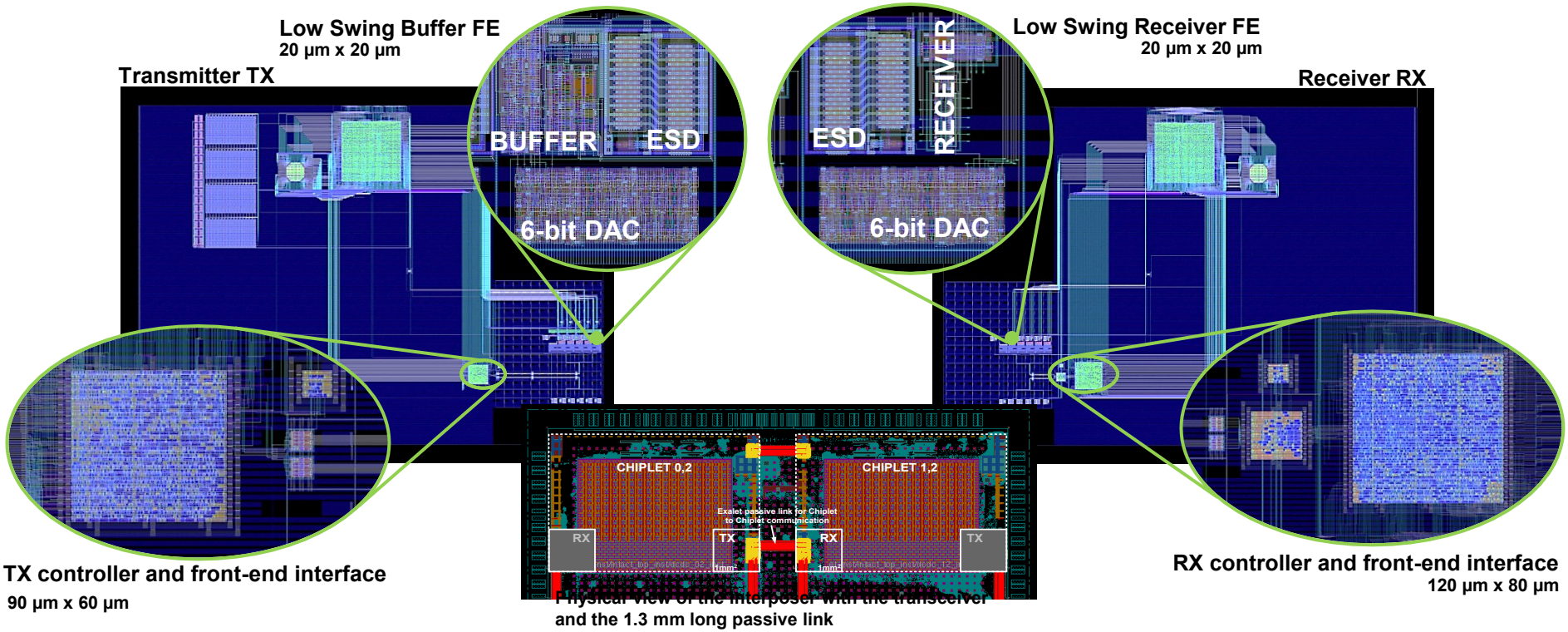


P. Mroszczyk, V. Pavlidis, "Mismatch Compensation Technique for Inverter-Based CMOS Circuits", presentation on ISCAS 2018

Transceiver Trimming



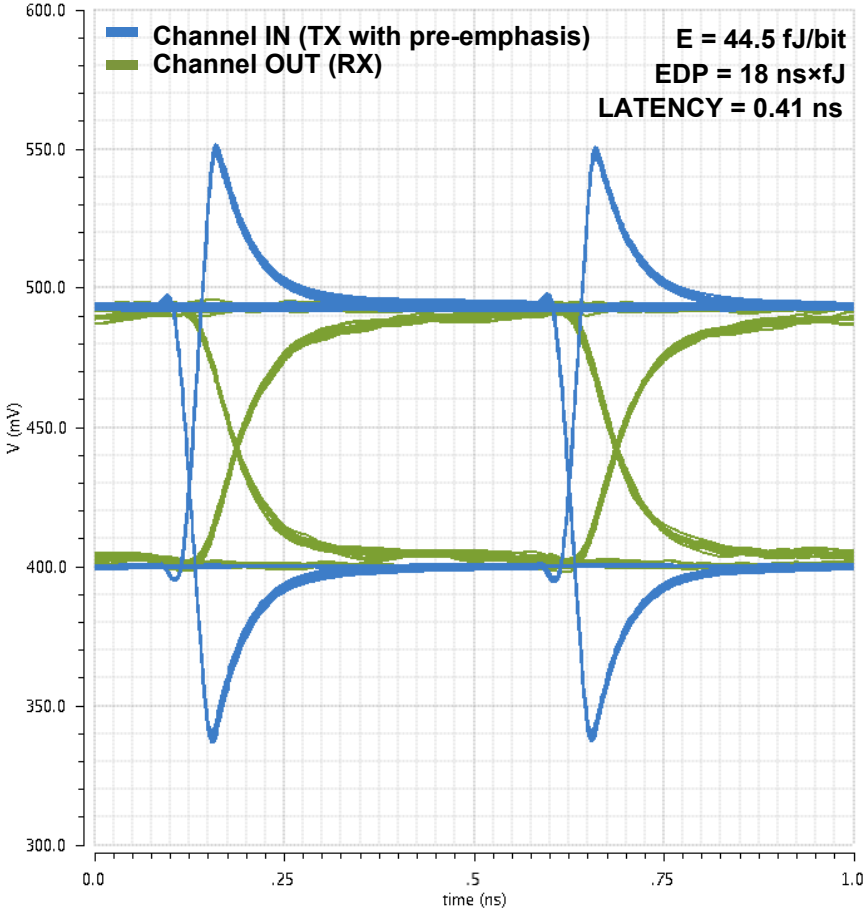
EMI v1.0 Transceiver in 28nm FDSOI

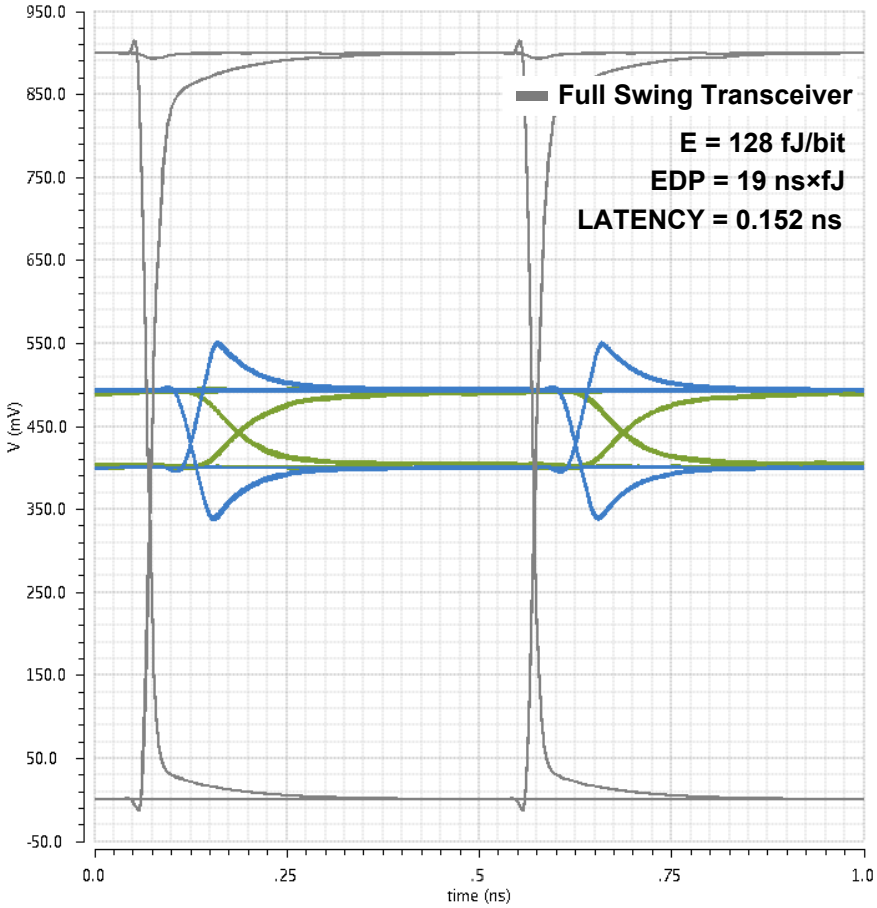


- **Exascale Manchester Interconnect (EMI) v1.0:**
  - Energy: **44.5 fJ/bit**, Speed: **2 Gb/s/wire** (SDR), bandwidth: **256 Gb/s** (128-wire link), **5 Tb/s/mm²**
  - Advanced body biasing scheme for parameter variability trimming
  - Up to **3× less power consumption** compared to a standard full swing solution (< 0.1 pJ/bit)
  - Over **5× less switching noise** compared to a standard full swing solution
  - Latency: 2 clock cycles from TX to RX (0.41 ns for level conversion and signal propagation)

EMI v1.0 Transceiver in 28nm FDSOI

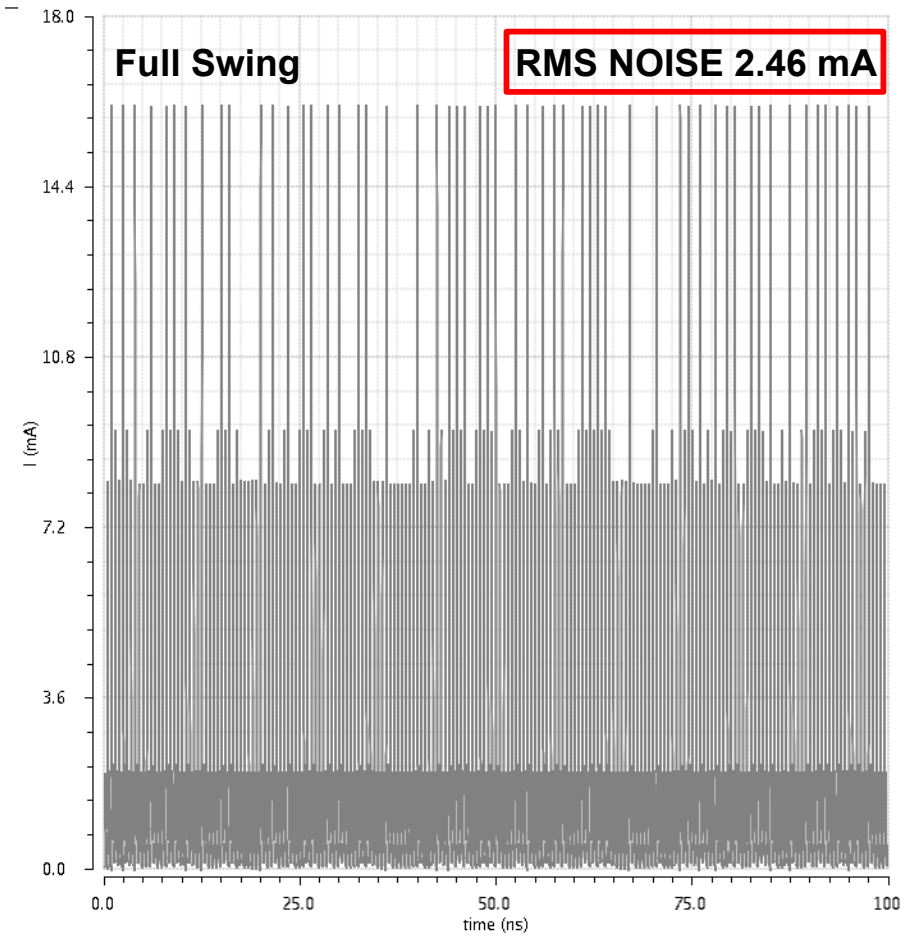
1-bit line @ 2 Gb/s (clock shielding) – EYE DIAGRAM

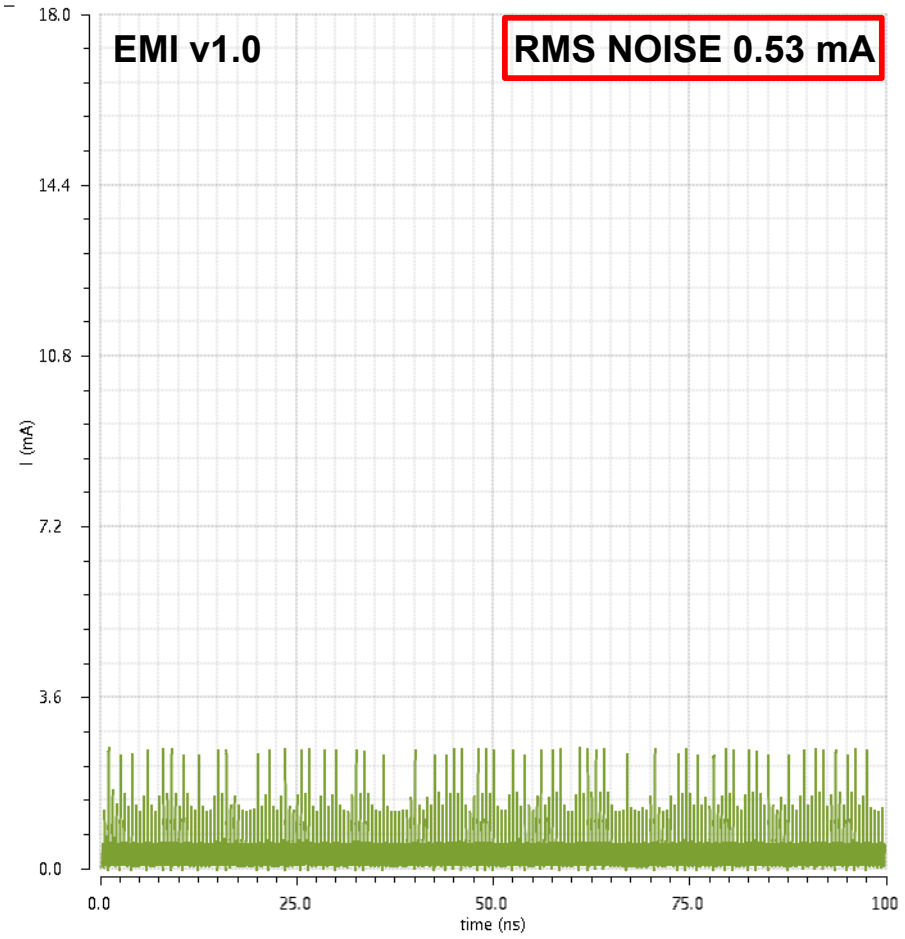




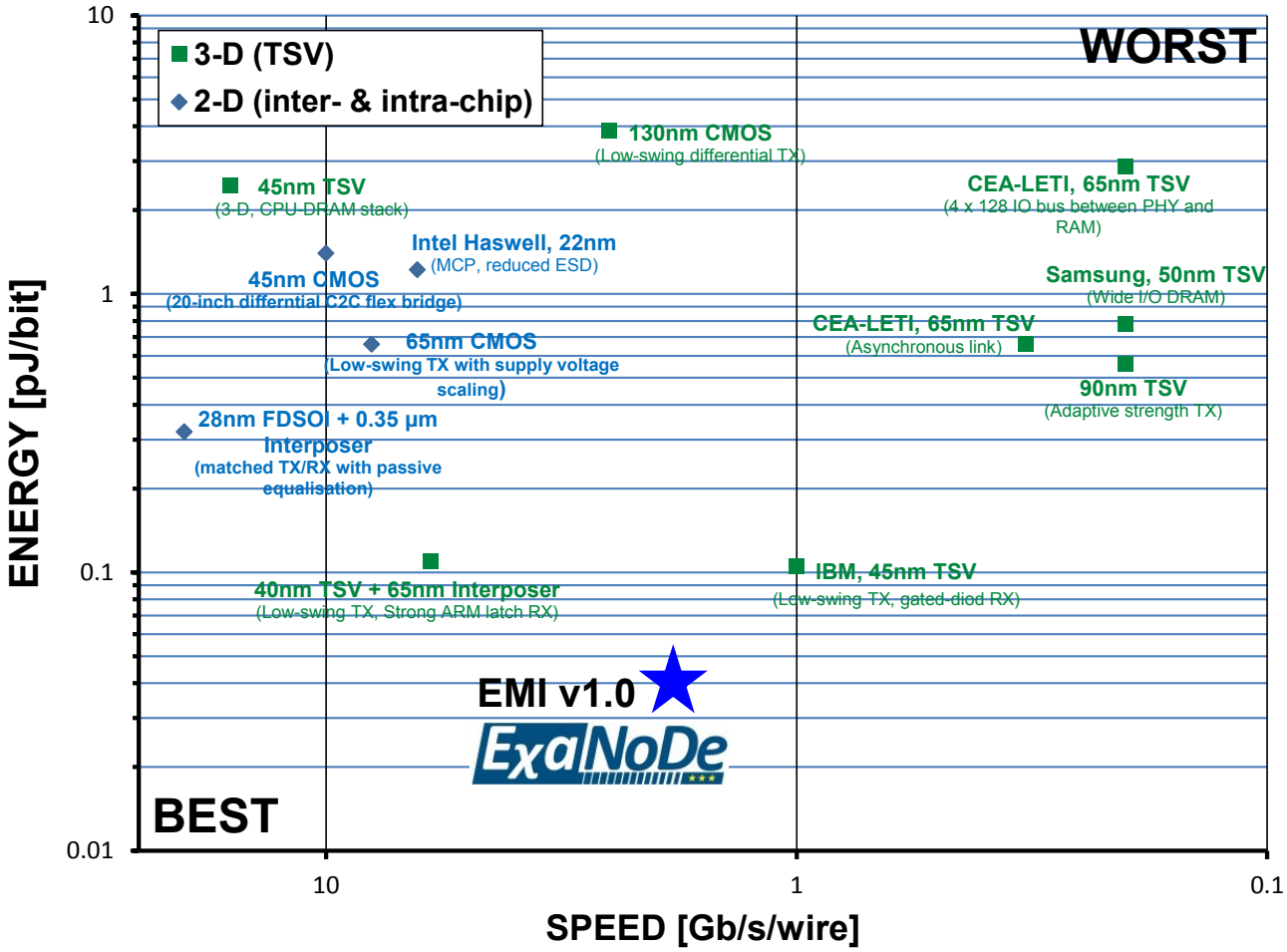
EMI v1.0 Transceiver in 28nm FDSOI

1-bit line @ 2 Gb/s (clock shielding) – SWITCHING NOISE

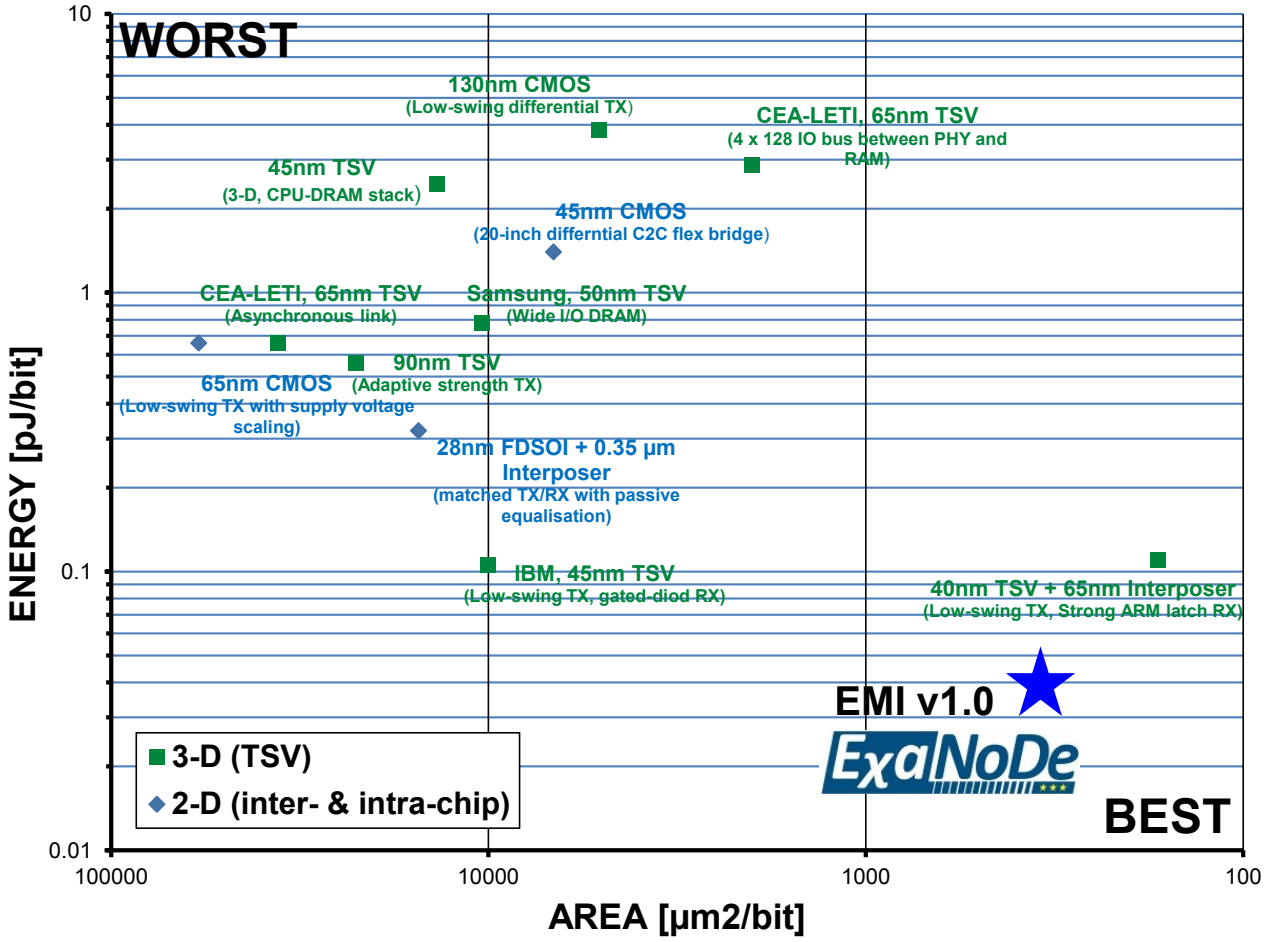




Energy vs Speed



Energy vs Area



Summary

- **The challenge is to reduce energy below 0.1 pJ/bit across an SoC**
- **Wireline communication offers high efficiency, high speed, reliability and security**
- **Looking for improvements on the physical layer (ExaNoDe)**
  - Low swing signalling
  - Hardware trimming and training
- **Looking for improvements on the transport layer (EuroEXA)**
  - Reordering encoding
  - Error correction
  - Multi-level encoding