3D sequential integration : review of opportunities and technology updates

P. Batude, L. Brunet, C. Fenouillet-Beranger, F. Andrieu, J-P. Colinge, D. Lattard, E. Vianello, S. Thuries, O. Billoint, P. Vivet, C. Santos, B. Mathieu, B. Sklenard, C.-M. V. Lu, J. Micout, F. Deprat, E. Avelar Mercado, F. Ponthenier, N. Rambal, M.-P. Samson, M. Cassé, S. Hentz, J. Arcamone, G. Sicard, L. Hutin, L. Pasini, A. Ayres, O. Rozeau, R. Berthelon, F. Nemouchi, P. Rodriguez, J-B. Pin, D. Larmagnac, A. Duboust, V. Ripoche, S. Barraud, N . Allout, S. Barnola, C. Vizioz, J.-M. Hartmann, S. Kerdiles, P. Acosta Alba, S. Beaurepaire, V. Beugin, F. Fournel, P. Besson, V. Loup, R. Gassilloud, F. Martin, X. Garros, F. Mazen, B. Previtali , C.Euvrard-Colnat, V. Balan , C. Comboroure, M. Zussy, Mazzocchi, O. Faynot and M. Vinet

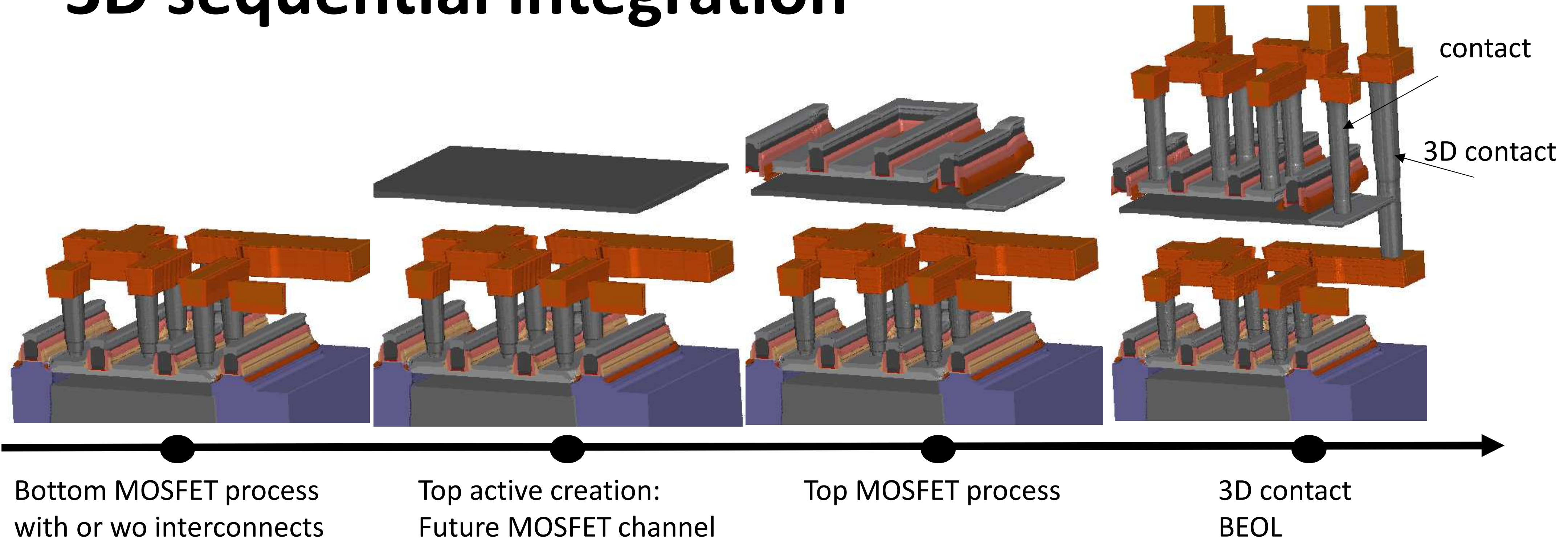
Outline

3D sequential characteristics

3D sequential opportunities

Process integration

3D sequential integration



3D sequential integration

contact

3D contact

Bottom MOSFET process
with or wo interconnects

Top active creation:
Future MOSFET channel

Top MOSFET process

3D contact
BEOL

Also named 3D monolithic
3D VLSI

THERMAL BUDGET CONSTRAINTS

… CoolCube™

3D sequential integration

contact

3D contact

Bottom MOSFET process
with or wo interconnects

Top active creation:
Future MOSFET channel

Top MOSFET process

3D contact
BEOL

Lithography alignment

e.g: 28nm node: 3σ<5nm

3D sequential integration

contact

3D contact

Bottom MOSFET process
with or wo interconnects

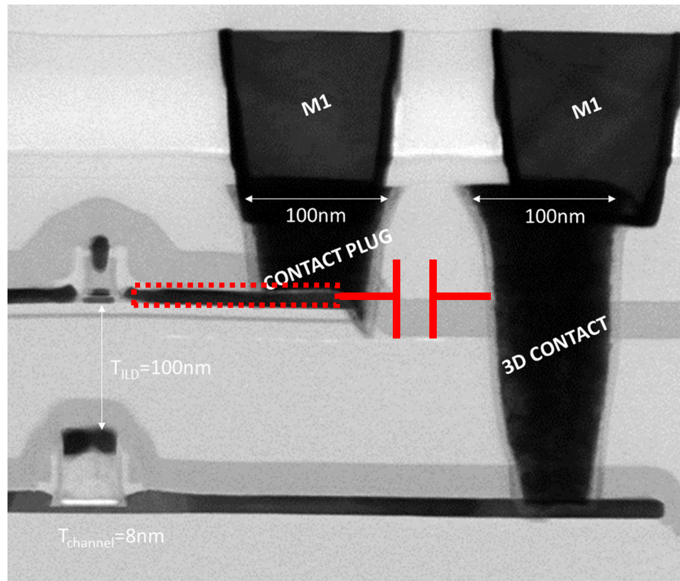
Top active creation:
Future MOSFET channel

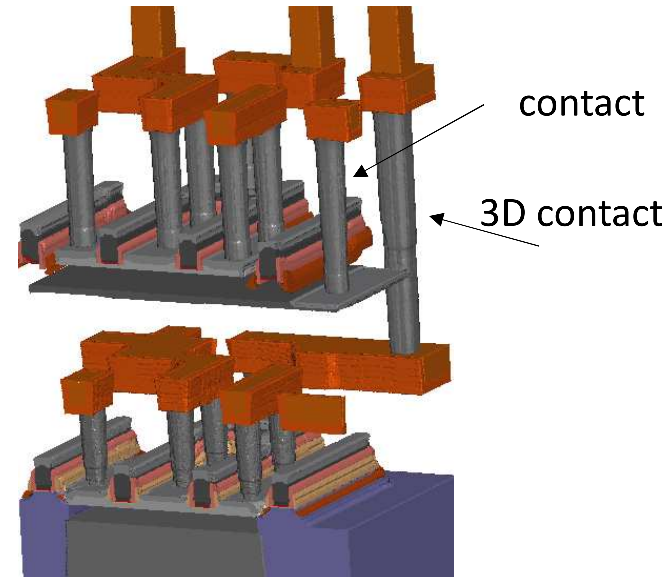
Top MOSFET process

3D contact
BEOL

3D contact = W plug
3D Contact scales with the device technology
e.g: 28nm node: ~40nm

3D sequential integration





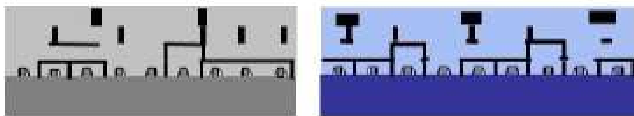
Thin active layer (10 to 100nm)
→ Small 3D via Aspect Ratio
→ Small Parasitic C

Sequential ≠ Packaging integration

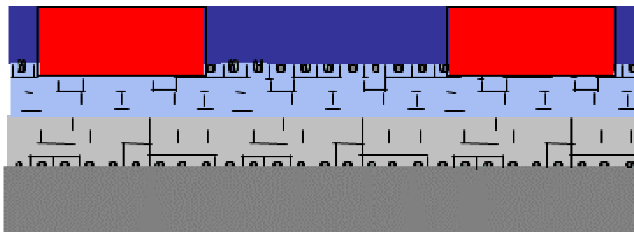
Packaging integration

(e.g.: TSV, copper to copper bonding..)

1/ Wafers processed separately

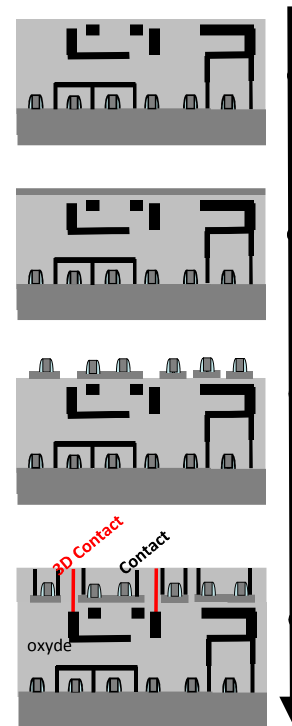


2/ Stacking and contacting



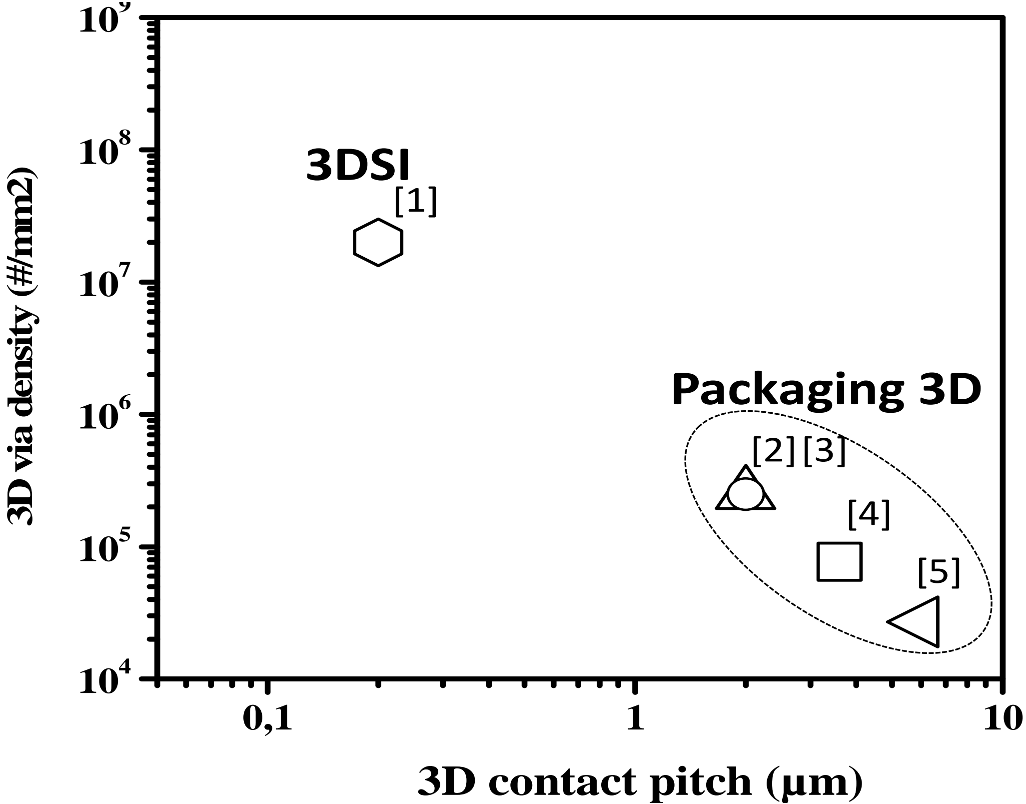
Alignment made during bonding
3σ min = 250nm

Sequential integration



Alignment by lithography
3σ = 5nm (28nm stepper)

3D contact density



$2x10^7$ via/mm^2 demonstrated [1]

Reachable 3D via pitch @ 14 nm node =80nm

[1]: L. Brunet et al., VLSI 2016, [2] I. Sugaya et al., ASMC 2015, [3] J. De Vos, 3DIC 2016 [4] L. Peng et al., EPTC 2016 [5] D. Zhang et al. TSM 2015

Outline

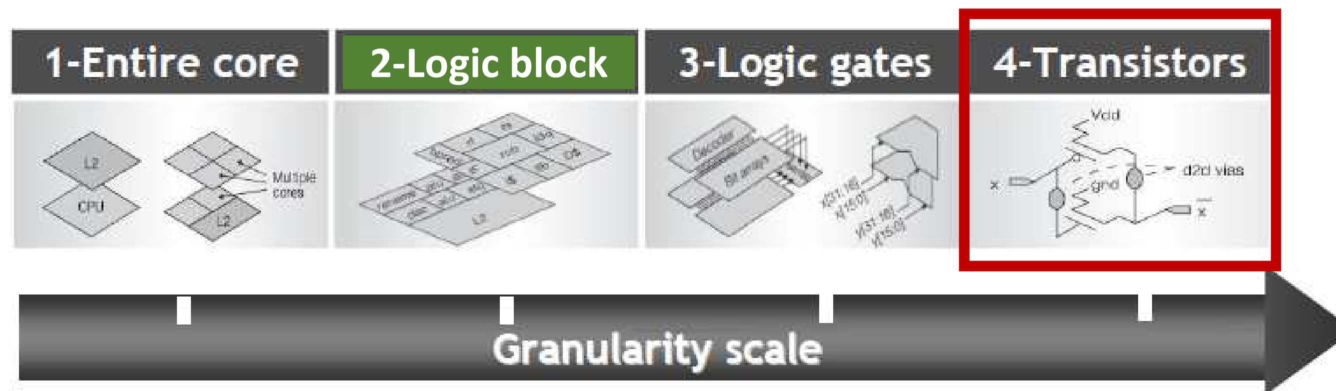
Computing applications

Alternative computing architecture

Sensor interface (More than Moore)

Overall goal:
describe technology requirements for specific applications

Computing applications: Boosting the FET performance

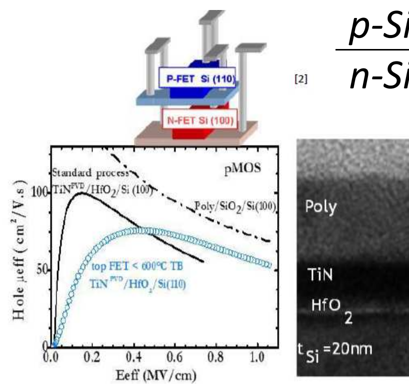


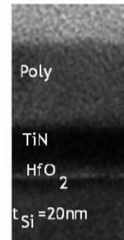
3D sequential offers the N & PFET stacking opportunity

N/P stack: the integration engineer's holy grail

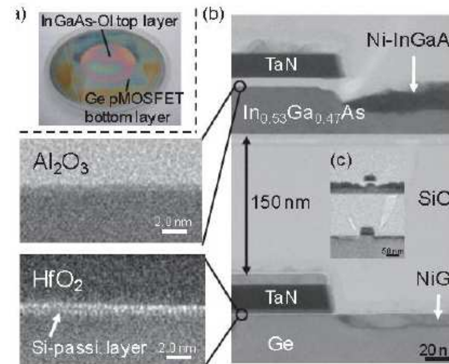
If for each FET polarity, one were to pick the best possible:

- Channel material
- Gate stack
- Stressors
- Contact metallurgy
- Surface orientation
- Device Architecture

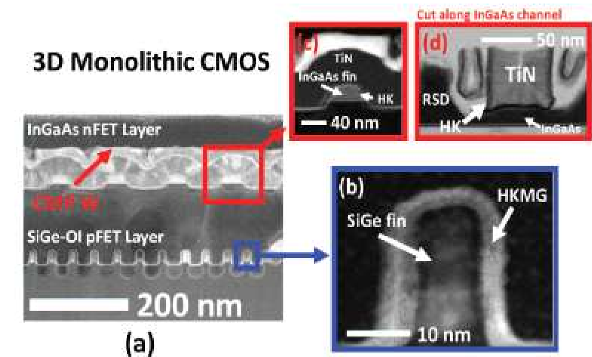




p-Si(110) / *n-Si(100)*



n-III-V / *p-Ge*



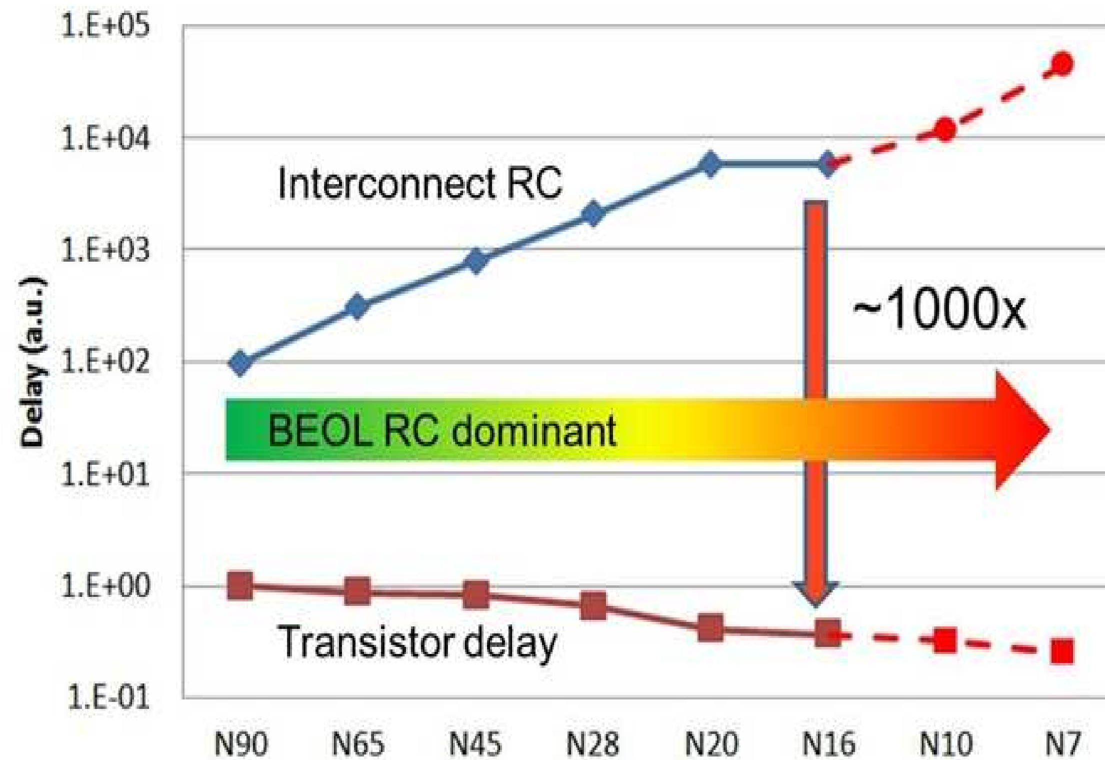
...then 3D sequential spares numerous litho steps and process selectivity challenges vs. co-planar

P. Batude *et al.*, IEDM 2009 (Leti)

T. Irisawa *et al.*, VLSI 2014 (AIST)

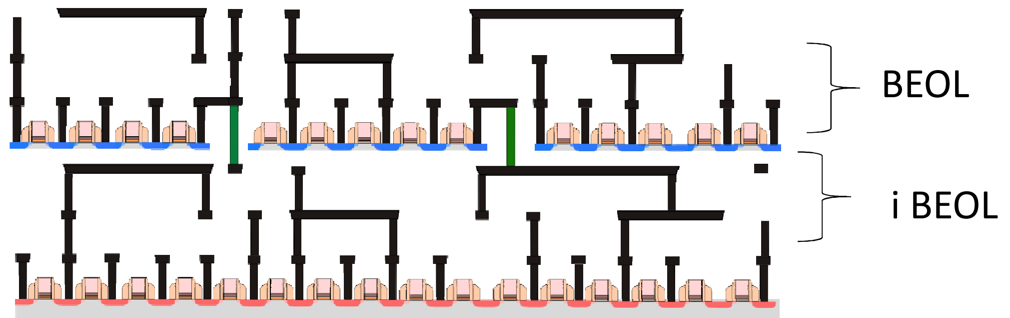
V. Deshpande *et al.*, IEDM 2015 (IBM)

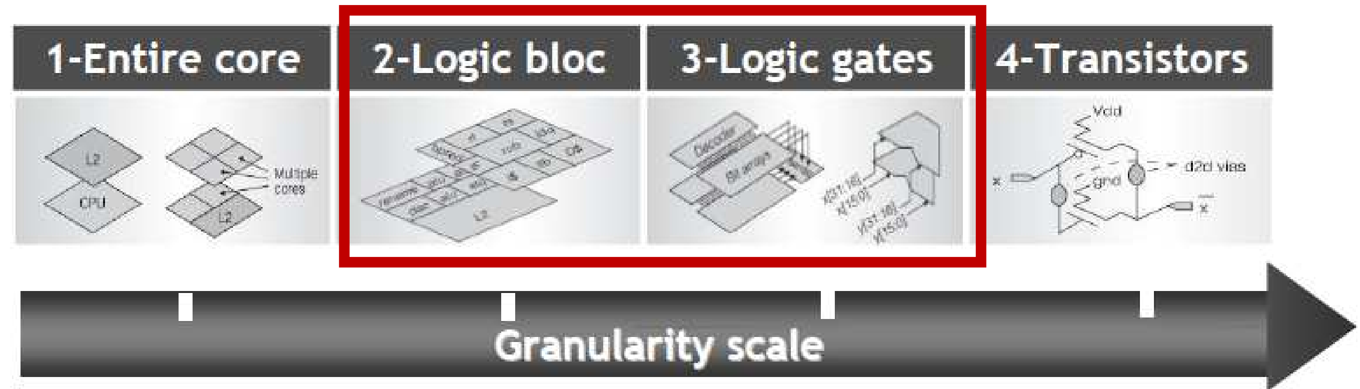
Interconnect delay supression: the designers' holy grail



Extracted from Geoffrey Yeap, Qualcomm's VP of technology IEDM 2013

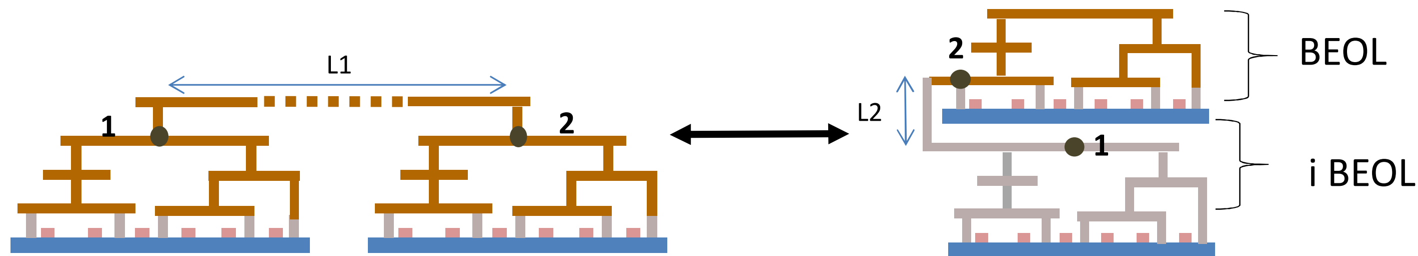
Interconnection delay →logic blocks and gate scale





IC gain performance by wirelength reduction
CMOS/ CMOS stacking

Gain in interconnection delay → CMOS/ CMOS stacking



- **Depends on the technology node**
- **Depends on the application**
- **Requires dedicated 3D P&R tools [1,2]**

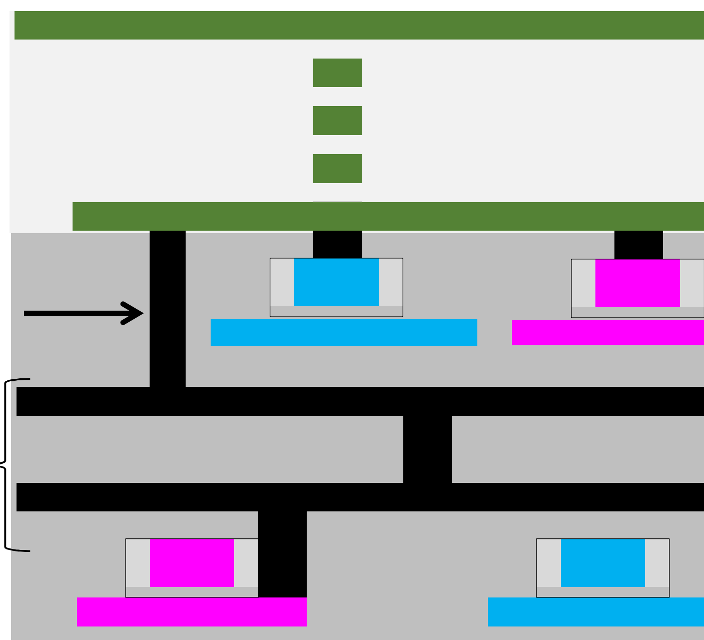
[1] K. Arabi et al., ISPD 2015 [2] O. Billoint et al., ISPD 2015

Full custom design: FPGA application

Stacking of 14nm FDSOI

CoolCube DKIT:

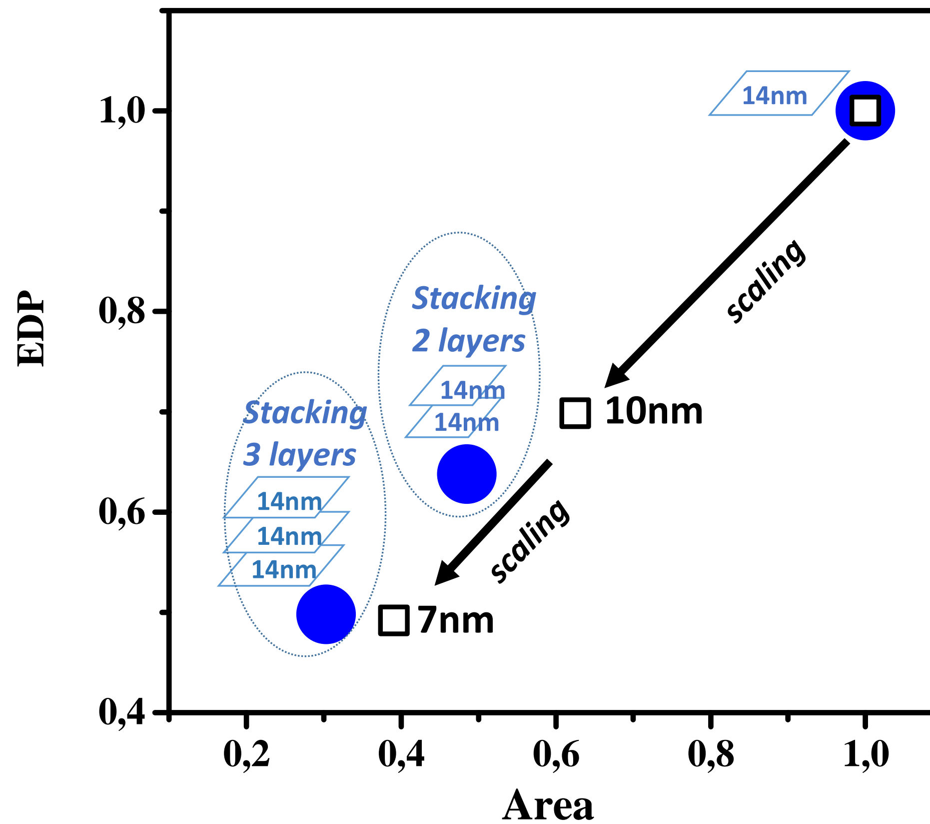
- Top BEOL (Cu & low-k) M1 to Mx
- 3D Contact (Pitch 80nm)
- Int. BEOL (W & SiO_2) M1i to M3i



Partitioning:

- Top level: Logic
- Bottom level: SRAM memory

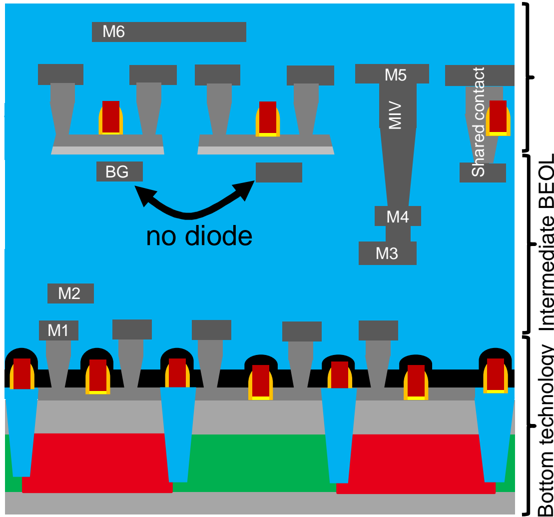
Full custom design: FPGA application



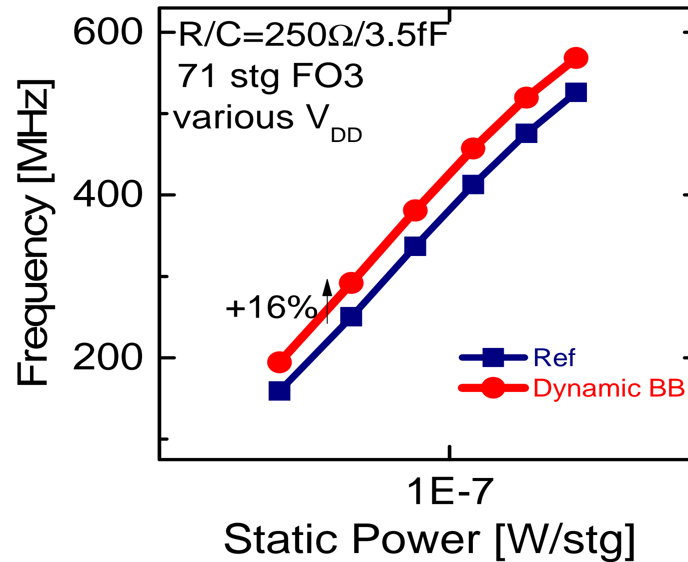
Stacking is more efficient than scaling the MOSFET

O. Turkyilmaz et al., DATE 2014 [2]: ITRS 2013, “System driver summary” [3]: ITRS 2013, “ORTC”

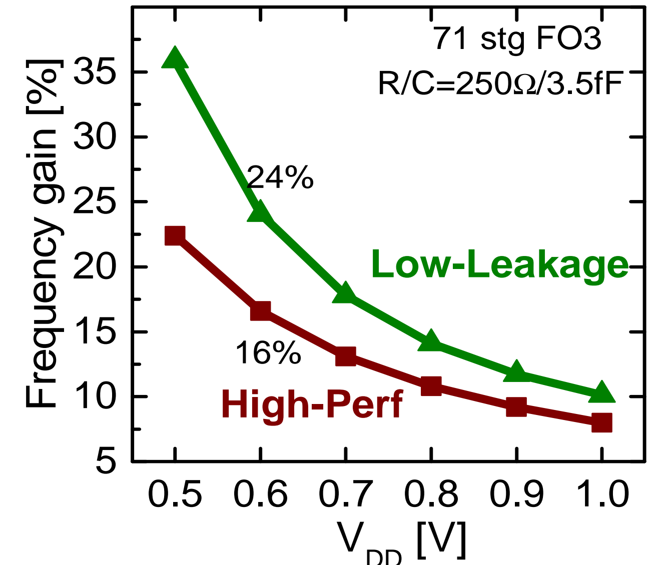
The ultimate technology for back-bias



Asymetric double gate
Low parasitic with local BG



+16% frequency gain at the same static power



Up to +36% freq. for low-leakage cells (high-V_T) and low-V_{DD}

F Andrieu, IEDM 2017

Outline

Computing applications:

Motivation for 3D sequential

technology implications

Alternative computing architectures

Sensor interface (More than Moore)

Overall goal:

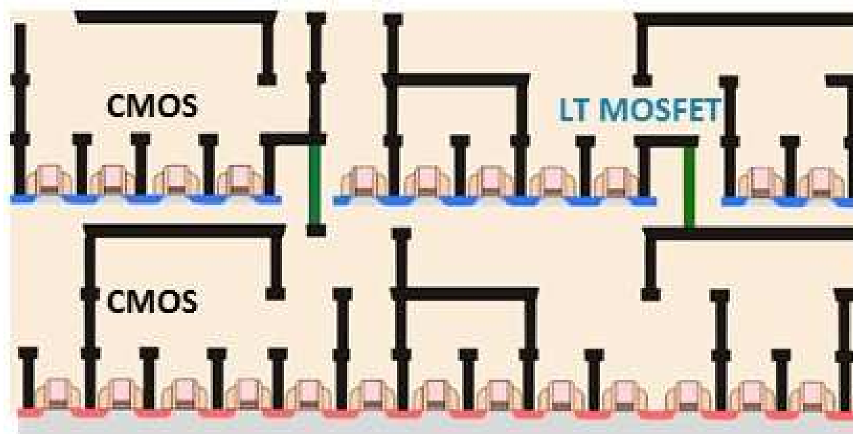
describe technology requirements for specific applications

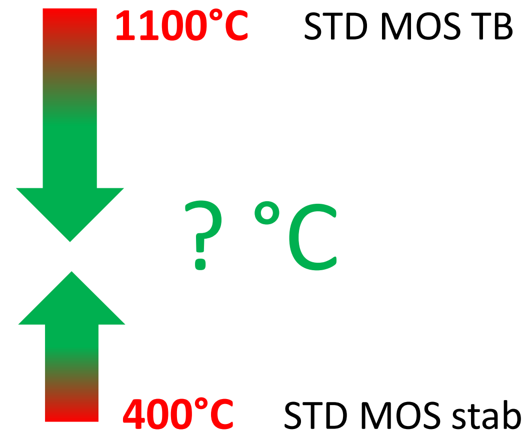
Technology for computing application

- CMOS on top and bottom levels
- Si based technology
- Intermediate BEOL
- 100% performance for top and bottom MOS

A - Bottom tier: what maximum thermal budget to keep perf at 100%?

B- Top tier: How achieving LT Top FET with 100% perf?

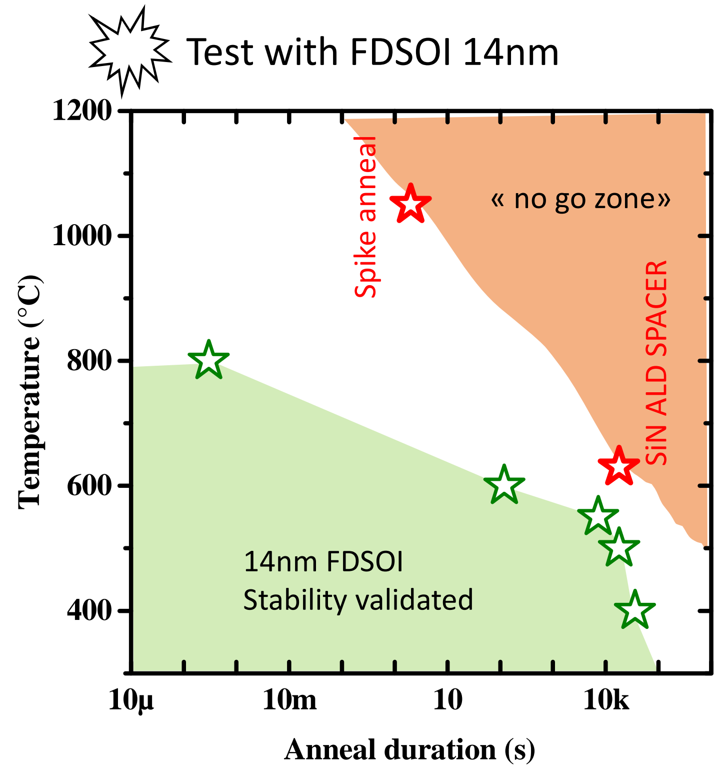




Bottom MOSFET stability

Interconnection stability

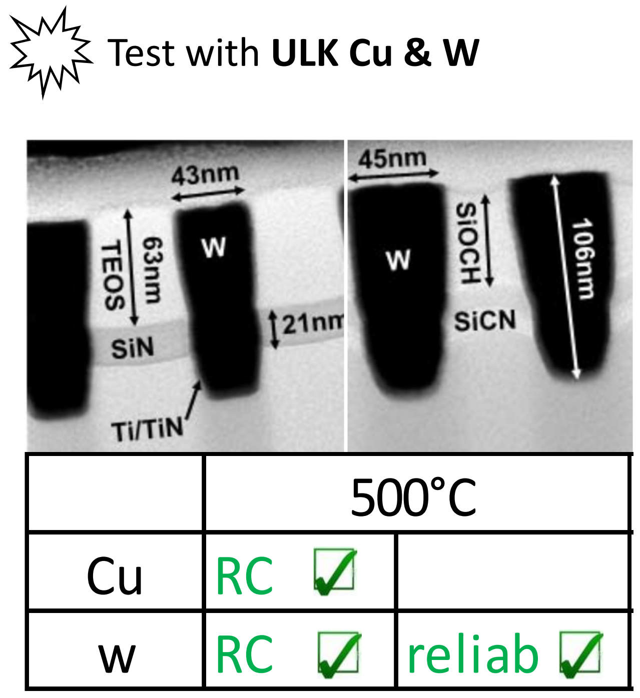
Test with FDSOI 14nm



Bottom MOSFET thermal budget PW
Will be summarized as «500°C 5h»

[1]: P. Batude et al., VLSI 2015

Test with **ULK Cu & W**



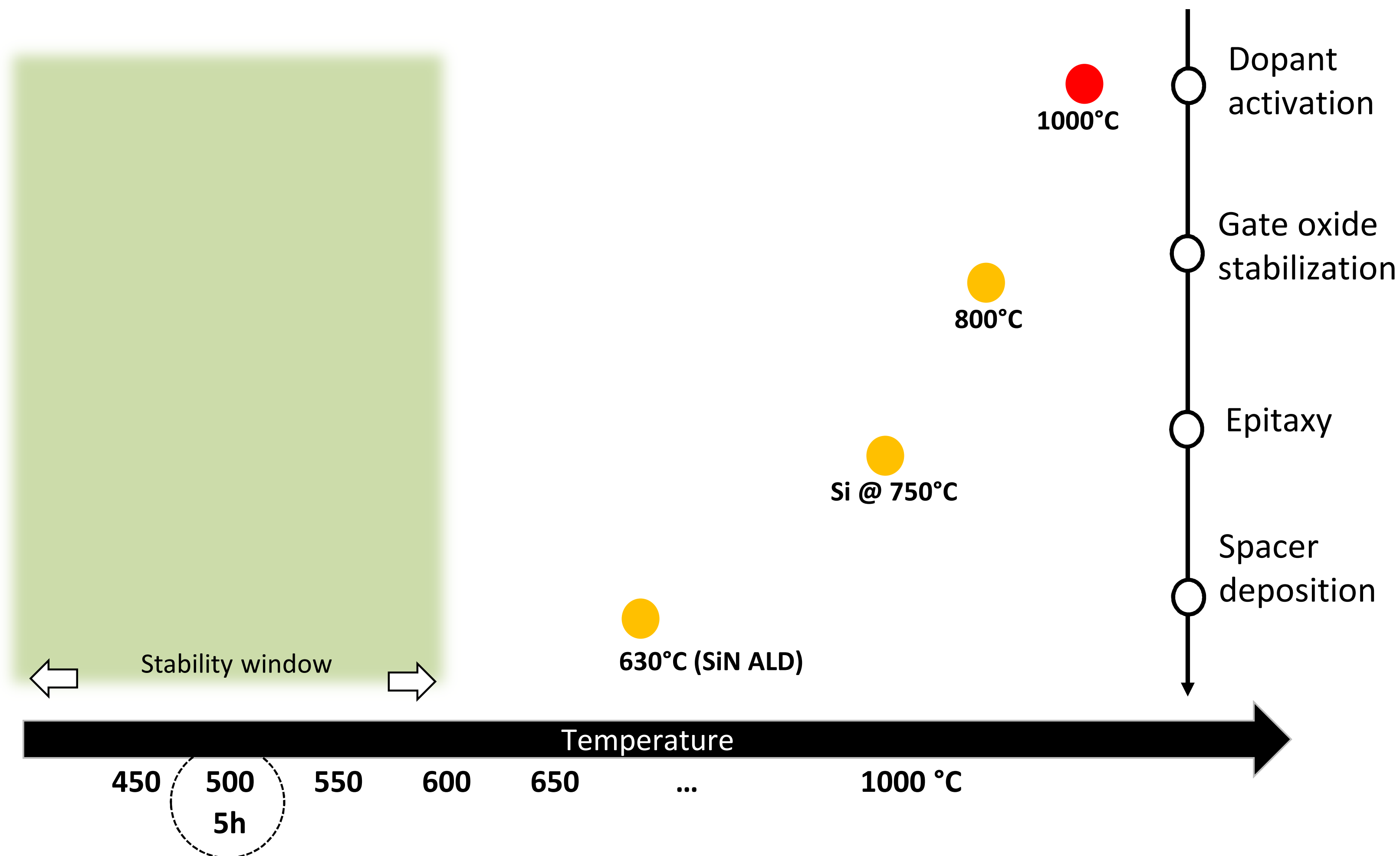
	500°C	
Cu	RC ✓	
W	RC ✓	reliab ✓

ULK is stable up to 500°C 2h

RC stability validated for Cu at 500°C 2h

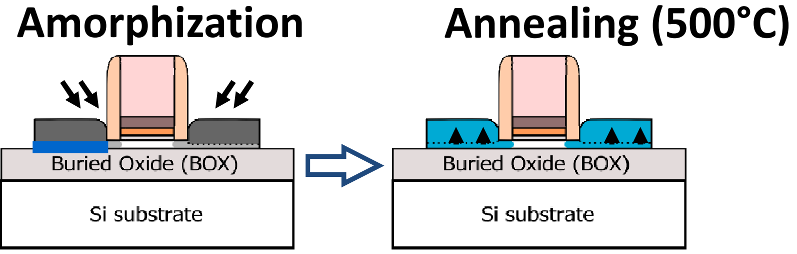
[1] C. Fenouillet-Beranger et al., *SSDM 2015,*
[2]: V. Lu et al., VLSI 2017

Top tier: towards a 500°C HP CMOS integration

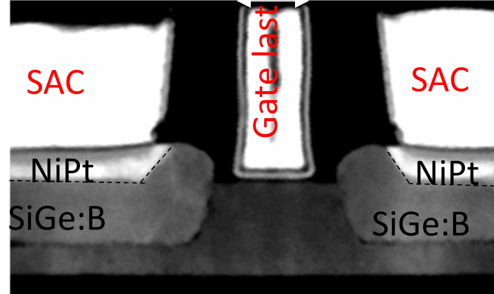


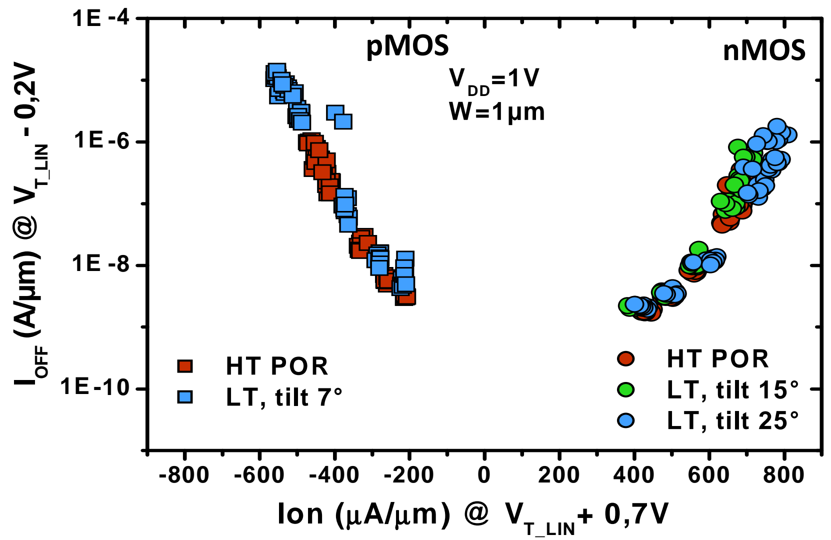
Rmk: * For 14 nm FDSOI and ULK interconnections

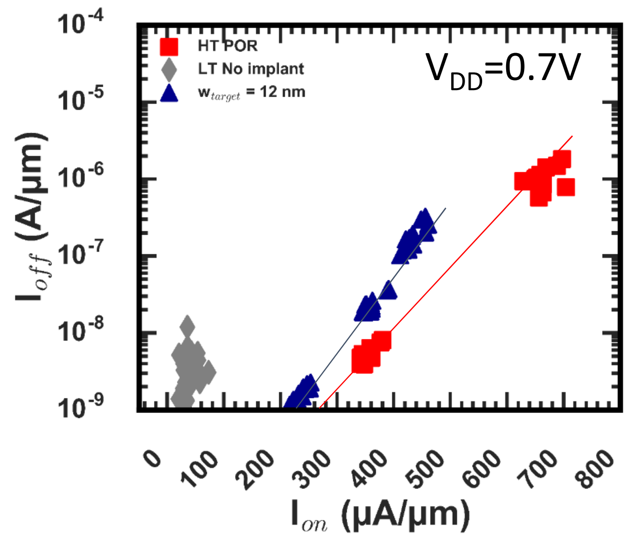
Low temperature junctions



SPER activation







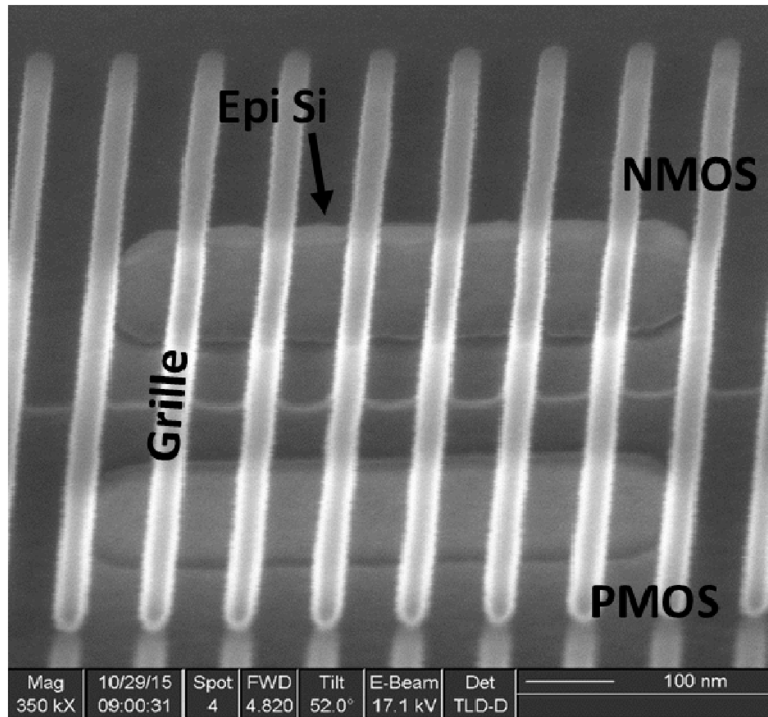
Low-temp. 28nm FDSOI

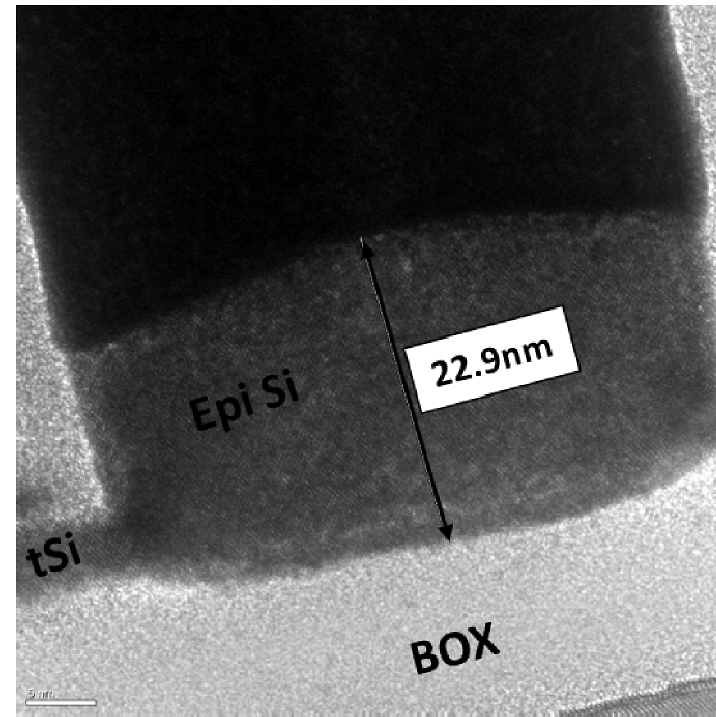
Low-temp. FinFET gate last & SAC

L. Pasini et al., VLSI 2015

J. Micout et al., IEDM 2017

Low temperature silicon epitaxy





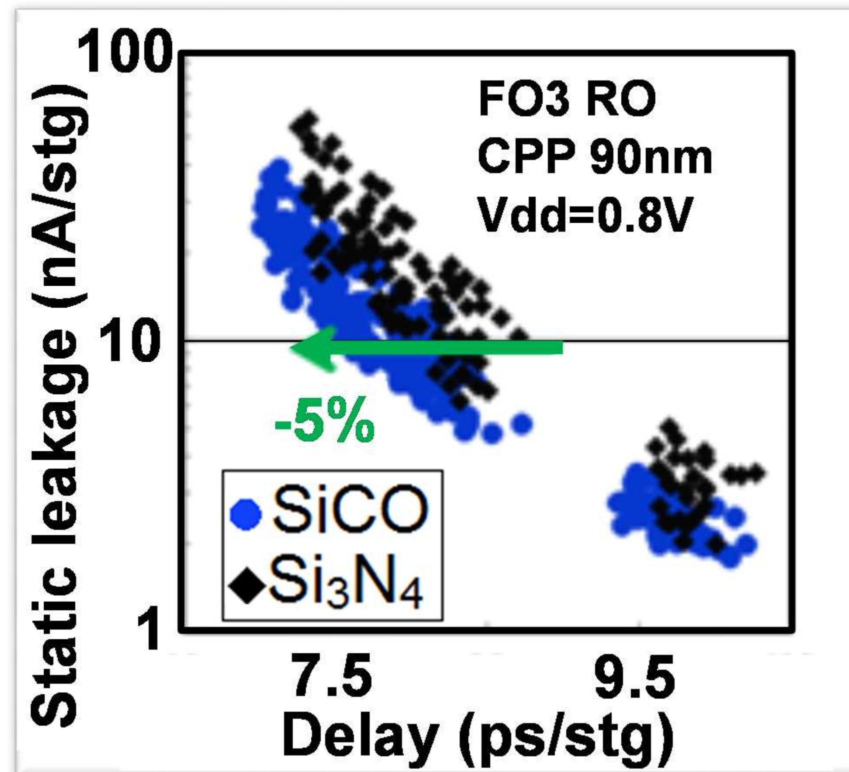
Selectivity and crystallinity validated at 500°C

Obtained by cyclic and deposition etch

V. Lu et al., VLSI-TSA 2017

Low temperature process tool development helps

Ex: ALD Nitride Ofset spacer replacement

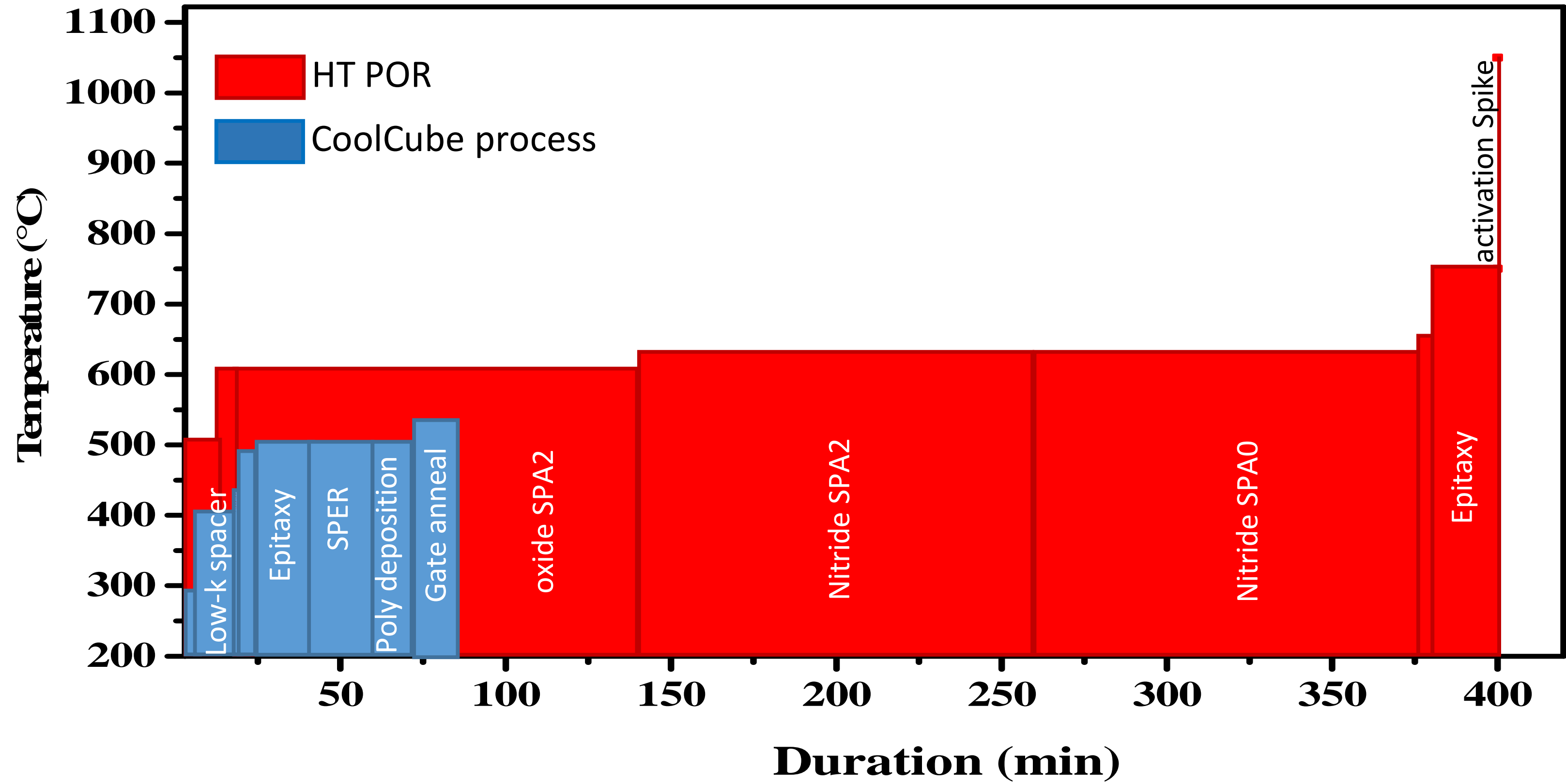


400°C SiCO spacer has been integrated succesfully

Gain in delay thanks to low k value

D. Benoit et al., IEDM 2015

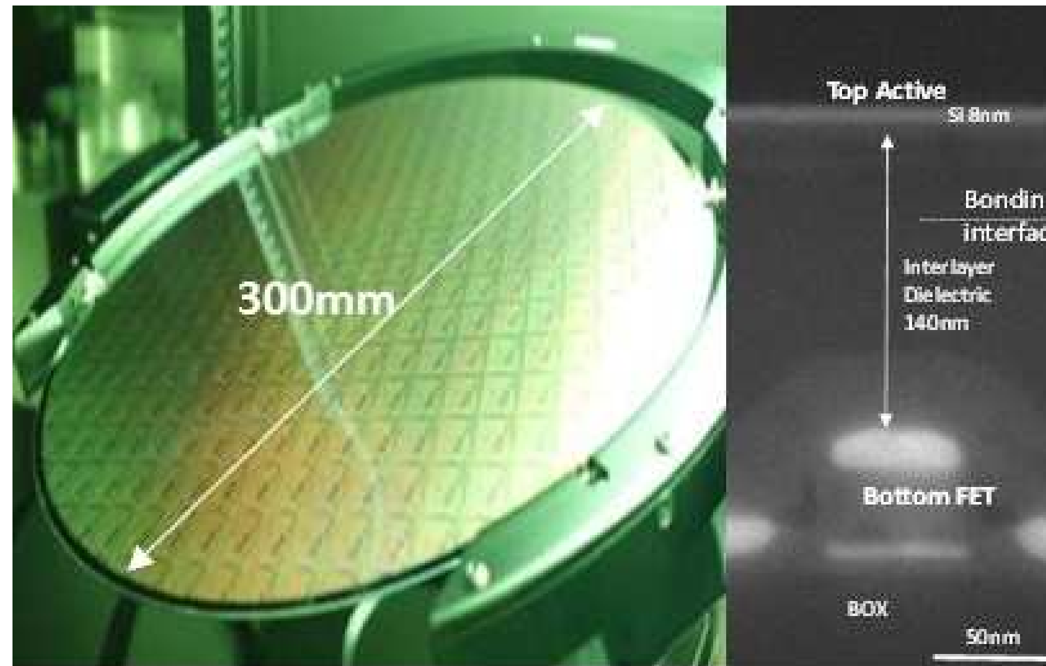
Illustration of the TB footprint reduction



Top FET thermal budget is well below the 500°C 5h limit

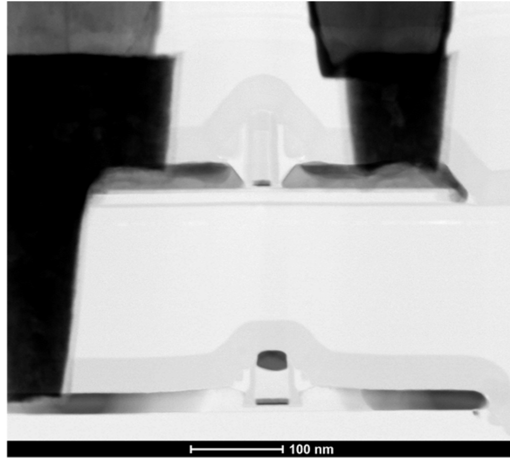
Top channel quality

Si Thin film transfer by SOI bonding

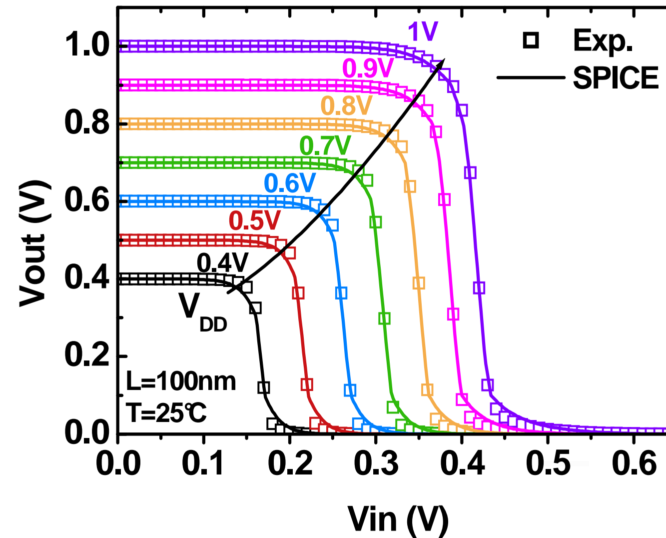


SOI transfers above MOSFETs demonstrated in 300mm
Low thermal budget<400°C
Perfect cristalline quality and thickness control

300mm fab 3D demonstration



L Brunet, VLSI 2016

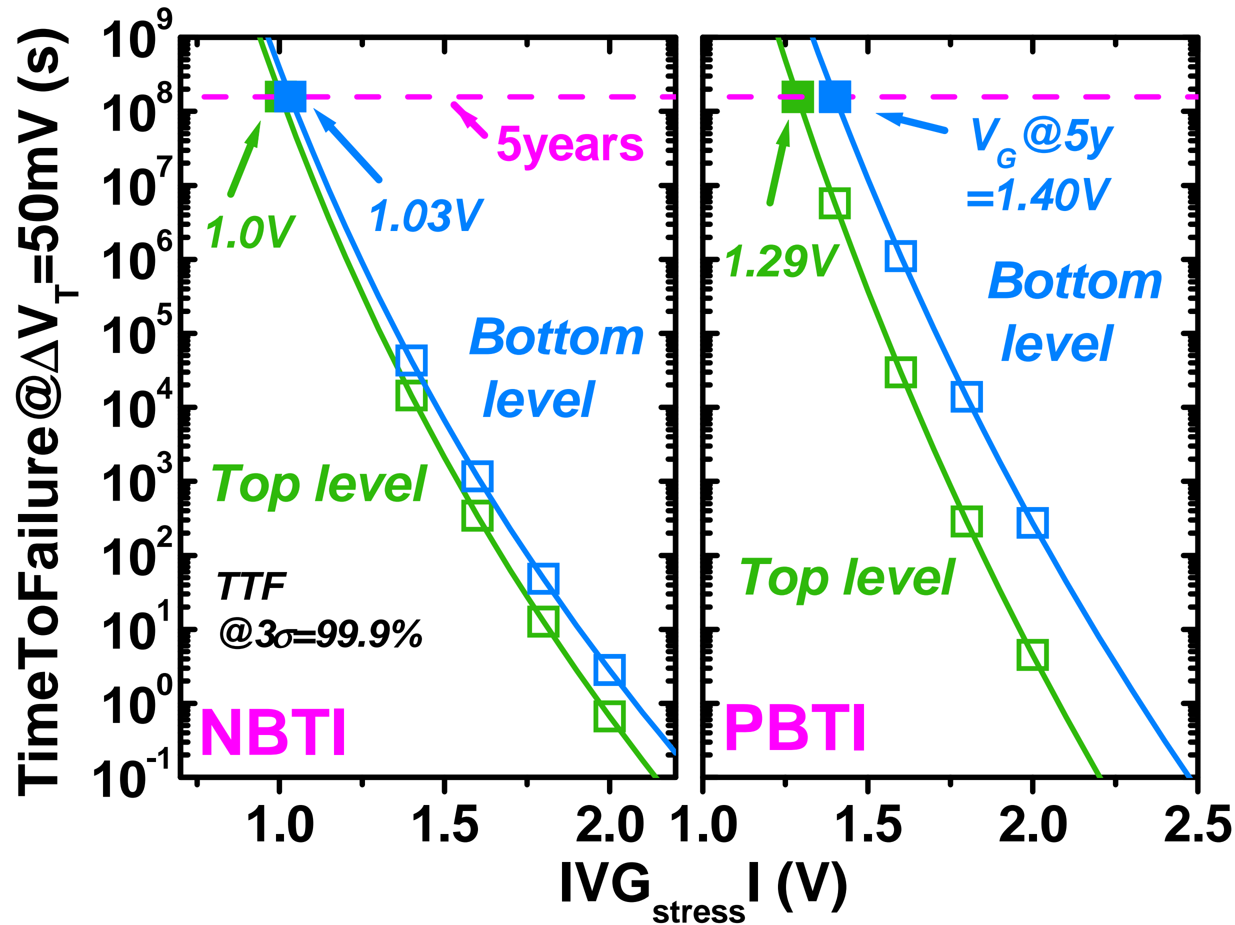


A Tsiara, VLSI 2018

- ✓ **Nanometric lithography alignment at wafer scale**
- ✓ **3D contact size=100nm**
- ✓ **10 nm thin top active layer**
- ✓ **BEOL→ FEOL transition demonstrated (NiPtSi)**

300mm fab 3D demonstration

A Tsiara, VLSI 2018 **First time analysis of performance and reliability of a 3D seq. scheme**



BTI@T=125°C Crit=50mV	VG@10y/3σ, PASS if VG>0.9V
PMOS (TL/BL)	0.98V/1.01V OK
NMOS (TL/BL)	1.26V/1.37V OK

☺ **First demonstration of TL passing lifetime criteria**

Outline

Computing applications: Following More Moore

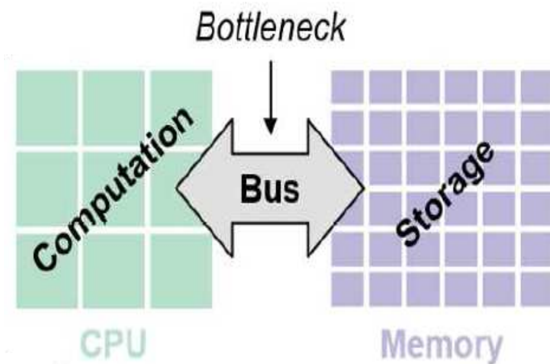
Alternative computing architectures

Sensor interface (More than Moore)

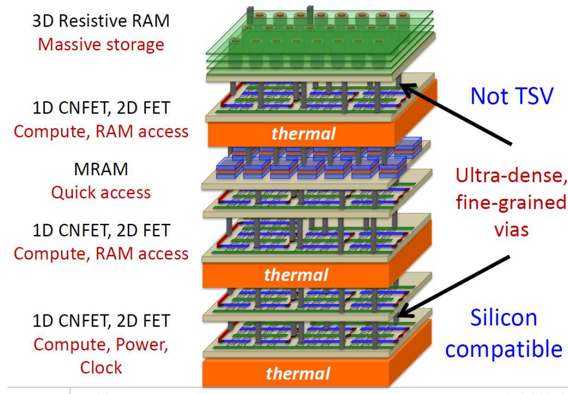
Global intention:
describe technology rquirements for specific applications

Alternative Computing to Von Neuman architecture

→ 3D sequential is an opportunity to break the memory wall



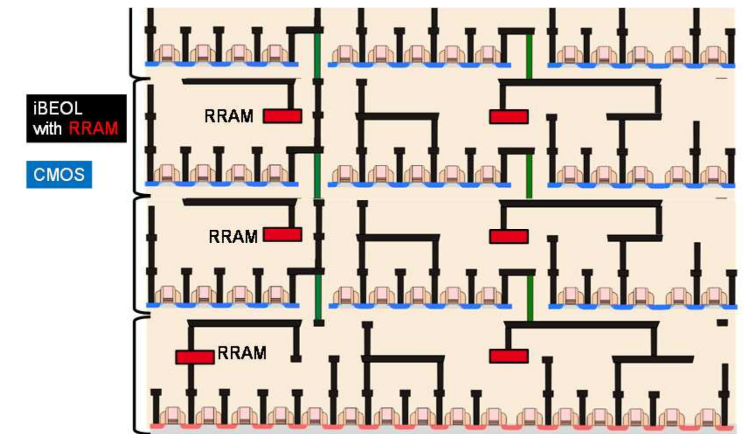
Computating immersed in memory



N3XT Computing system [1,2]

X 1000 gain in consumption expected with computing near memory

Neuromorphic computing



Brain-inspired computing cube

- High contact density mimics the high interconnectivity of neurons
- RRAM mimics the synapses

[1] Shulaker et al., IEDM 2014 , [2] Aly et al., Rebooting computing, 2015

Alternative computing:

Applications: **Near memory computing** **Neuromorphic computing**

- High number of stacked layers needed

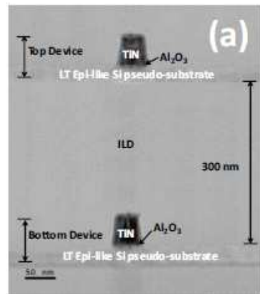
Top MOS TB ~500°C 2h / Max TB tier 1= 500°C 5h → Maximum 2 stacked layers

-Transistors performance is not the bottleneck

Interest for Ultra low TB MOSFETs (400°C)

Alternative computing: Ultra low TB FETs (400°C)

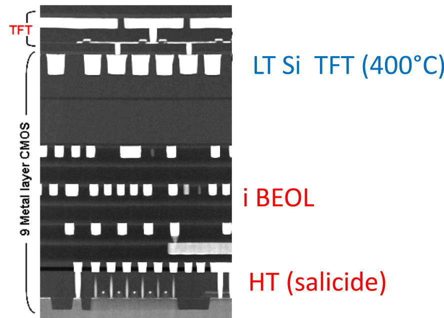
Transistors on Poly Si



LT Si TFT (400°C)

HT (salicide)

[1,2] NDL



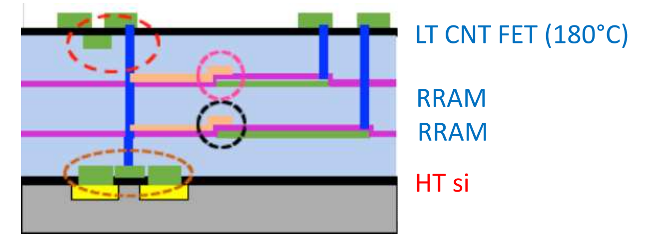
LT Si TFT (400°C)

i BEOL

HT (salicide)

[3] Toshiba

CNT FET (180°C)



LT CNT FET (180°C)

RRAM

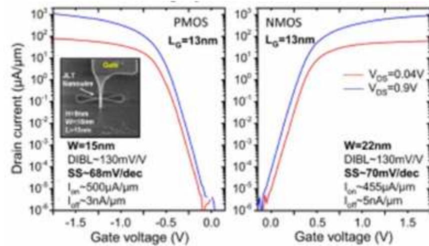
RRAM

HT si

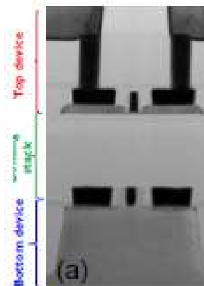
[4] Stanford, MIT

Junctionless

Monocrystalline channel

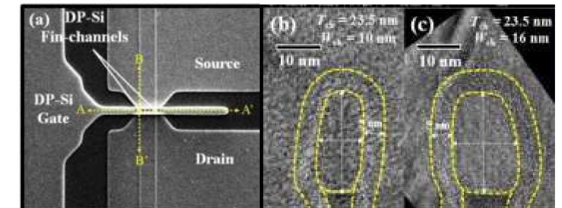


[5] Ieti



[6] IMEC

Polycrystalline channel

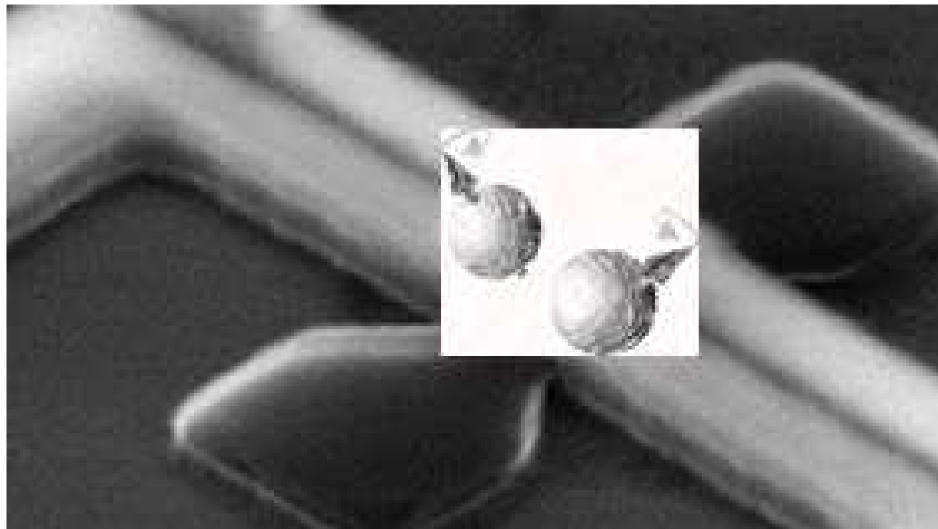


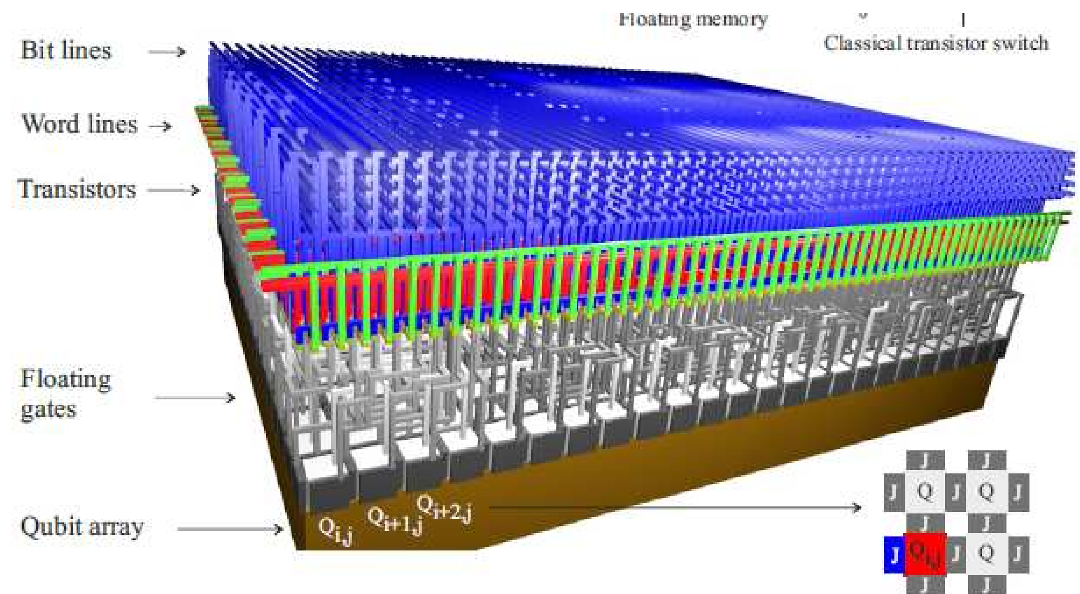
[7] NDL

[1] T. Wu et al., IEDM 2015, [2]f-K. Huesh et al., IEDM 2016] [3] [4] M-M. Shulaker et el., IEDM 2014] [5] S. Barraud et al., EDL 2012
[6]: A. Vandooreen et al., S3S 2017 [7]: D-R Hsieh, TED 2017

Alternative computing: Quantum computing

Spin-based quantum dots must be coupled to each other in a dense array





Stacked error code correction layer to adress every qubit in the array

M. Veldhorst et al., https://arxiv.org/pdf/1609.09700.pdf

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Computing applications: Following More Moore

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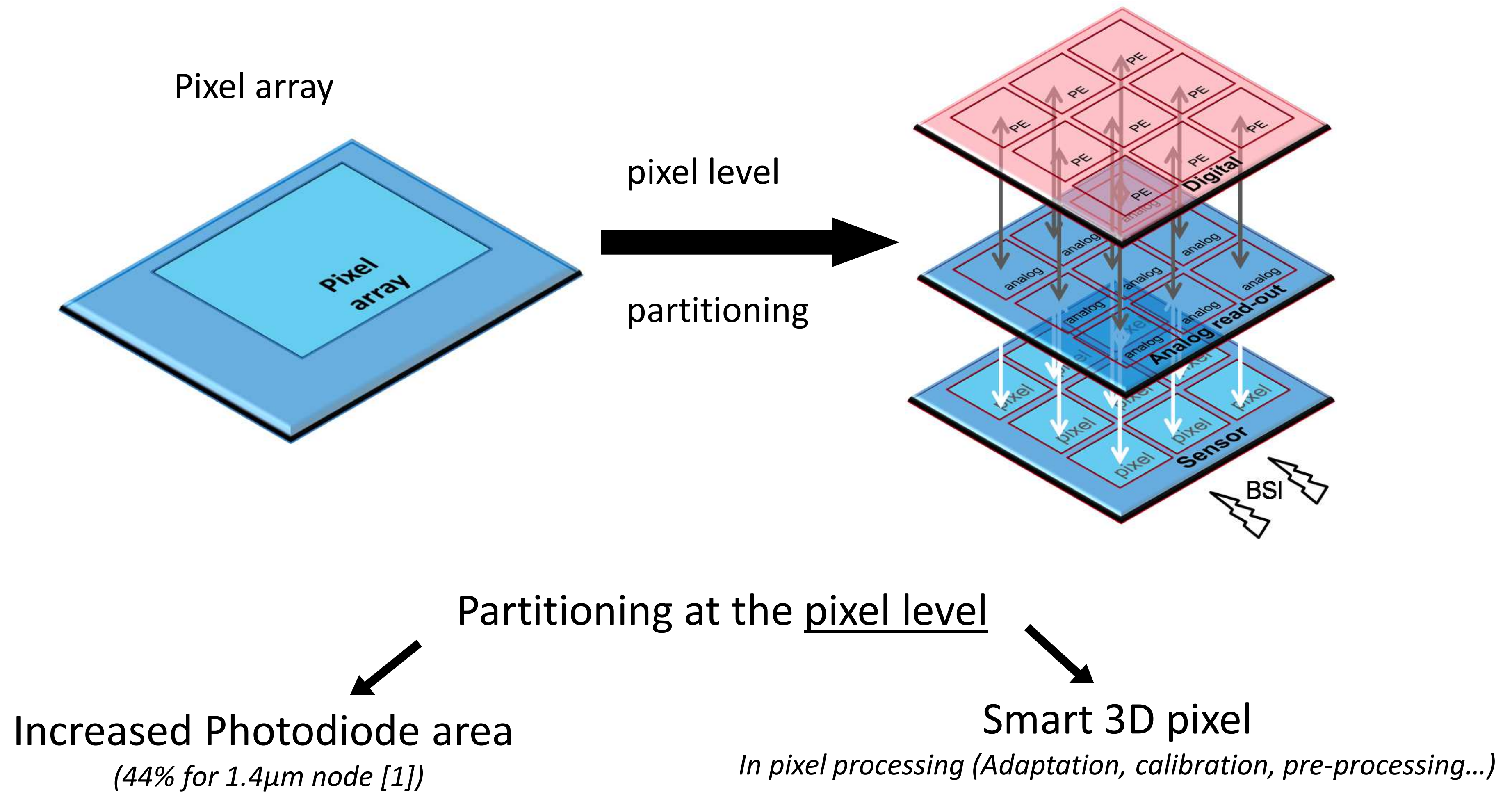
Sensor interface (More than Moore)

Global intention:
describe technology requirements for specific applications

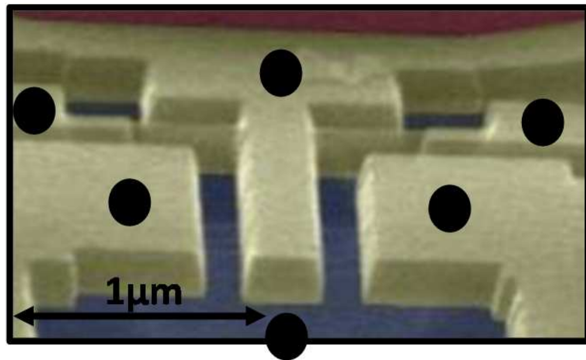
Sensor interface: Application examples: image sensor



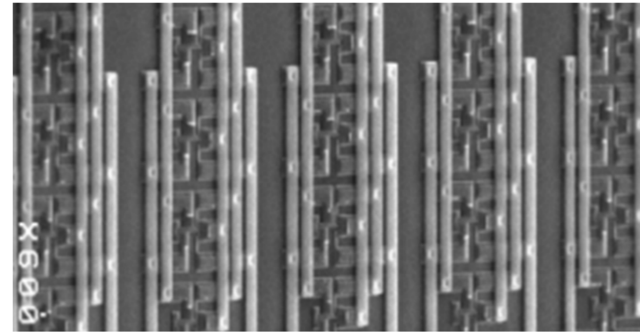
[1]:P. Coudrain et al., IEDM 2008

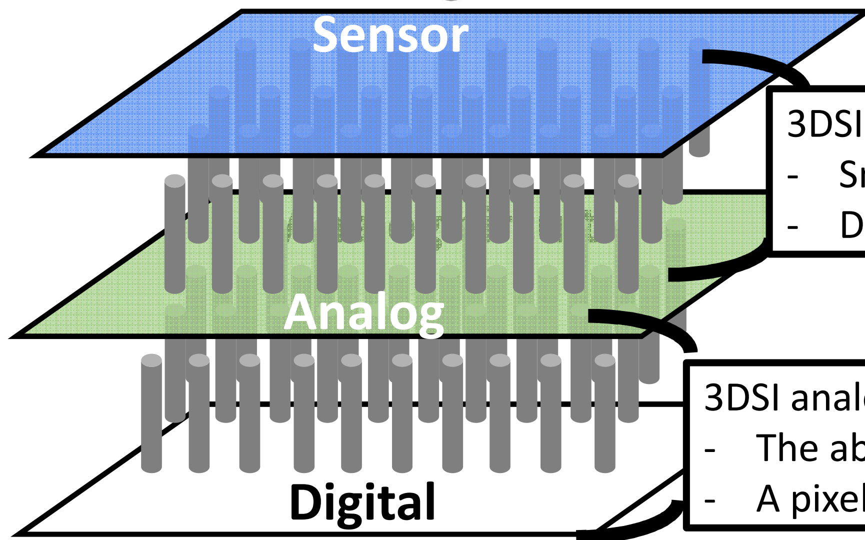
Sensor interface: Application examples

Arrays of resonant NEMS for mass spectroscopy applications



[1]





3DSI offers
- Small parasitics
- Density of contacts (i.e. 6 to 8 /µm2 needed fo NEMS)

3DSI analog and digital
- The ability to partition analog and digital for small pitch pixel
- A pixel foot print reduction

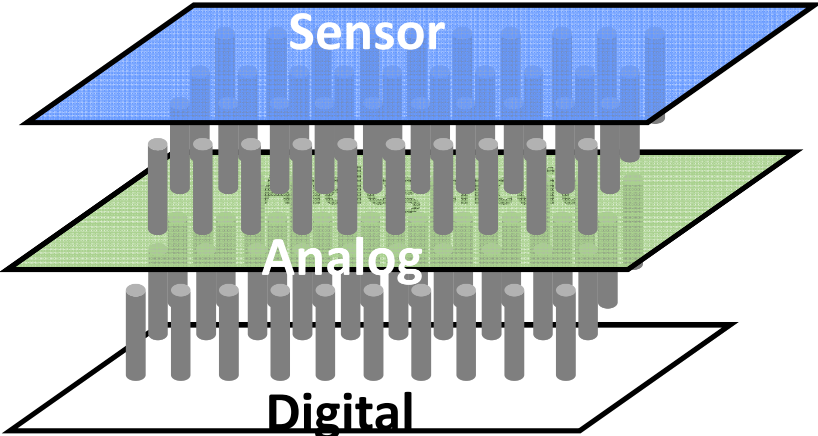
[1]:E. Sage et al., arxiv 2017

Sensor interface

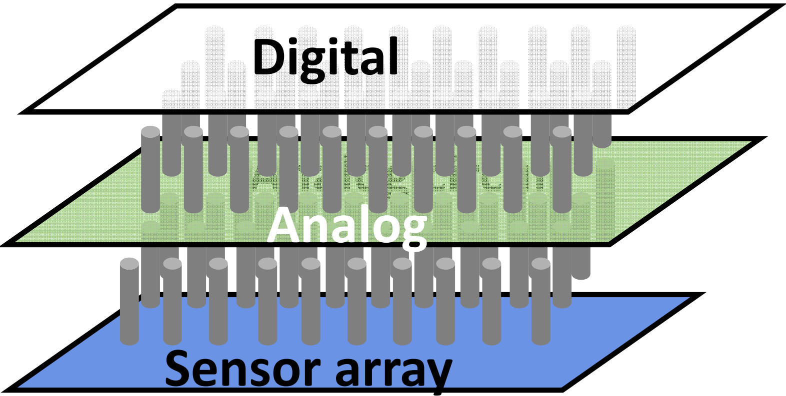
Analog device needed

Different partitionning depending of the sensor type (front side or back side)

Front side sensor (NEMS of FS image sensor)



Back side sensor (Back side photodiode)



Analog devices integration in 3D sequential

Analog FET thermal stability :

Relaxed nodes are mostly used:

- Thicker Ni-based salicides → increased stability [1] ☺
- Eventually Co-based salicides → up to 700°C TB max [2] ☺
- iBEOL not necessarily needed between FETs ☺

Low-temperature analog MOSFET development:

Gate lengths are relaxed :

- Thin channel is not mandatory (RSD epitaxy supressed) ☺
- R_{access} optimization is less critical ☺

Increased constraint on gate stack quality ☹

[1]:De Keyser et al. Appl. Phys. Lett. 96, 173503 _2010 [2]: P. Coudrain et al., IEDM 2008

Conclusion

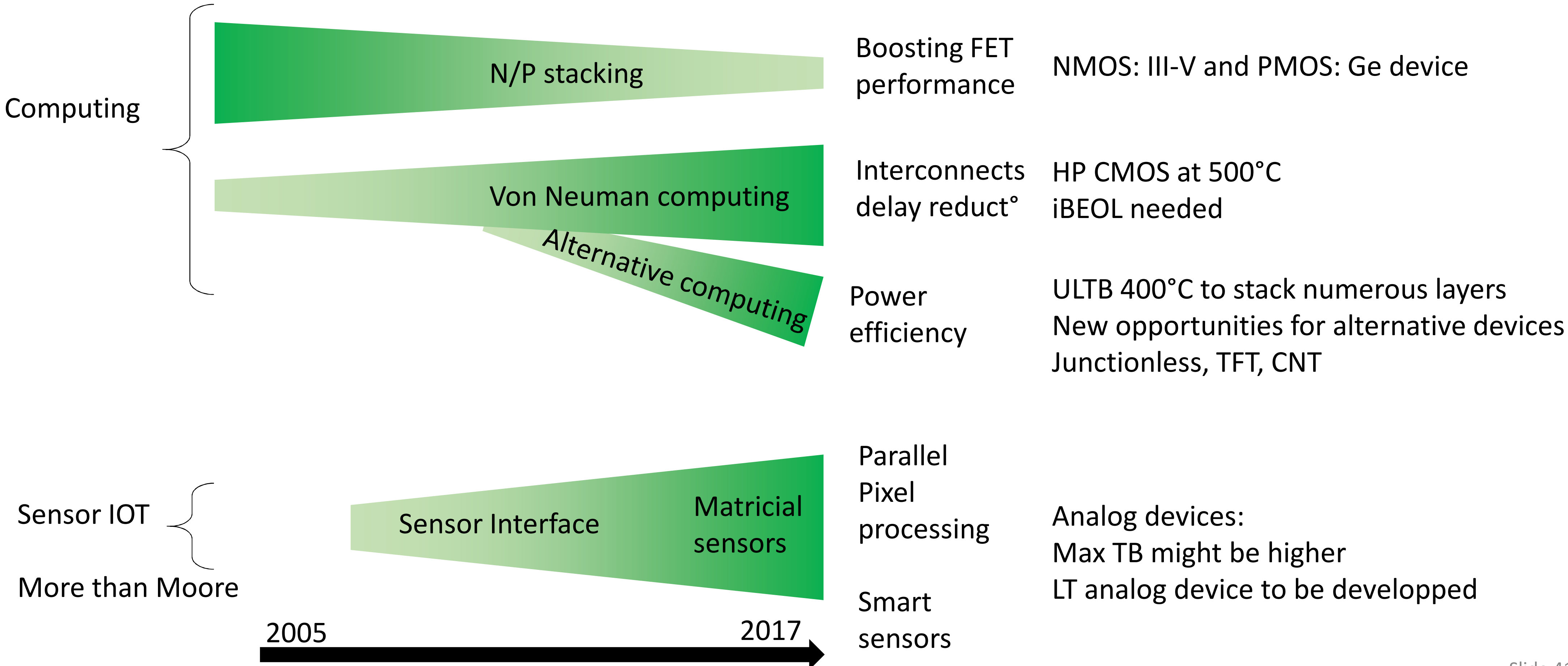
3D sequential is demonstrated in a 300mm industrial environment

Bottom tier (MOSFET and interconnection) max TB =500°C

All the process modules for top HP FET are within this 500°C TB limitation

Computing is the most demanding application in terms of device I_{ON}/ I_{OFF} performance

Conclusion



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Thank YOU for your attention