3D Scalability from High Performance to Ultra Low Power

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Technology Effects are Accelerating

Global Connectivity

Smartphones as Appendages

Mobility

Smart Mfg

Chore Time Down

Social Media

Smart Manufacturing

Effects of "Free Shipping"

From Text to Voice to Photos & Video

Internet as Ultimate Source of Memory

Artificial Intelligence

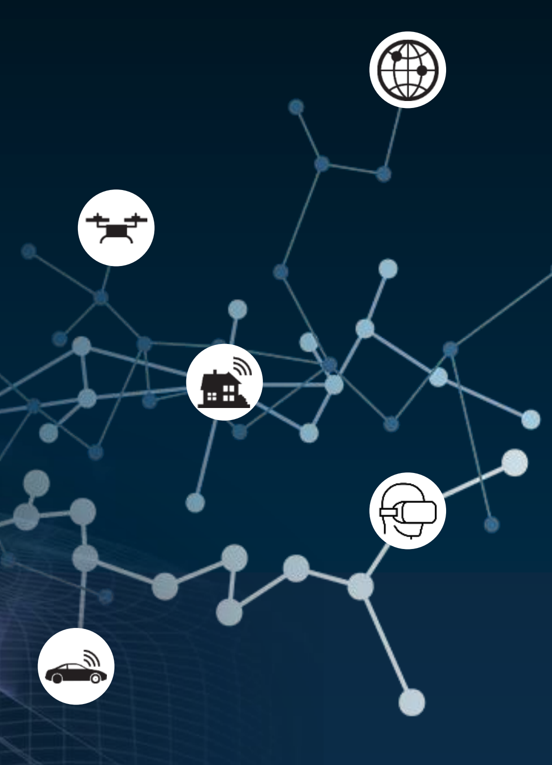
Loss of Privacy

Augmented/ Virtual Reality

Autonomous Vehicles

Cybersecurity

Entertainment Anytime, Anywhere



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Rapidly Expanding Client Capabilities

Client Capabilities

- Camera, optics, sensors
- Always-on voice & video
- Local Interactions – voice, video, context
- Continual feedback

In High-Profile Applications

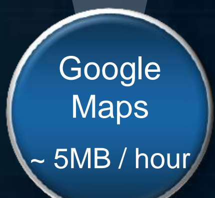
Mobile Vision

IoT

Generating exponential growth in data that requires Local processing

Self-Driving Car ~25GB / hour

HD Video Streaming ~0.9GB / hour



Cloud + Intelligent Edge

- > 10X lower latency
- Lower costs
- Increased privacy
- Real-time decisions
- Cloud storage & analytics

Self-driving cars *need their own* AI capabilities on-board, *to make real-time mission-critical decisions* [1]

Industry-leading smartphone OEMs and chipmakers are *focused on* doing AI on the device instead of the cloud [2]

Sources:
[1] Bernstein Research in https://www.gam.com/en/insights-content/2017/thematic/cloud-plus-intelligent-edge-the-fog/
[2] The Verge in https://www.theverge.com/2017/9/13/16300464/apple-iphone-x-ai-neural-engine
GF Internal assessments

Source: Bernstein Research

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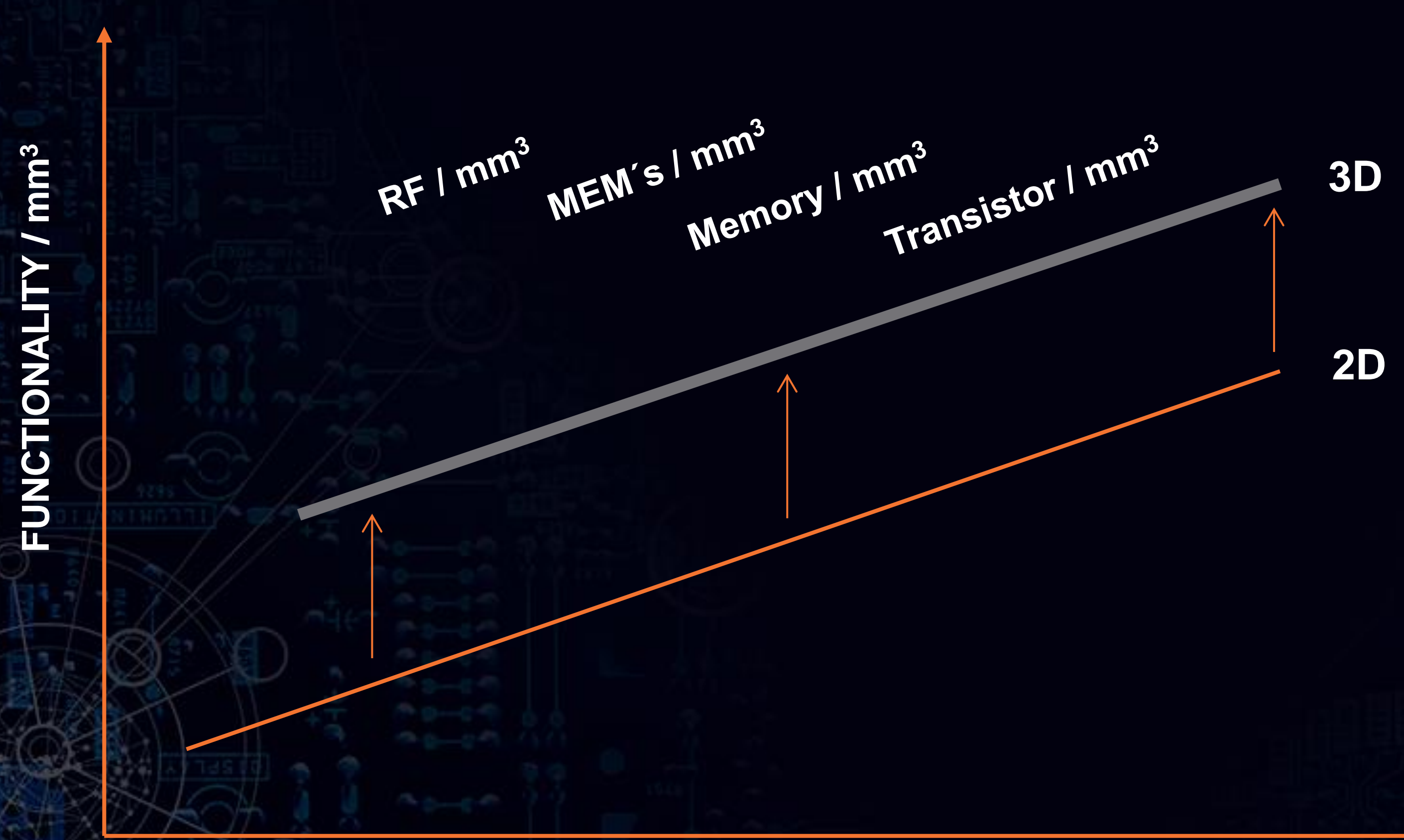
How Can 3D Packaging Enable Scaling?

- Need to think in terms of FUCTIONALITY per VOLUME, not area…..



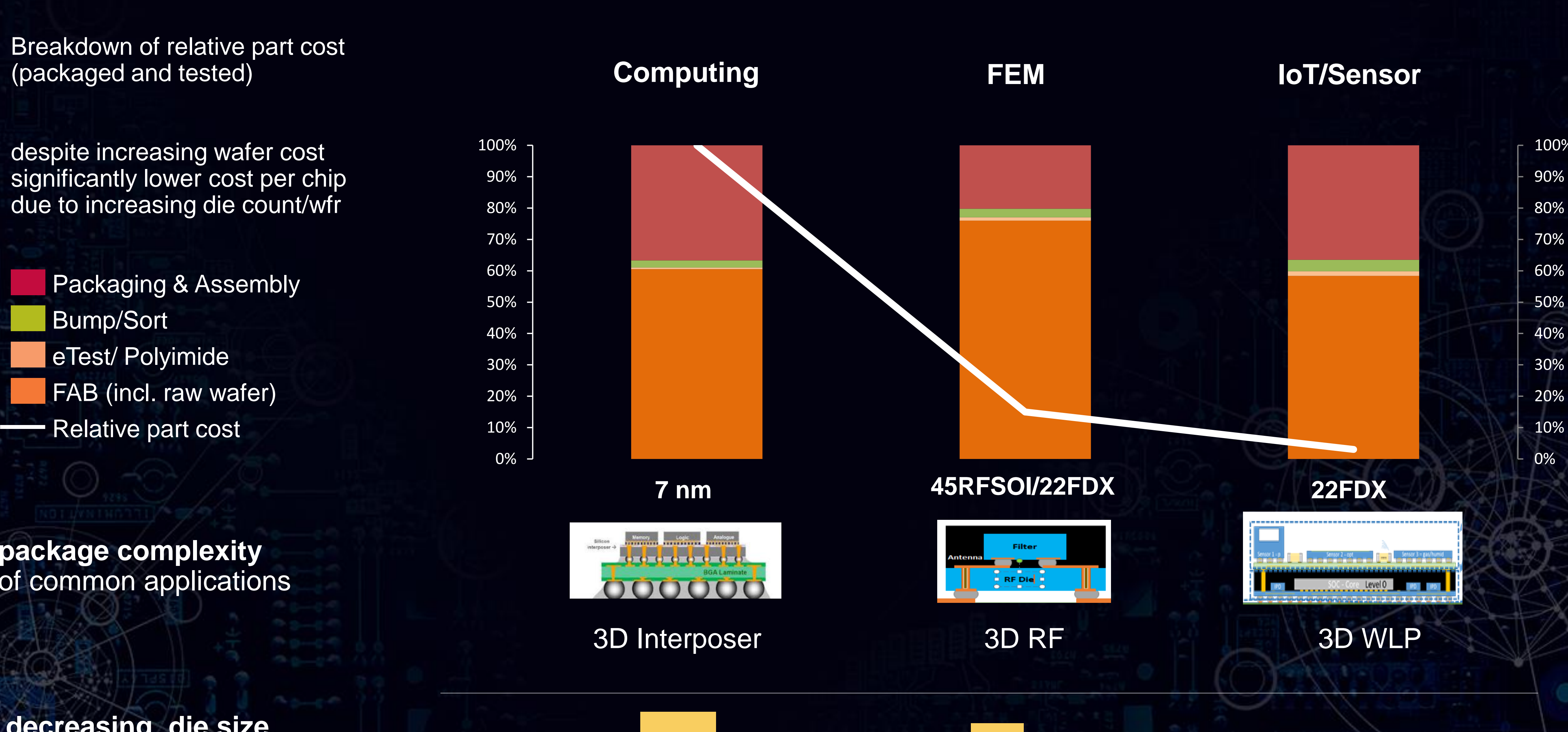
- Stacking die results in larger number of transistors/devices
- Stacking die enables heterogeneous functions (MEM´s)
- Stacking of functions enables compact systems (5G, Imager)

EASY Concept

- Lets talk about how we get there!

Increasing importance of 3D packaging in overall chip supply chain

while Moore's law is valid for silicon, packaging becomes major driver for cost per chip



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Our Top Questions. Where do we go next?

1. What's the right technology for my specific application?
2. How do I accelerate time to market at lowest cost?
3. What 3D technology for which application and why?

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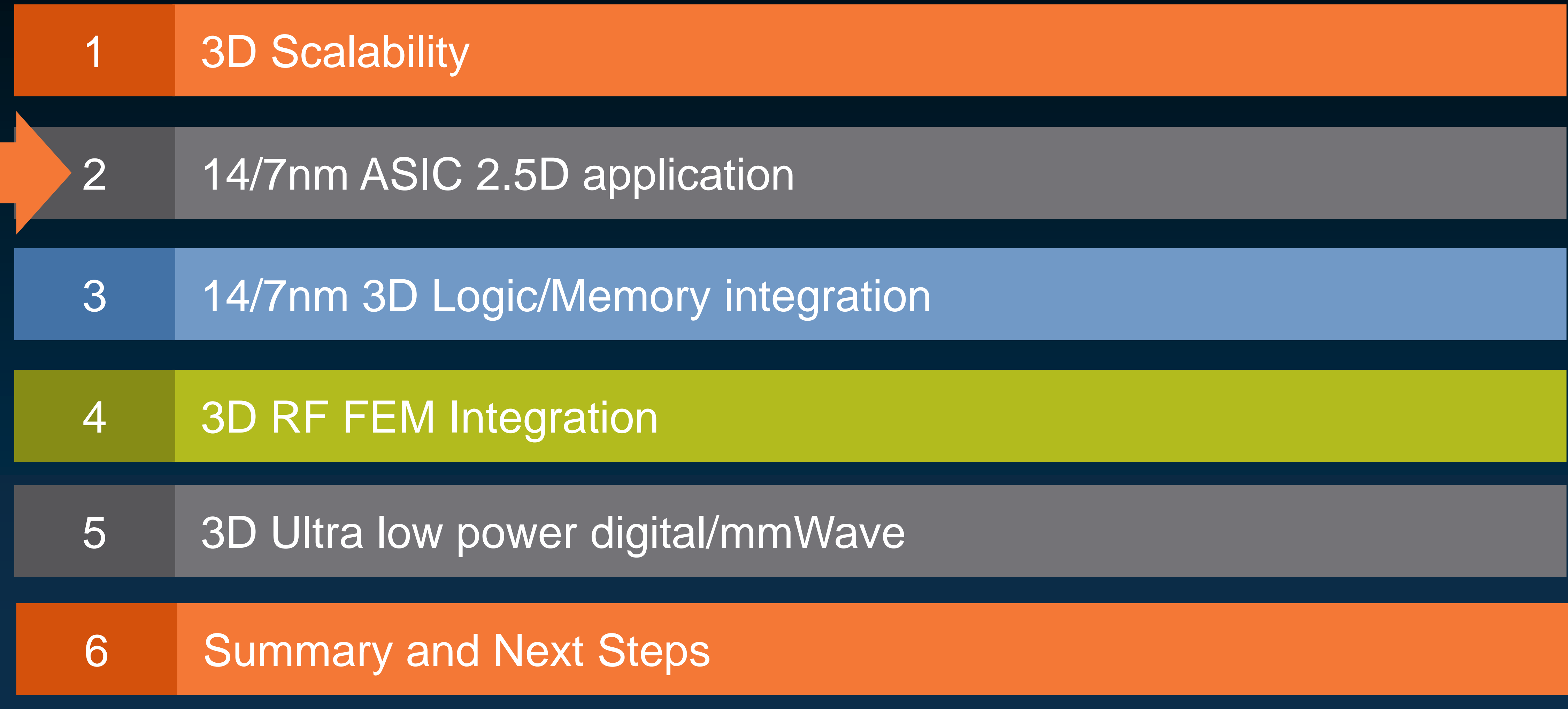
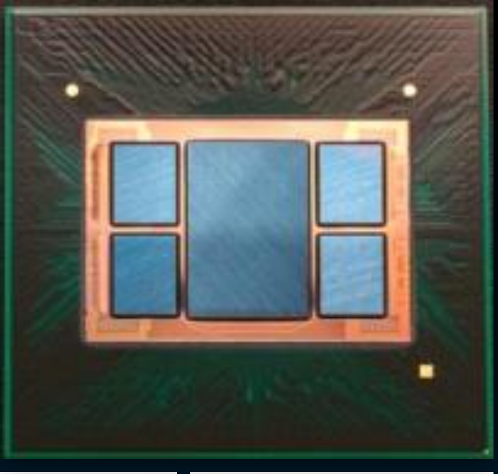
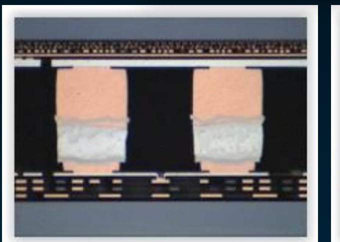
Agenda

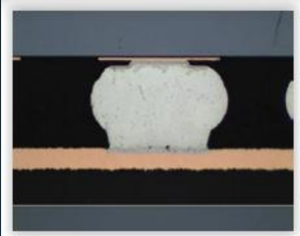


2.5D Package Integration w/ Silicon Interposer

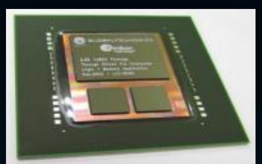


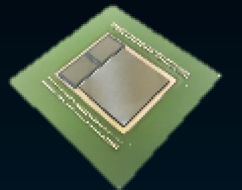
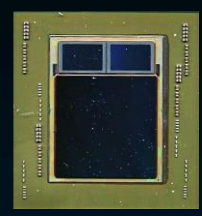
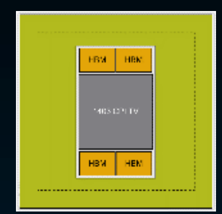
- GLOBALFOUNDRIES continues to solidify its leadership position in 2.5D technology
  - Primarily driven by HBM integration:
    - Provides high bandwidth access to on-module memory
    - Multiple 14LP products taped out, more in execution
    - 14LP will feature enhanced 3.2 Gbps HBM2E PHY
    - HBM gen3 support planned once memory definition is complete
  - 7nm will expand integration capabilities with a high-I/O, low power parallel interface
    - Up to 800 Gbps per mm of chip edge
- 7nm will be the 4th GF silicon node qualified on silicon interposer
- Flexible business model enables:
  - Full ASIC module turnkey offering with GF ownership of HBM component procurement, yield and reliability
  - Lowest cost solution with HBM consignment model





2.5D Packaging Test and Qualification Vehicles



TV	1	2	3	4	5	6
	Base process setup	CPI Qualification	functional HBM Qual	CPI Qualification + Thermal	Product Qualification	CPI Qualification
Interposer size	26x32 mm	26x32mm	19.5 x 26.2mm²	25 x 30mm²	27 x 35mm² (stitched)	30 x 44.5 mm² (stitched)
TSV dia/depth	10µmx100µm					
Top die arrangement	1 large, 2 small	1 large, 2 small	1 large, 4 HBM1	1 large, 2 HBM2	1 large, 2 HBM2	1 large, 4 HBM2
Large die size	400 mm² (32nm)	324mm² (28nm)	160 mm² (28nm)	410 mm² (14nm)	640mm² (14nm)	640mm² (14nm)
Package size	50x50mm²	50x50mm²	40x40mm²	50x50mm²	>60mm²	65mm²
P5 Package Qualification	Pass ✓	Pass ✓	Passed functional qualification ✓	Pass ✓	2Q2018	ERA: 4Q2018 P5: 2Q2019

2.5D Integration effect on Chip Size

	SCM	w/HBM	Area Decrease
IP	~40 DDR Cores	1 HBM PHY	
Chip Size	DDR	HBM	-15% (depends on chip size)
Laminate			-30-40% (depends on laminate size)

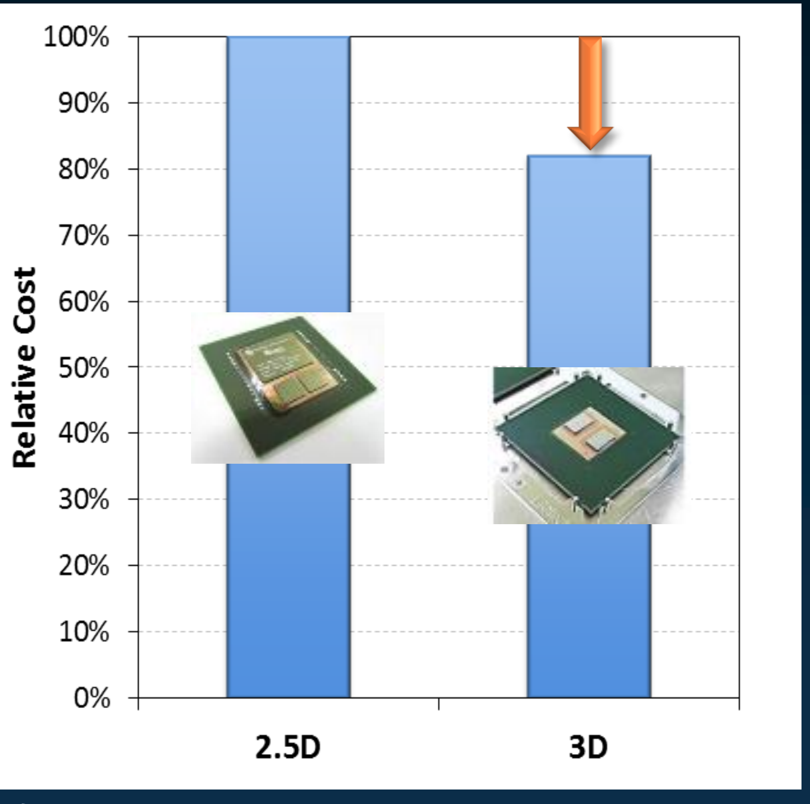
- Additional cost of interposer and assembly steps can be offset by smaller 14LP logic chip and laminate size depending on the product definition

3D Packaging as a Cost Reduction?

- For an ASIC die w/ HBM, 3D packaging is generally lower cost than 2.5D.
- Assume an ASIC + 2 HBM:

Key Cost Component	2.5D	3D
ASIC Die + Bump	x	x
Si Interposer + Bump	x	
TSV Fabrication	x	x
TSV Reveal	x	x
HBM Stacks	x	x
No. Flipchips	4	3

~20% Cost Reduction



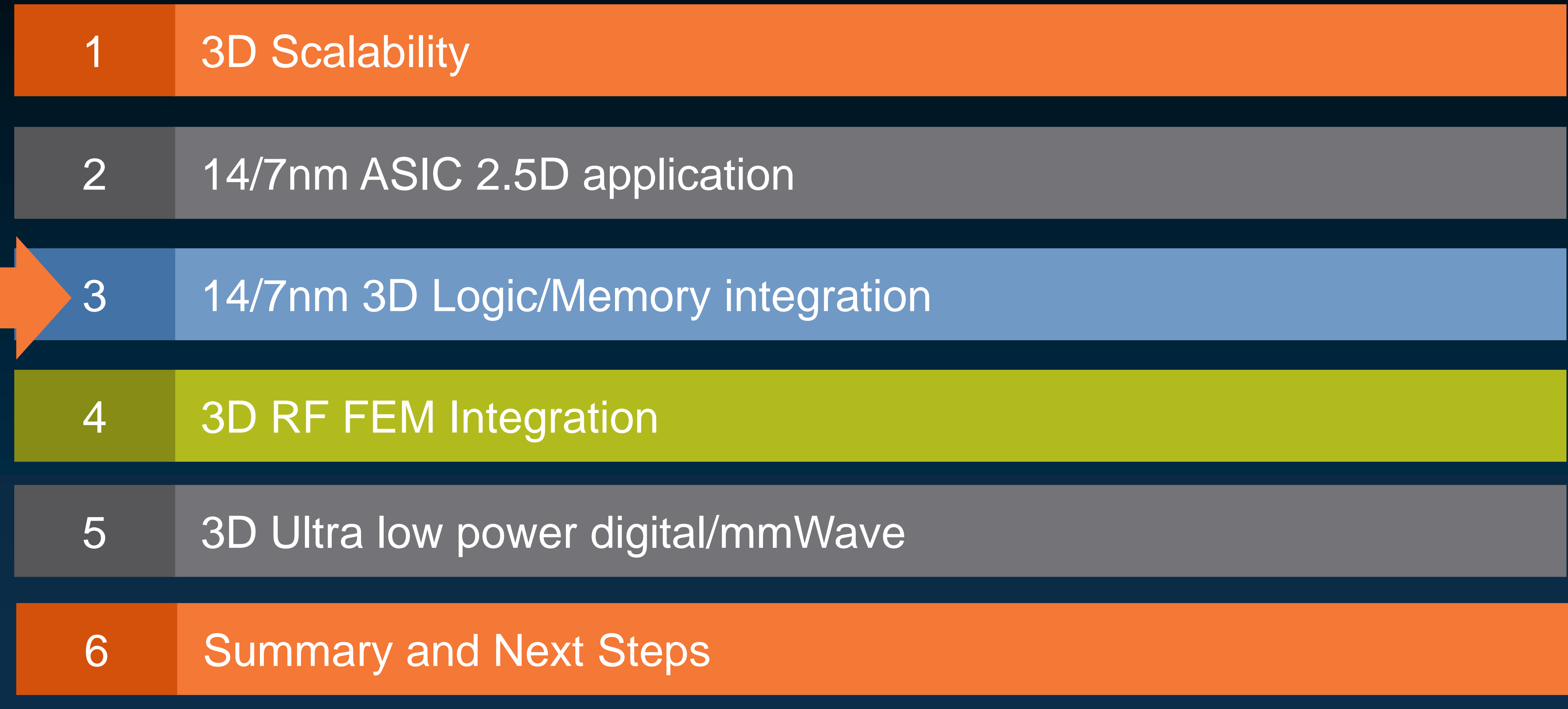
3D eliminates the Si interposer fabrication, bumping, and flipchip costs. Test cost not included.

thoughts

- Future will bring 6 HBM’s industry players already seems to have hardware

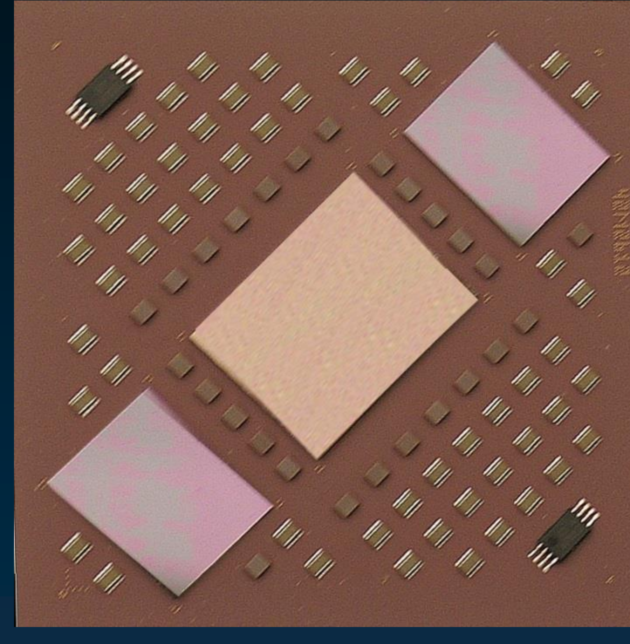
- Industry is not happy with Si Interposer due to cost, yield, and complexity
  - Competing solutions are evolving
    - 2.1D (e.g. iThop)
    - Fan-Out Technologies (TSMC’s InFo, Samsung, all OSATs)
      - Line and space for RDL routing reduced to be close to silicon (or good enough)
      - Fan-Out on substrate is already qualified
    - Over molded TSV last (some OSAT), but limitation on pitch

Agenda



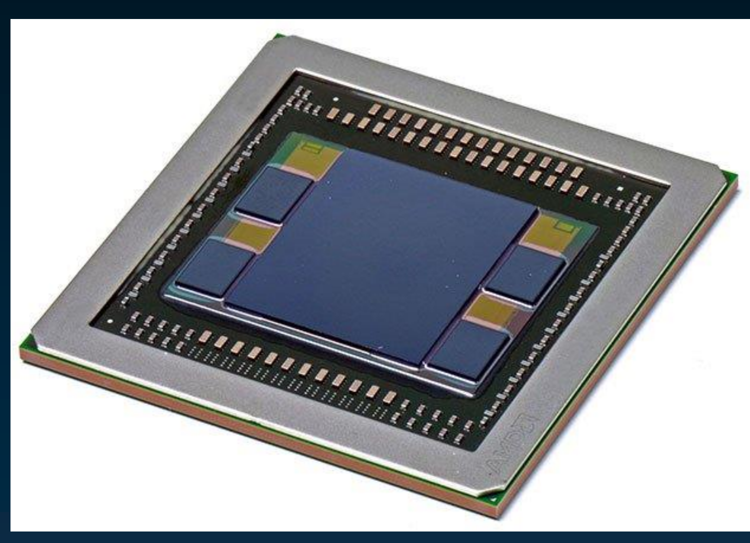
Pre-3D Logic Advanced Memory Solutions

IBM Power6



Intel Haswell

AMD Vega GPU



Board Level Integration → **TSV Integration**

3D TSV Enablement & Status

Implementation Status

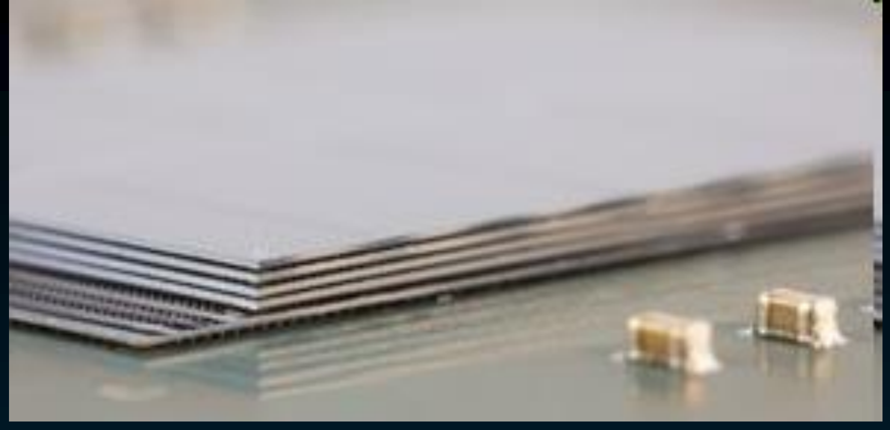
- TSV process capability at GLOBALFOUNDRIES
  - 32nm: HVM Production in East Fishkill, NY
  - 14nm: Package reliability qualification complete
  - 7nm: TSV Process defined and Development ongoing

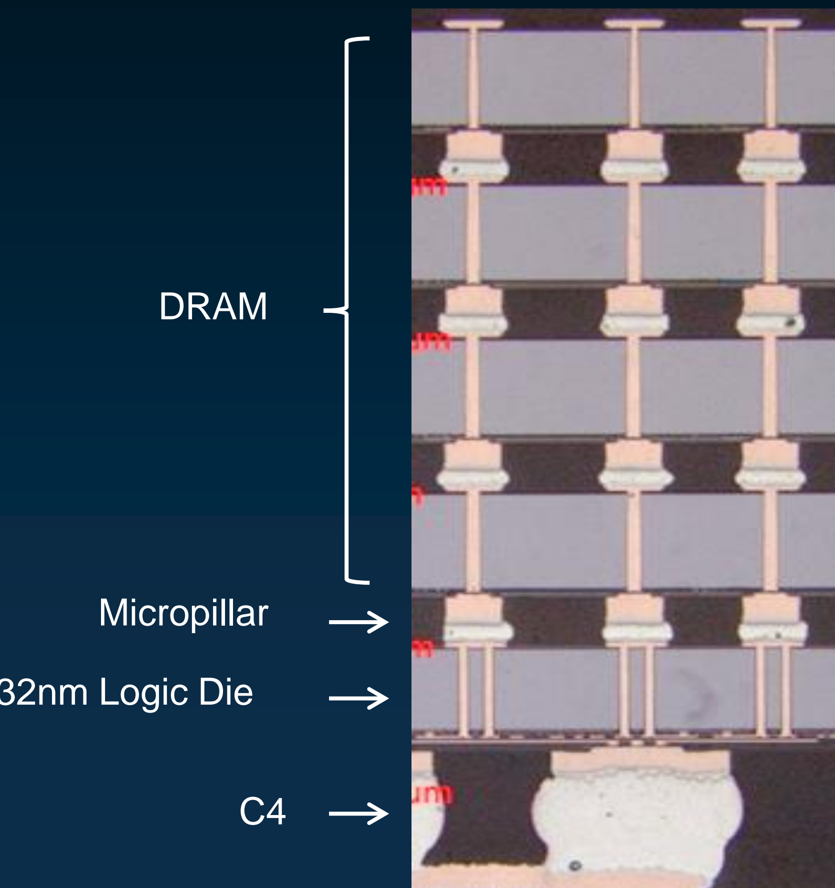
Manufacturing Flow

- Wafer fabrication w/TSV at GLOBALFOUNDRIES
- Wafer-to-wafer bonding at GLOBALFOUNDRIES
- Develop and utilize OSATs for TSV wafer Backside Integration (BSI) and 3D packaging

TSV Program Status

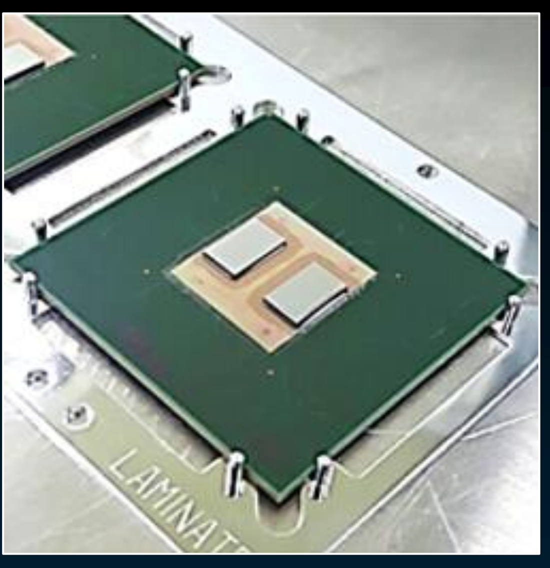
- ✓ Excellent reliability and yield results
  - ✓ TSV integration & functional characterization
  - ✓ TSV package test & reliability data
  - ✓ TSV production ready for 14nm
- ✓ 7nm process defined and in development
  - ✓ First production implementation planned for 3D SRAM
  - ✓ Design manual and PDK availability (7nm PDK0.9_1.0)



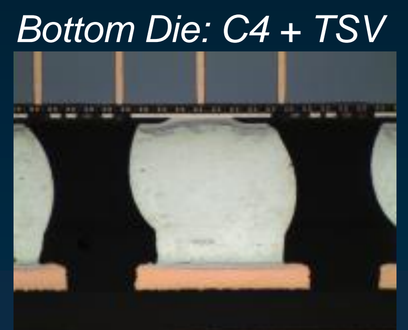


14nm 3D Testsite

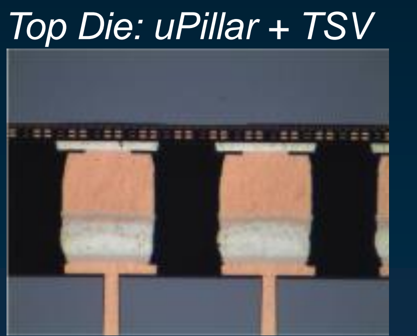
- Backside processing (MEOL):
  - Soft reveal process used to reveal the TSVs from backside, followed by Cu RDL and Ni/Au capture pad.
  - Die-to-Substrate (D2S) process with Mass Reflow (MR) used to stack 50um thin TSV die and thick top dies.
- Assembly results:
  - 100% yield for C4 and Micropillar attach achieved with optimized assembly process

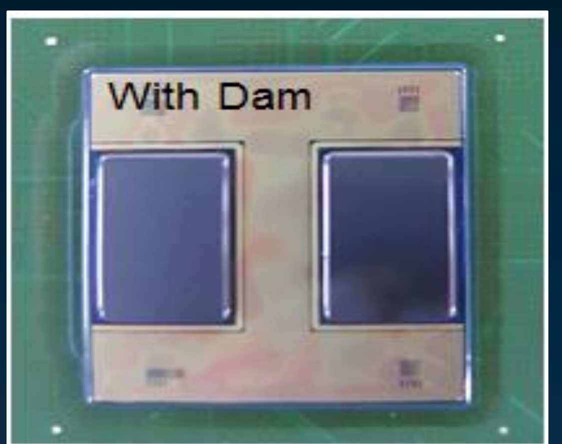


Bottom Die: C4 + TSV

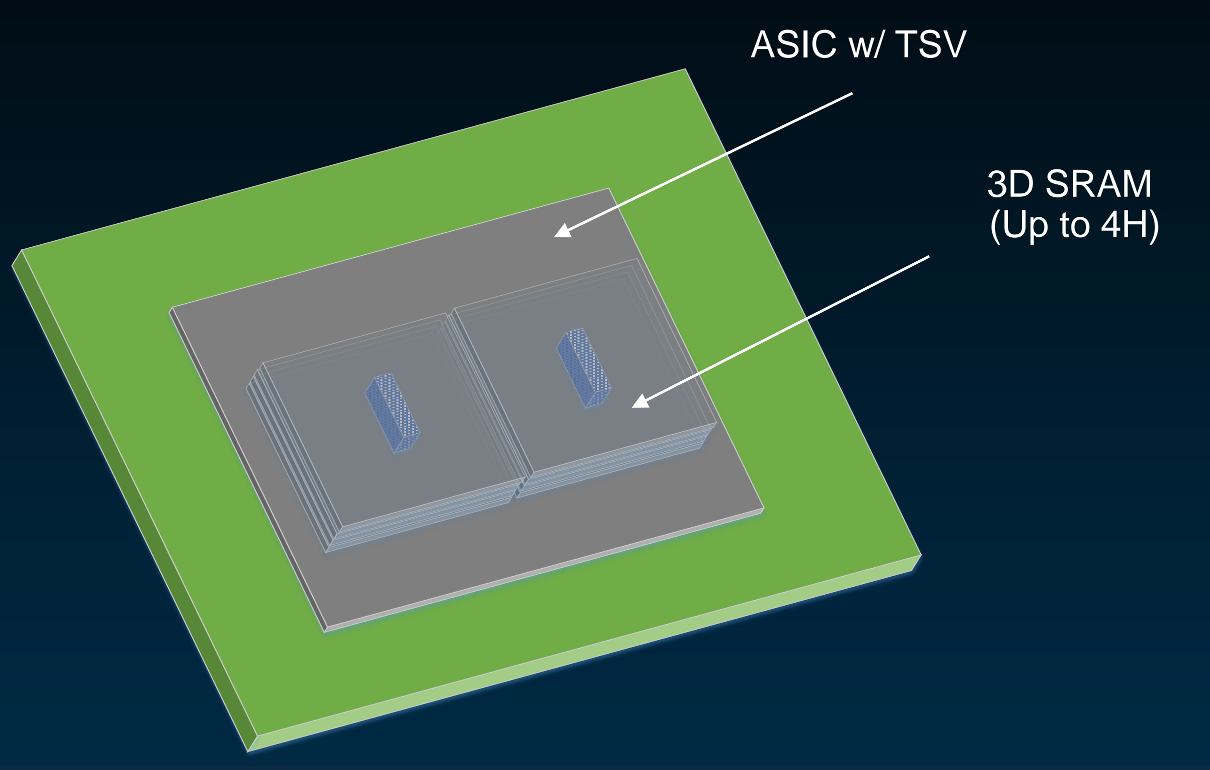


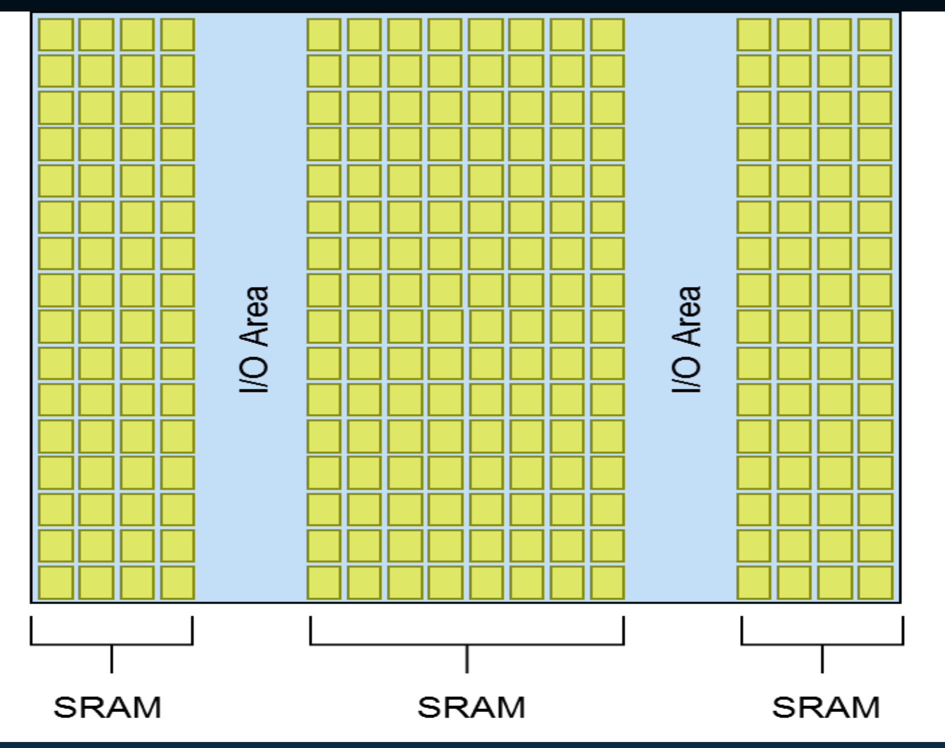
Top Die: uPillar + TSV





3D SRAM Enabling Efficient Memory-Logic Coupling





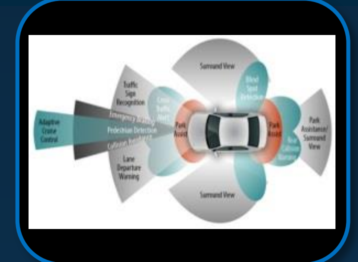
- 3D SRAM under development to provide HBM alternative for high performance computing applications.
  - Data Center, Networking, Artificial Intelligence / Machine Learning.
  - Low power, high bandwidth (~8x bandwidth of HBM2).

Why 3D SRAM?

Performance Comparison to HBM2

3D SRAM Supports Industry Needs!

Parameter	HBM2	3D SRAM
# Channels	1X	6X
Data rate / IO	1X	2-4X
Bandwidth (unidir.)	1X	~10X
Max Capacity	1X	~1/10 X
Power	1X	~0.3-0.5X
Random Cycle	1X	60X
Latency	1X	>5X
Integration	2.5D	3D on ASIC
Temp capability	Limited by DRAM	-40 to 125°C
Automotive Support	No Path to Automotive Support	No Gates for Automotive Support



Conclusions

- 3D packaging is here, and is primed to help industry continue “scaling” ---> need to consider volumetric rather than area based device densities.
- Two 3D logic implementations are on the near term horizon:
  - Memory stacking on logic.
  - 3D SoC design ---> Fine grained IP block partitioning.
- Solutions available for ultra-thin die and thermal challenges.
- Implementation is dependent on customer acceptance --- early adopters have potential for big payoff.
  - In addition to power/performance gains, 3D can actually be lower cost!

Agenda

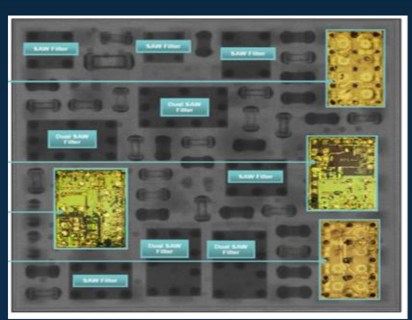
1	3D Scalability
2	14/7nm ASIC 2.5D application
3	14/7nm 3D Logic/Memory integration
4	3D RF FEM Integration
5	3D Ultra low power digital/mmWave
6	Summary and Next Steps

Why 3D/TSV for RF?

State of the Art RF FEM

Advanced RF FEM

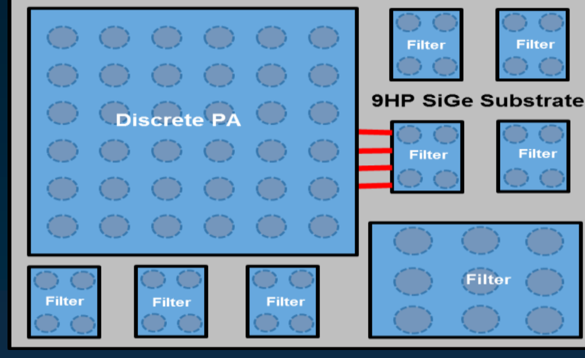
Multi Chip LGA / QFN



✓SiGe or RFSOI
✓Higher Performance
✓Higher Integration
✓Lower Power
✓Smaller Footprints

Industry Concerns

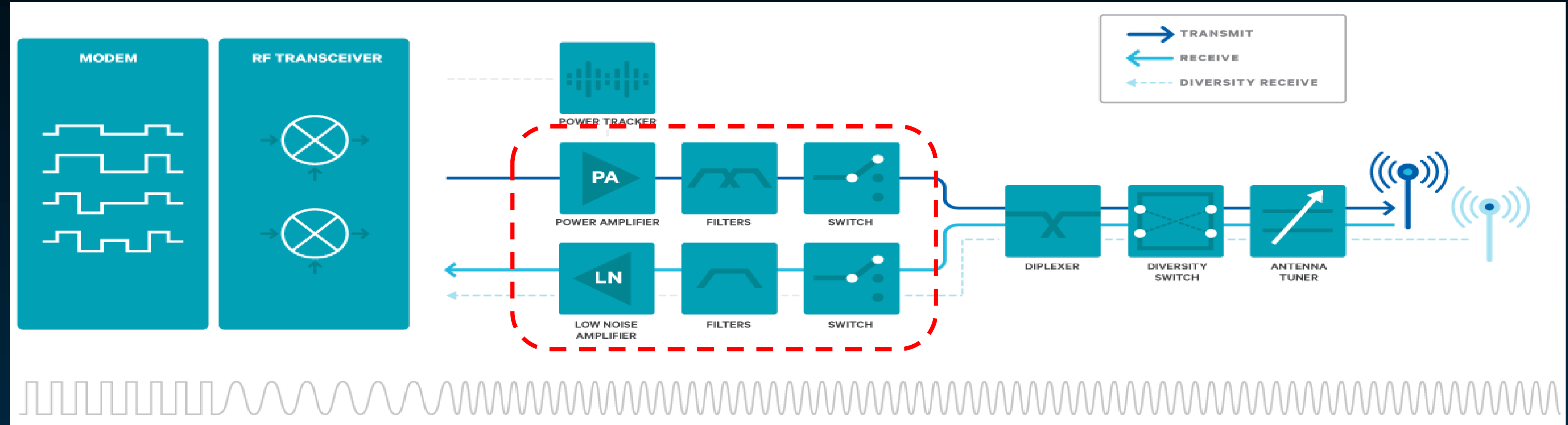
- Cost Comparison
- Electrical Performance
- Thermo-mechanical Reliability



3D/TSV Module

3D/TDV RF Module Basics

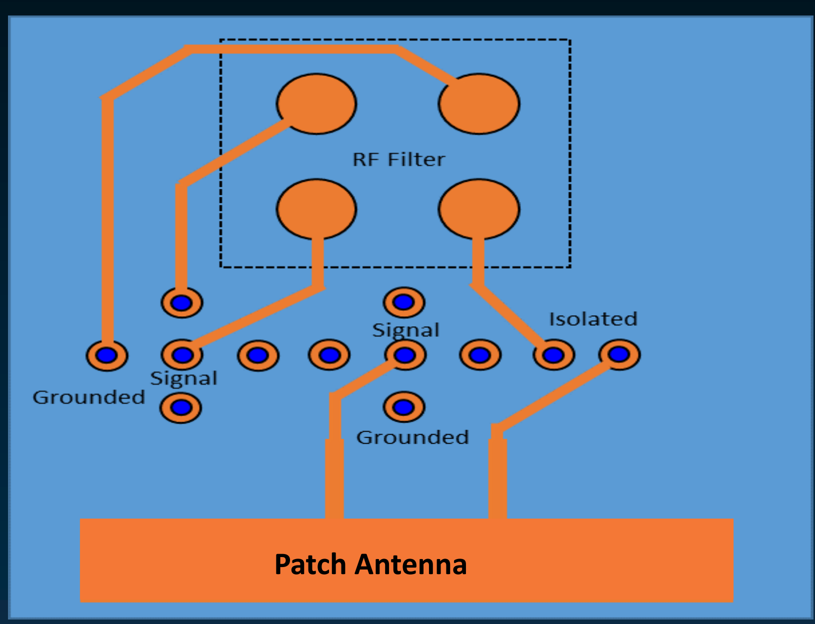
Cellular Front End Architecture



Higher frequency allows increasing integration levels on SOC and package

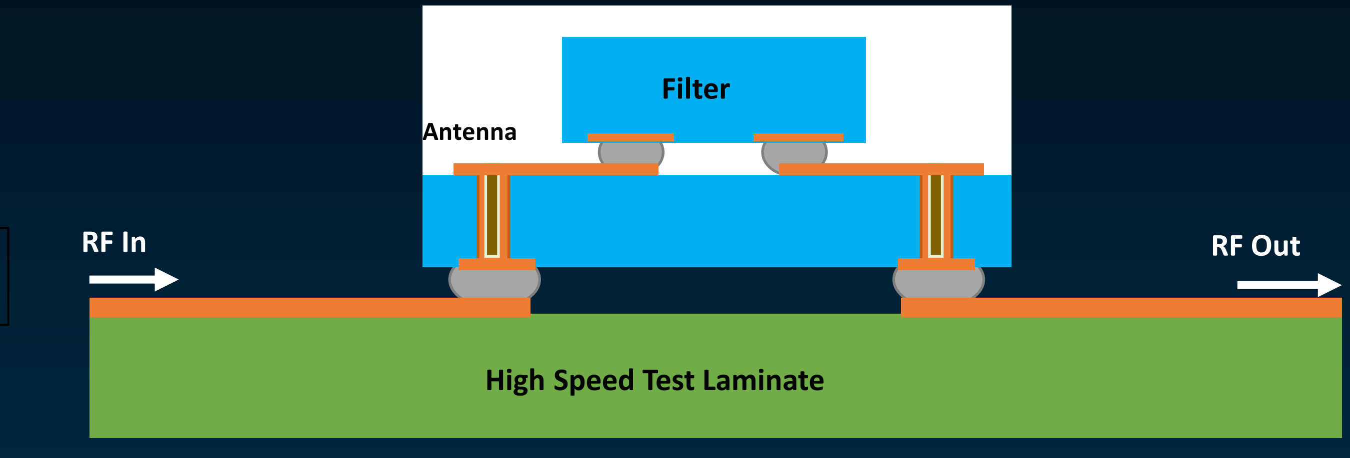
- Design verification for the critical RF Path.
- Significant Package Shrinkage
- Improved Electrical Performance with Lower Power Consumption
- Size and Cost reduction
- 100GHz Capability

3D/TSV Test Vehicle Design



3D/TSV RF Module

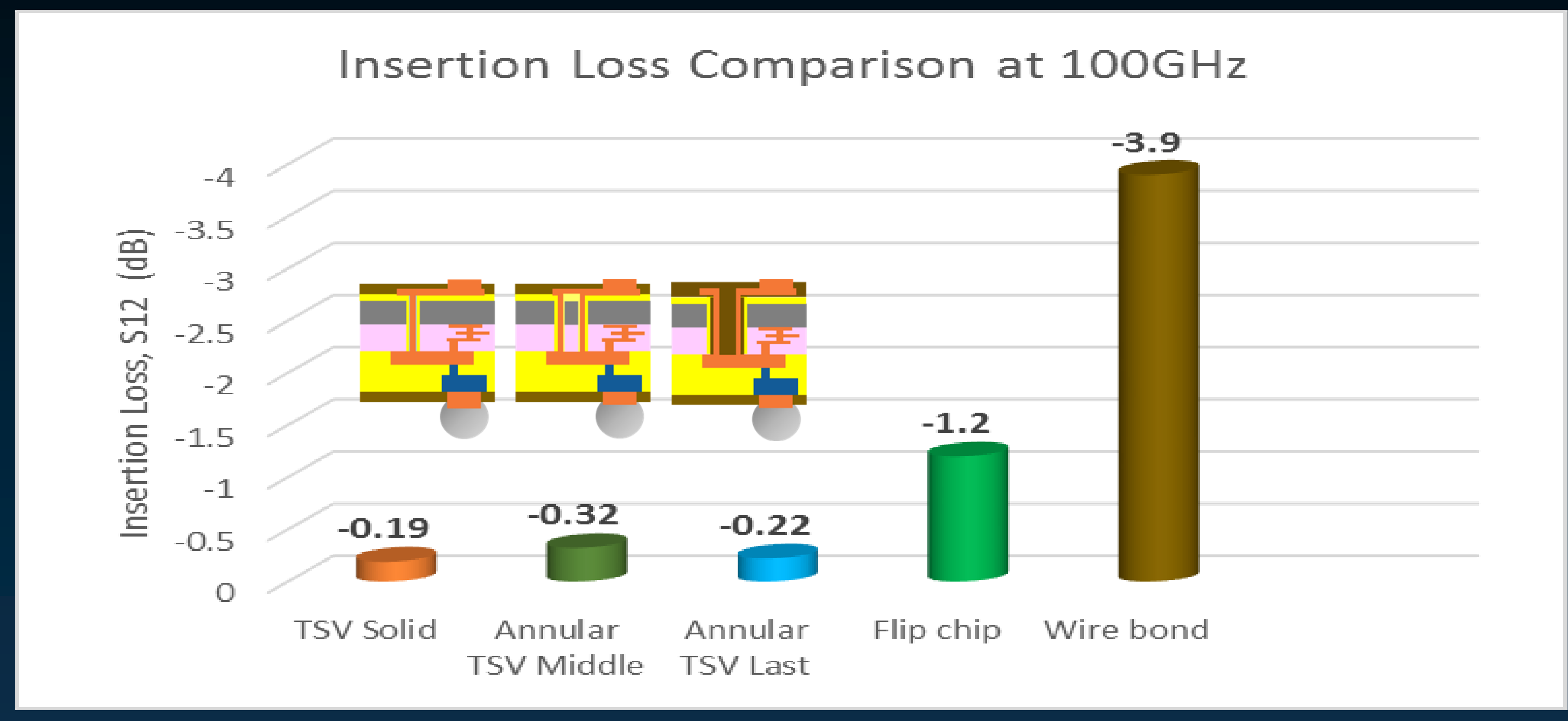
Signal Generator



Targeted Data

- TSV Capability
- 3D Capability
- Electrical Capability

3D/TSV High Speed Modeling



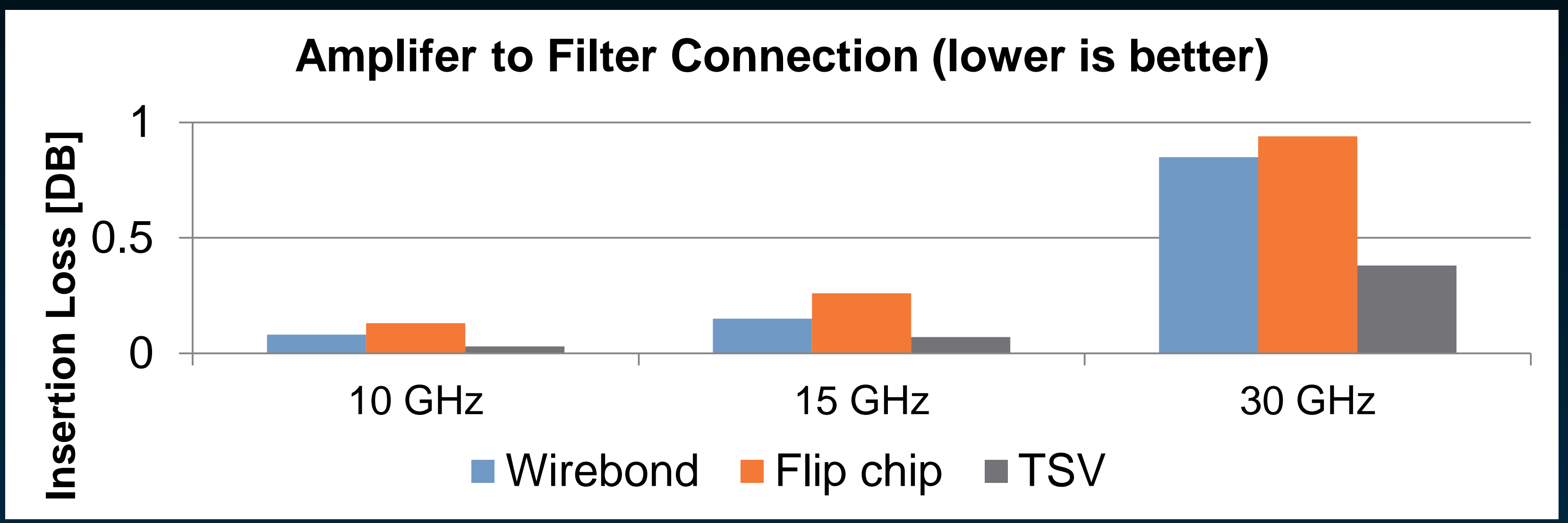
Source: Lane Ryne, Honeywell (Wire bond)

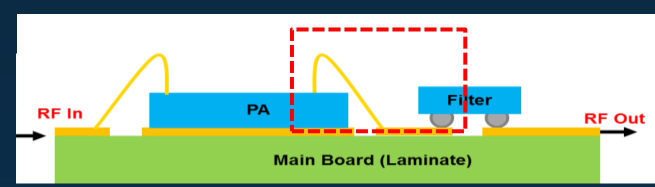
<u>Insertion Loss (S12) Comparison</u>

- All Three TSV Insertion Loss at 100GHz are comparable to Flip Chip Interconnection

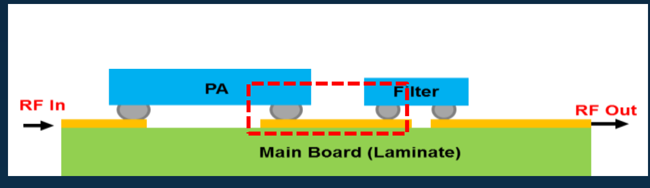
3D/TSV Die Stack Modeling for Amplifier to Filter

- ✓ **3D/TSV Performs better than Conventional 2D Flip chip and Wire bond Chip on Laminate**

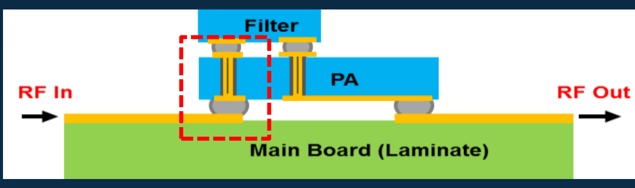




2D Wire bond chip on Laminate



2D Flip chip on Laminate



3D/TSV Die Stack

3D RF Module

- All of these numbers could probably be improved with additional optimization effort
  - TSV superiority tied to elimination of 1 mm of microstrip, more compact designs will see reduced benefit.
- Conventional 5x wirebond looks to outperform single flip chip for this design, but is in turn outperformed by TSV
  - Multi-C4 solutions not explored
- Return loss probably limits bandwidth in all cases
- Based on projections TSV should have better noise immunity, higher energy efficiency, and stable operation up to 30 GHz

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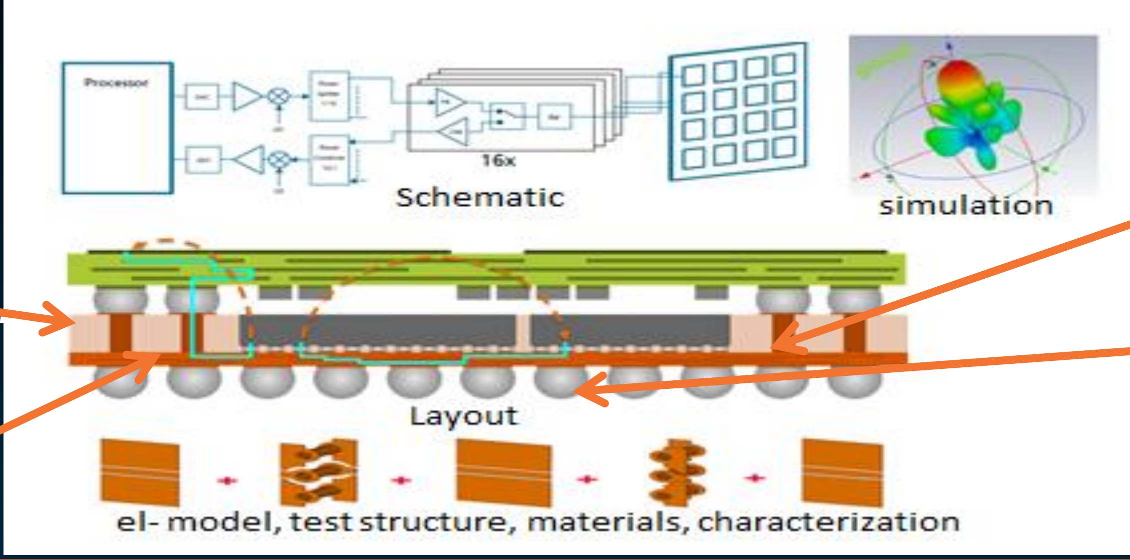
3D WLP Packaging Demonstrator (GF 22FDX technology)

EDA Plattform:
SiP level
DRC/LVS/PEX

Low Loss Mold Material

High Q Inductor
Thick Cu waveguide



Capacitor
Resistor
Splitter

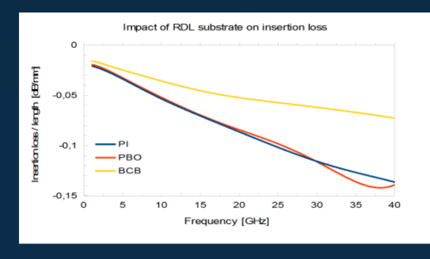
RF Test
at wafer level

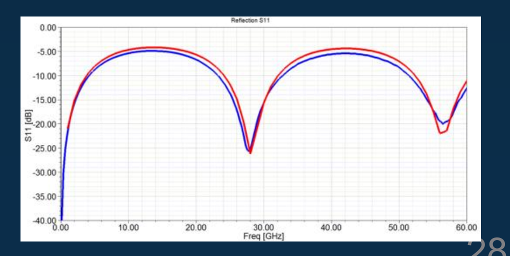
Cross Section
GF´s HDFO

RF Turnkey Value Proposition

- ❑ Significant area and thickness reduction
- ❑ No substrate. Simpler BOM
- ❑ Si/package co-design
- ❑ One stop shop turnkey solution: Si + package + test

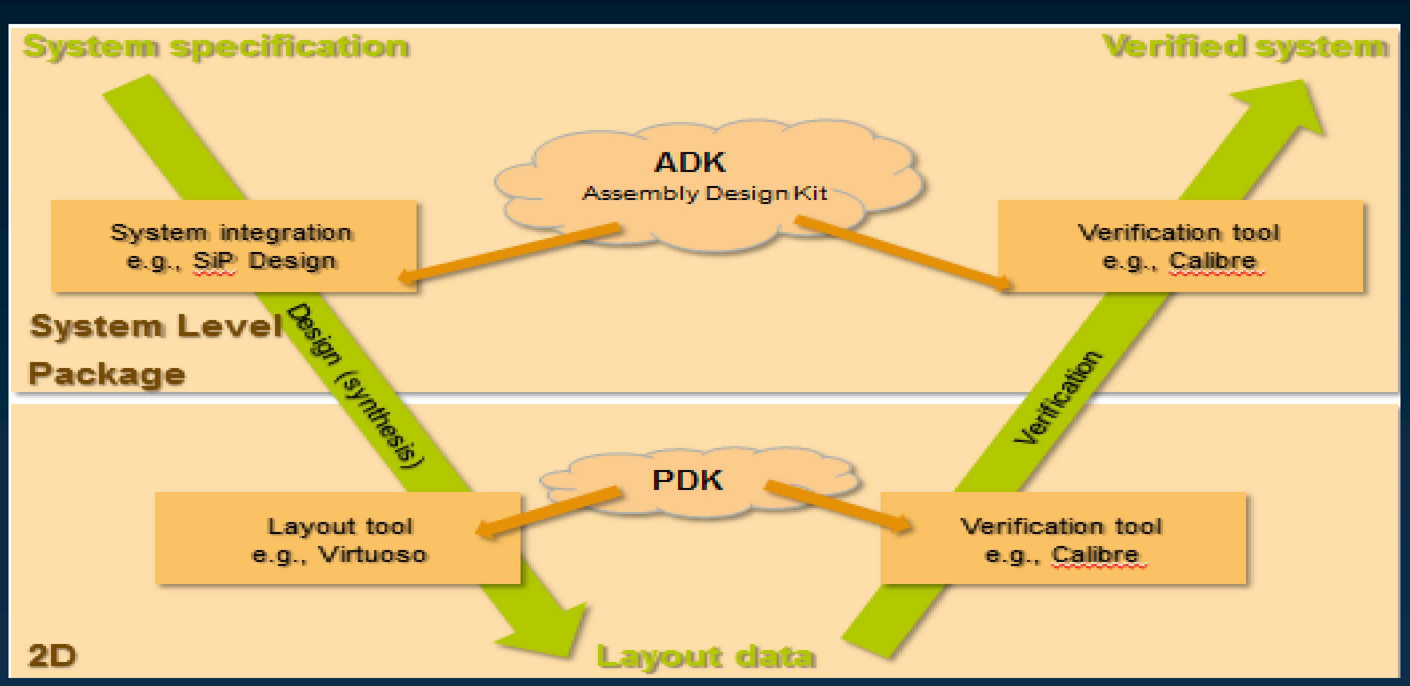
Less Than 0.15 dB/mm loss (microstrip line)





EDA platform: Design for 3D

- Introduction and realization of an integrated Design Kit (ADK)
- Extension of chip Process Development Kits (PDK) to package (PDK-A)
- Integration based on automated GDS merge and ITDB hierarchical data structure
- Digital on top flow (80% of design digital, 20% RF/mmWave)
- Not depended form EDA tool vendor, different PEX tools integrated (i.e. ANSYS, CST)

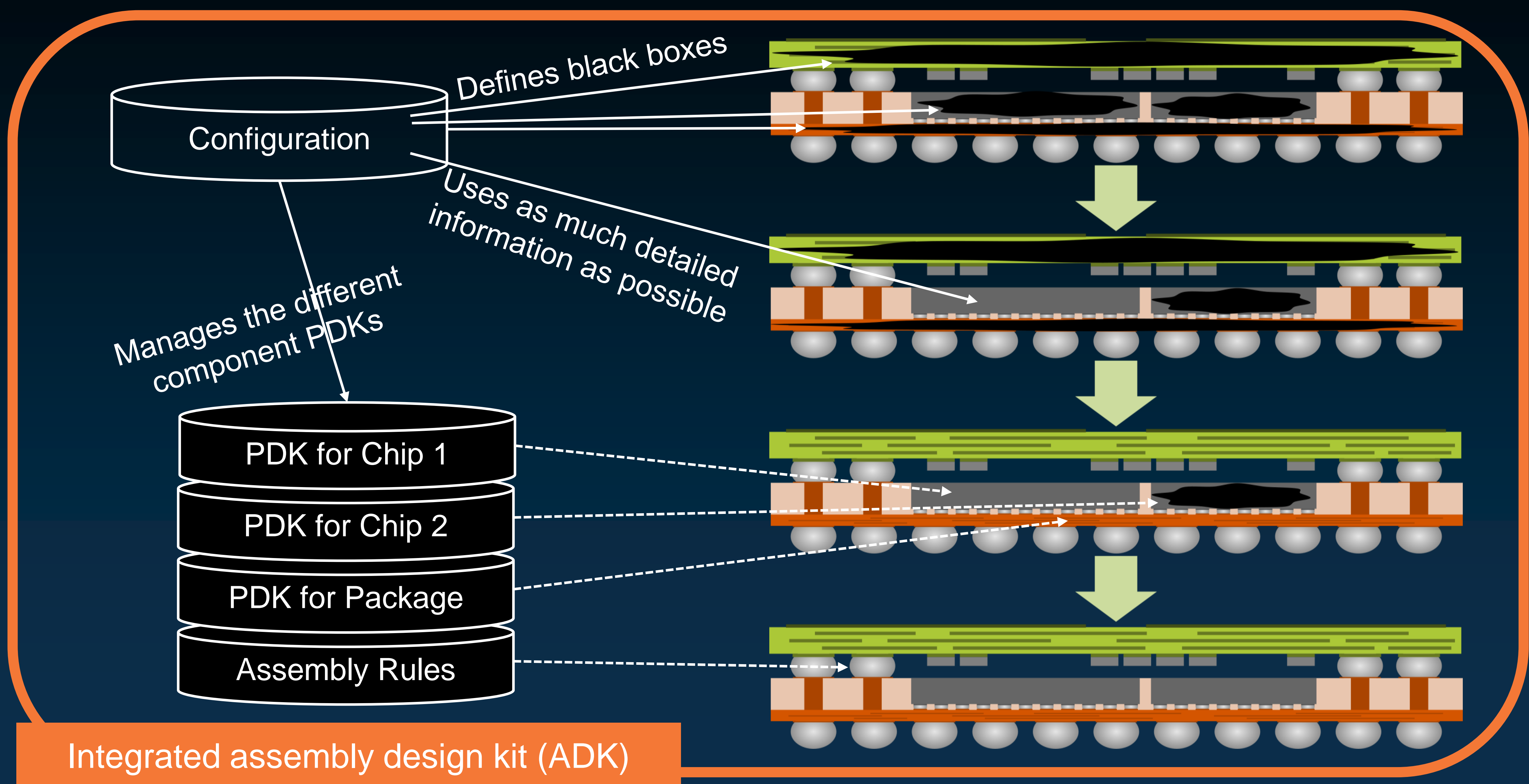


7 step co-design method:

1) Design in layout tool (Virtuoso)*
2) Export GDS chip and package*
3) Merge GDS chip/package*
4) Import merged GDS
5) Run SiP level DRC (Calibre)
6) Run SiP level LVS (Calibre)
7) Run el-simulation (Ansys / CST)

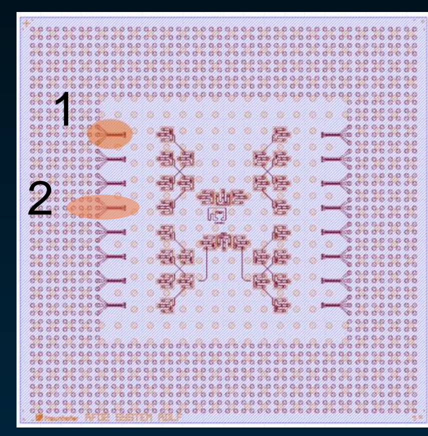
* 1)-3) can be merged ,i.e. design the SiP in one step (chip + package)

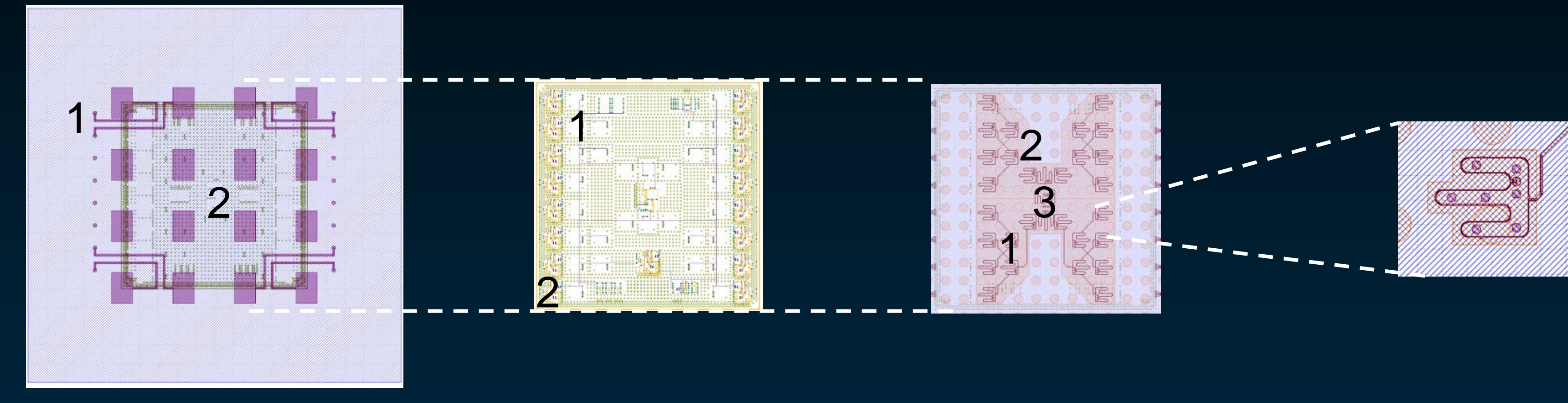
Black Box Concept – Incremental Design Closure



Benefits for using integrated 3D design kit

Co-Design Kit/ADK enables:





3D Package	3D Antenna	Chip	Chip + RDL	P-Cell/Splitter
1 Removed ball	1 16xpach feeding	1 Cu-Pillar Pitch	1 No core voltage balls	1 Cu-Pillar position
2 Low loss CPW	2 60GHz patch location	2 CPI rules	2 Reduction of shield	2 50ohm chip termination
		Voltage drop < 10%	3 Co-located structure	Optimized chip BEOL

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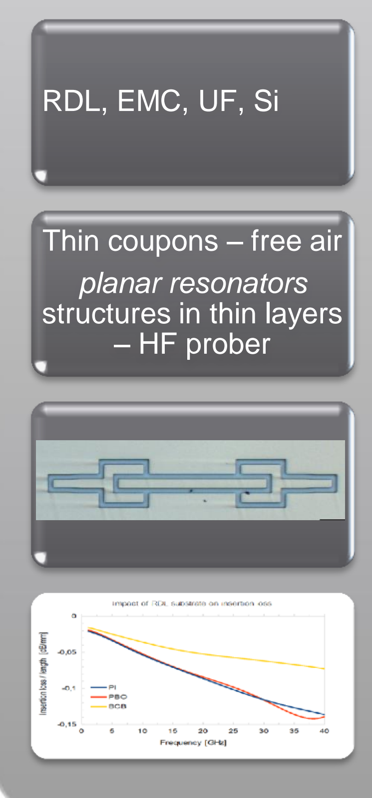
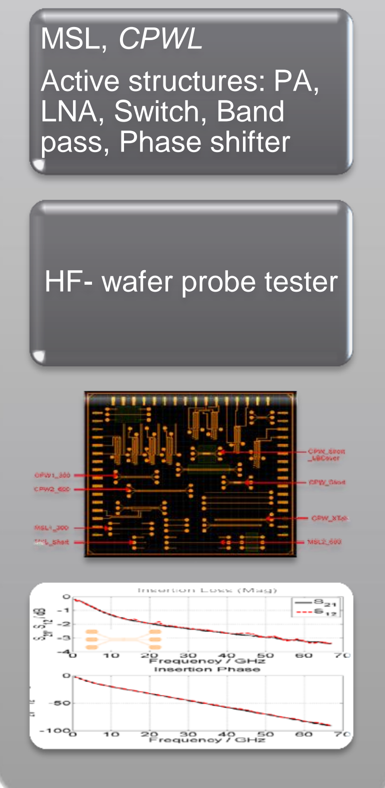
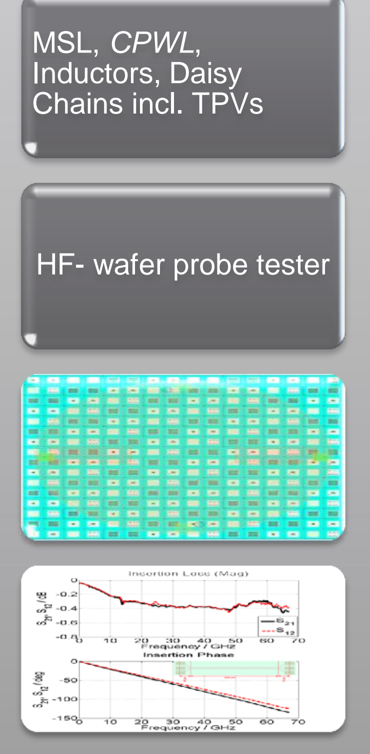
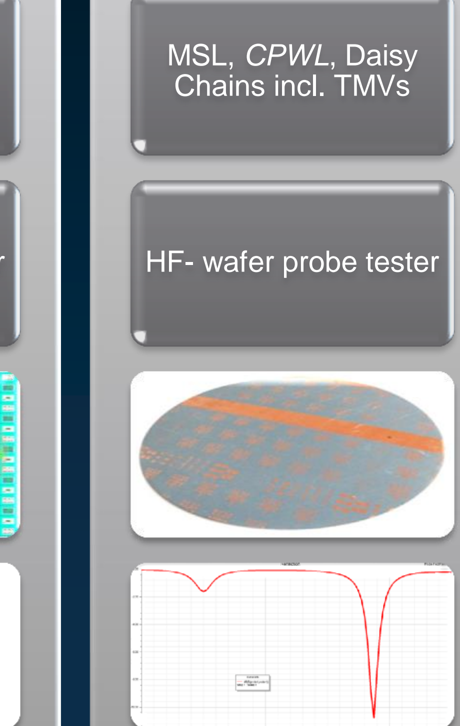
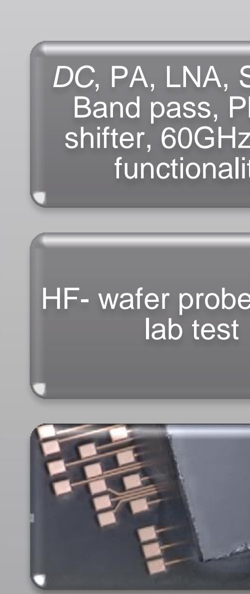
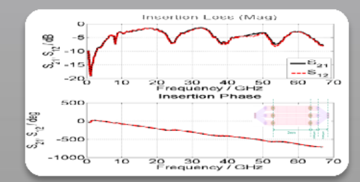
Co-design Concept Deployment

ADK	Material characterization	Chip Design Evaluation	Package Evaluation	IP Component	System evaluation
Structure / Elements for Evaluation	RDL, EMC, UF, Si	MSL, *CPWL* Active structures: PA, LNA, Switch, Band pass, Phase shifter	MSL, *CPWL*, Inductors, Daisy Chains incl. TPVs	MSL, *CPWL*, Daisy Chains incl. TMVs	*DC*, PA, LNA, Switch, Band pass, Phase shifter, 60GHz WiFi functionality
Methods	Thin coupons – free air *planar resonators* structures in thin layers – HF prober	HF- wafer probe tester	HF- wafer probe tester	HF- wafer probe tester	HF- wafer probe tester, lab test
Design/ Structure (example)					
Results (example)					

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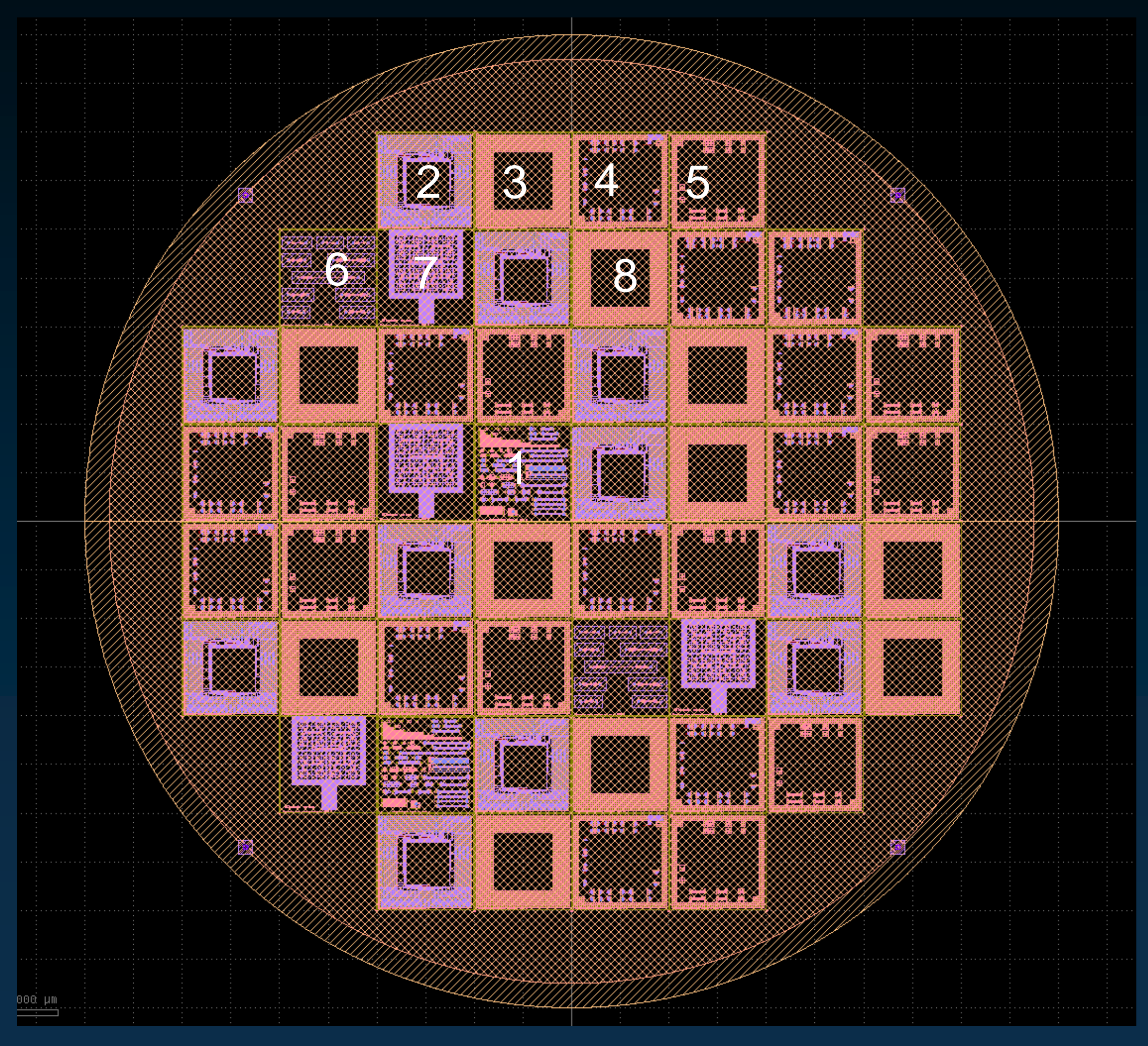
20-110 GHz: Examples of ADK characterization/validation

Multiple design test pattern:

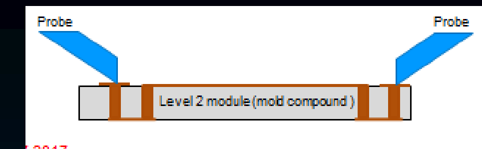
1. Allow RF structure characterization up to 110GHz
2. Characterize RDL and antenna dielectrics
3. Test package elements
4. LDI-structured laminate on 300(500)µm mold wafer

Mask elements:

- Test field: 1
- Test field: 2
- Test field: 3
- Test field: 4
- Test field: 5
- Test field. 6
- Test field. 7
- Test field. 8

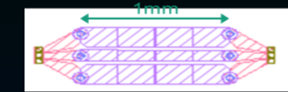


Examples of ADK characterization/validation

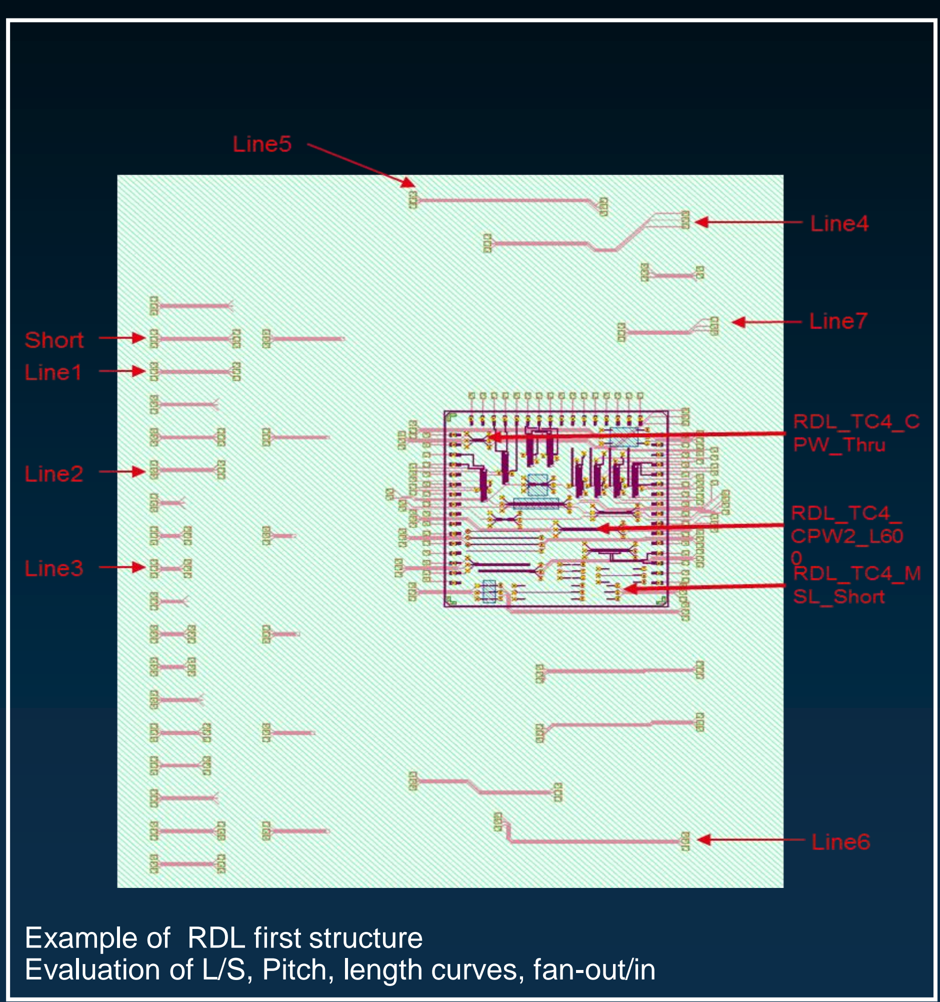


Package test site	Test plan 20-110GHz	Results
	- RF test pattern for **transmission lines**, **TMVs** (shielding, cross talk) - Varying pitches, L/S - TMV daisy chains – D/C - Probing on top - RF-characterization up to 110GHz	• s-parameter measurements • de-embedding for characterization of single structures • R for daisy chains • Wafer prober (from MPI) and Rhode&Schwarz Vector-Network analyzer
	- Patch-Array Antenna with Shield on bottom - 53GHz – 67GHz: Mold with one top and one bottom layer (RDL)	• Using an antenna characterization equipment [Rhode&Schwarz Vector-Network analyzer] to analyze antenna performance, measure shape of radiation pattern • Characterization of thermo-mechanical behavior of antenna package

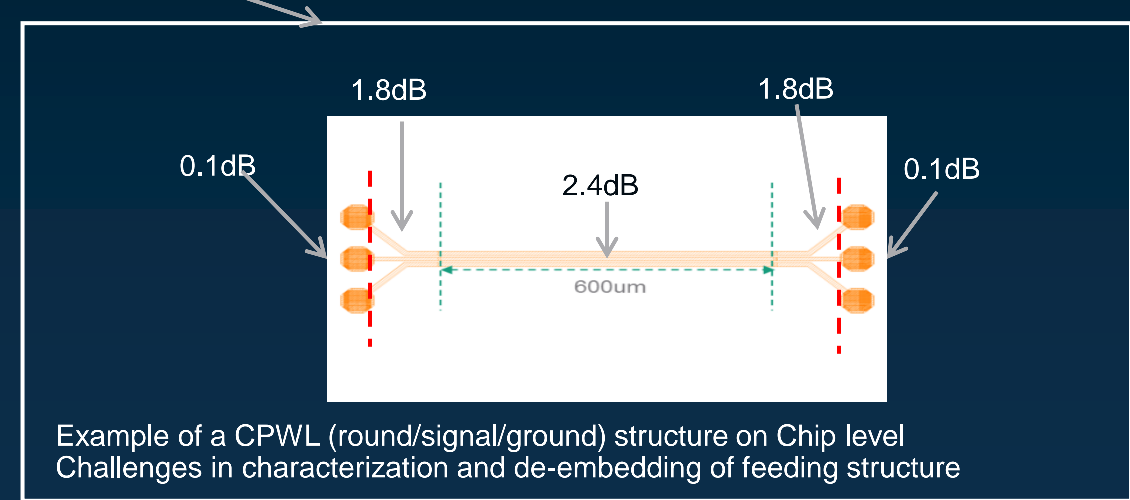
Co-design Concept Deployment: Electrical Characterization



F	Die level* [dB/100µm]		Interconnects** [dB/ element]			RDL first [dB/1mm]	Mold level [dB/1mm]
	CPW	MSL	TMV pitch 250µm	TMV pitch 400µm	CuP Pitch 100um	CPW	CPW
30GHz	0.2	0.6	0.5	1.75	0.8	0.26	0.2
60GHz	0.4	1	0.75	2.25	0.1	0.5	0.25



Example of RDL first structure
Evaluation of L/S, Pitch, length curves, fan-out/in

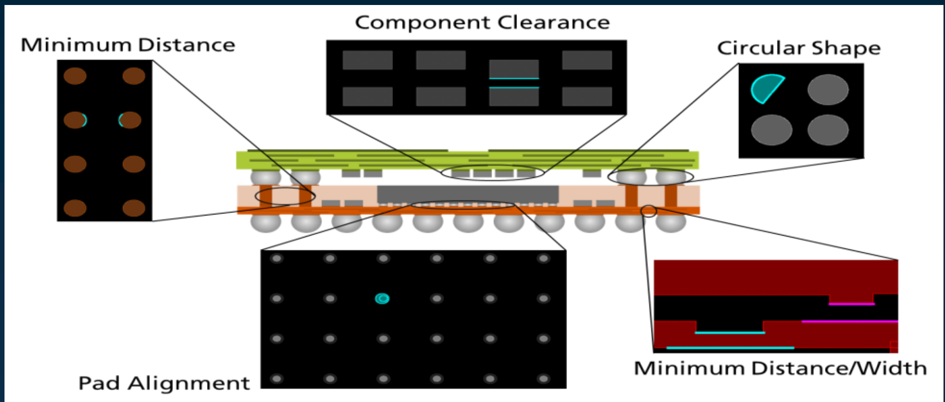


Example of a CPWL (round/signal/ground) structure on Chip level
Challenges in characterization and de-embedding of feeding structure

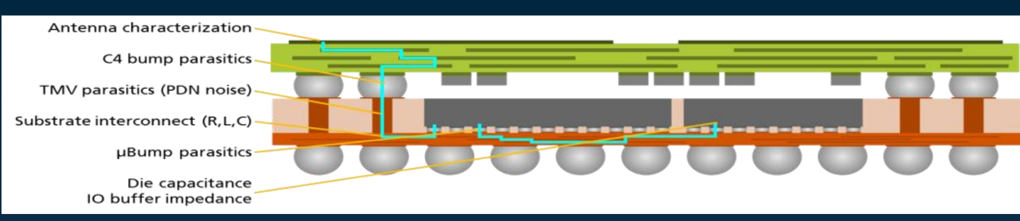
RF performance is depended on design, material and needs electrical models for chip and package

Co-design Concept Deployment: Design Flow – DRC/ LVS & PEX

- Brakes the wall between chip and package design and allows a smooth interaction between both worlds
  - Vendor independent overall DRC and LVS
    - Allows DRC also between package and chip elements to check the correct alignment
    - Allows LVS for chip and package elements – package elements are also checked



- Merging chip and package design allows smooth interaction and improves system level performance
  Parasitic extraction
  - Enables extraction tools e.g. HFSS, CST
  - Allows parasitic extraction from transistor to a package
  - Extends the predefined PDK models to package
  - Models for interconnects, antennas, inductors, …
  - Description of a 3D path by concatenation of models
  - Allows pre-layout simulation to check e.g. the losses



Agenda

1. 3D Packaging Requirements
2. 14/7nm ASIC 2.5D application
3. 14/7nm 3D memory integration
4. 3D RF FEM Integration
5. 3D Ultra low power digital/mmWave (D43D)
6. Summary and Next Steps

3D Scalability from High Performance to Ultra Low Power

Low Power ---------- Performance

Application	Key Parameter	3D Architecture
Compute and Wired Network	Die size and power consumption of CPU, 112 Gbit SERDES, HBM for memory bandwidth	2.5D interposer
Compute/AI	SRAM Stack for more memory bandwidth, wafer level test	W2W, Hybrid Bond D2S → D2W
3D FEM	Insertion loss at 100GHz, Switch, PA, Filter	D2W, TSV last, overmold
5G/mmWave	Die Size < 10mm^2, DSP+FEM on SOC	3D WLP, MCM, AoP
IoT/Sensor	< 5mm^2 Ultra Low Power, low noise, IP compatible with sensor modules	W2W (no TSV), 3D WLP

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Thank you!

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Conclusion

- High Performance application continue to use 2.5D
  - Development underway
  - AI will drive direct bond (W2W and D2W) with SRAM
  - 3D will bridge high performance and low power
- Low Power 3D, multiple technologies can do
  - Technology selection on performance at affordable price.
  - Design cost play a significant role
  - Optimization and integration efforts play a key role
  - Opportunity for Europe/China with automotive and industry 4.0
- 3D Design automation and reference flow development is key

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