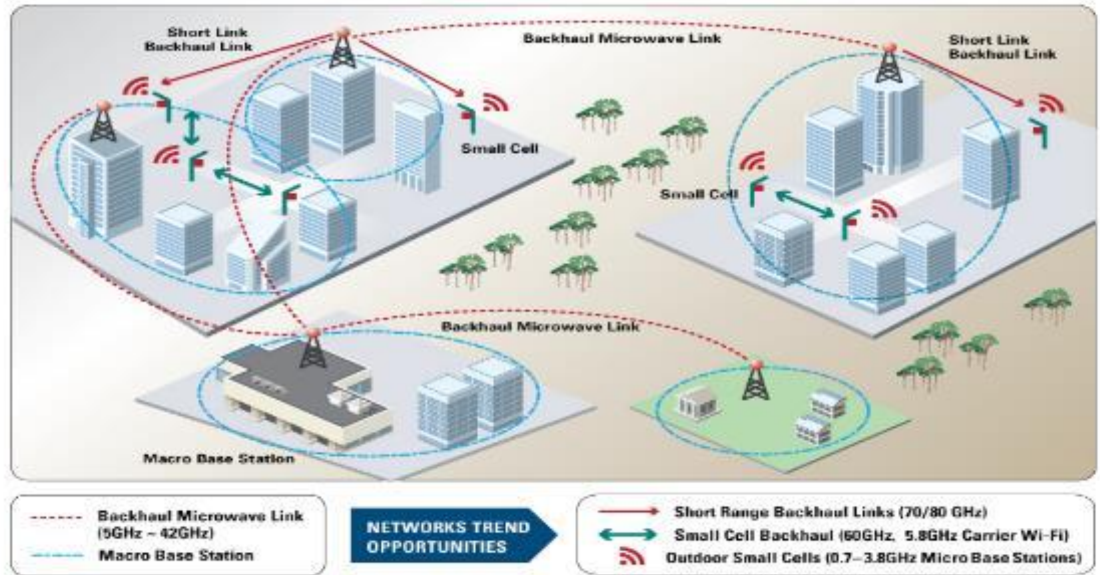
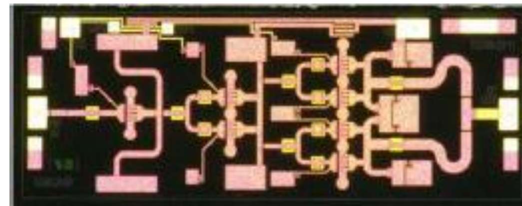


5G_GAN2 ECSEL PROJECT: 200mm CMOS COMPATIBLE GaN/Si HEMT FOR KA BAND POWER AMPLIFIER

CEA LETI| Hervé RIBOT | 26/06/2018



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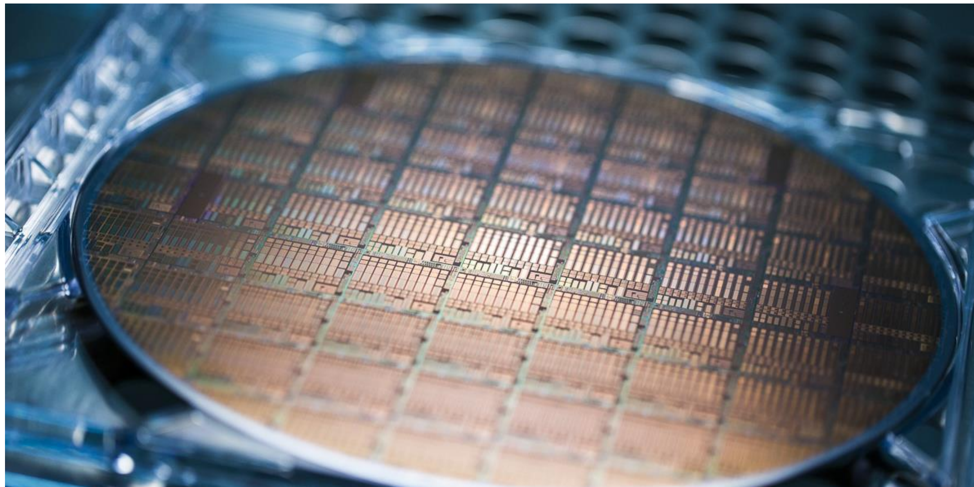
KEY OBJECTIVES

- **Leveraging LETI platform on 200mm N_{on} power transistors to accelerate R&D of Ka band RF transistor on GaN/Si:**
  - TRL: 1 → 4 in 3-year program
  - Target performances: 30 GHz CW 3W/mm, gain>14 dB, PAE >45%. Cost/mm^2 to be confirmed, but <1/4 that of similar device on 4'' GaN/SiC



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MOTIVATION

- **Cost reduce High performance PAs for 5G systems and ultimately, facilitate SIP integration:**
  - 200mm CMOS foundry compatible
    →Larger number of PAs per wafer
    →Better uniformity and higher process yield
    →Better equipment uptime
    →No dedicated line required (fabless/fablight business model can be implemented)
  - Other CMOS opportunities:
    →Leverage Si implantation for ultra low resistance contacts and access regions
    →Leverage CMOS gate know-how for mmWave PA
    →Explore Film transfer on optimized HR substrate (ceramics…) for improved RF and/or thermal performance (derived from LETI activity on advanced substrated with Soitec)
    →Leverage 3D/TSV technology on Si (more mature than on SiC) for easier SIP integration.
  - CMOS compatibility constraints: Si substrate not as good thermally as SiC, more mismatched (17% vs 3,5%), No gold , No lift-off.

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LETI TEAM FOR WP2 AND MAIN STAKEHOLDERS

LETI Team lead engineers:

- Device Engineering: **Erwan Morvan** (erwan.morvan@cea.fr)
- « CMOS compatible »Process Engineering and WP2 key contact: **Yveline Gobil** (yveline.gobil@cea.fr)
- 200mm GaN/Si MOCVD : **Matthew Charles** (matthew.charles@cea.fr)

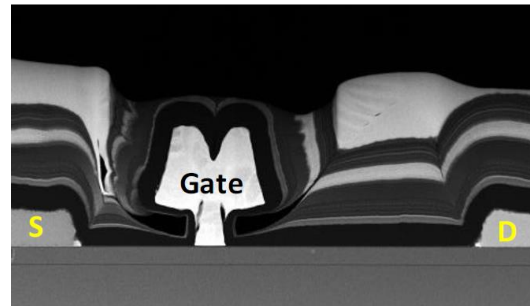
Main stakeholders:

- Ericsson, Thales CS & TESAT: Expecting Systems cost savings
- UMS: Expecting access to cost effective/ high volume PA Product line
- Xfab as a potential 200mm foundry for GaN/Si HEMT.
- III-V Lab as R&D partner for RF design and testing of PA + comparison to GaN/SiC.
- CEA LETI Packaging Team: Post process of GaN/Si wafers for easier SIP integration
- UPadova: Assessment of GaN/Si HEMT robustness

KEY ACTIVITIES IN WP2 (FIRST SIX MONTHS)

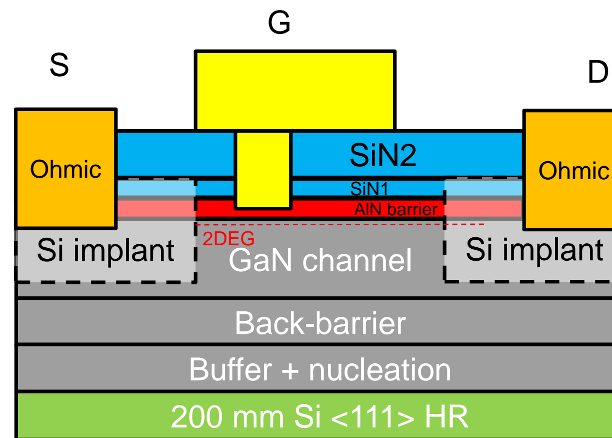
- **Epitaxy: Optimize MOCVD epitaxy of GaN on 200mm HR Si**
  - Use of in-situ SiN passivation
  - Optimize AlGaN and/or AlN barriers for improved Rsheet and robustness
  - Optimize their effective thermal boundary resistance layer (TBReff layer)
  - Reduce overall epilayers thickness and bow (20µm)

- **Validate LETI epilayer stack (GaN/Si) using III-V Lab existing GaN/SiC masks and front end process**
  - Epitaxial growth (MOCVD) of 200mm wafers in LETI
  - Dice 3" wafers into 200mm wafers
  - Process 3" wafers at III-V Lab using their masks and GaN/SiC process (gold contacts, mushroom gates by lift off)
  - Test of GaN/Si HEMT at LETI (DC) and III-V Lab (HF)



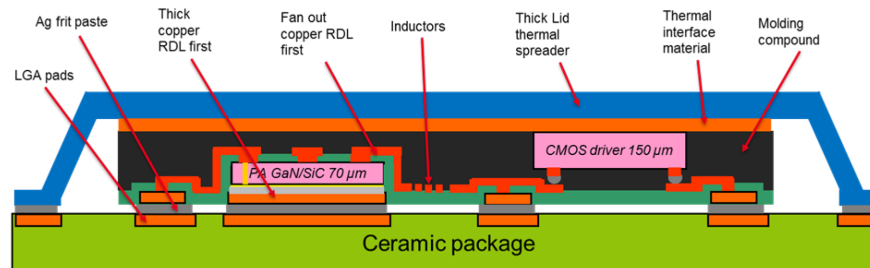
KEY ACTIVITIES IN WP2 (FIRST SIX MONTHS)

- **Very low resistance Si implanted layers (C-MOS compatible)**
- **Gold-free ohmic contacts with access resistance <0,1 Ω.mm through Si implantation process optimization**



KEY ACTIVITIES IN WP2 (LONGER TERM)

- **Leverage CMOS gate technology for mmW Power HEMT**
- **Establish a baseline process flow for 200mm CMOS compatible HEMT for Ka band (No gold, no lift off).**
- **Prepare for SIP integration, by taking into account Packaging team requirements**



- **Contribute to failure analysis process including electrical diagnostic and physical analysis (PFNC).**

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CONCLUSION

- LETI is leveraging its 200mm MOCVD epitaxy and HEMT technology platform for RF Power Amplifiers.
- LETI aims at bringing CMOS capability to the development of a cost effective GaN platform, ready for high volume manufacturing
- Benchmarking with GaN/SiC components all along
- NanoCharacterization Platform (PFNC) to contribute to characterization and failure analysis of GaN/SiC and GaN/Si devices after robustness testing.

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