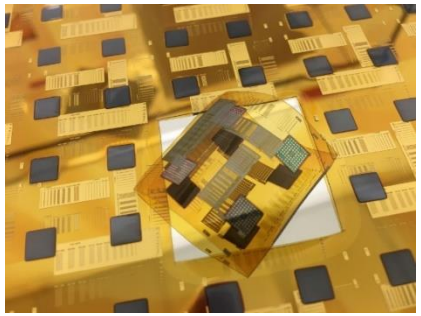
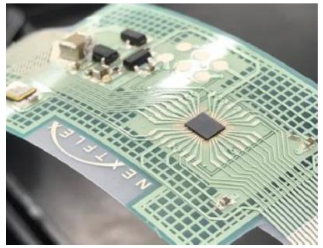


FLEX YOUR MEMS: INTEGRATING SILICON DEVICES INTO FLEXIBLES ELECTRONICS

Philippe Robert

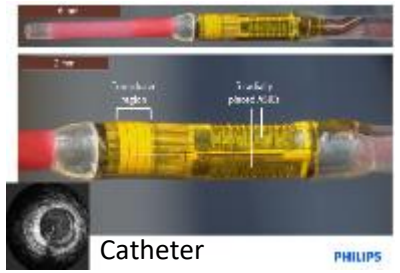
Leti MEMS Workshop, June 25 2019, Estrel Congress Center, Berlin

CONTEXT : ELECTRONIC ON EVERYTHING ⇒ THIN AND FLEXIBLE

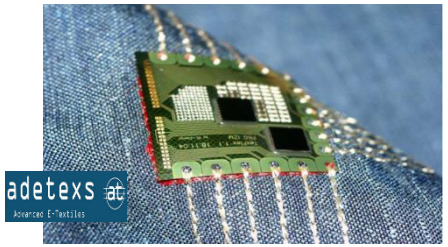


TempTraq's
Wireless Patch

- Electronic on human
- Electronic in textile
- Electronic on objet



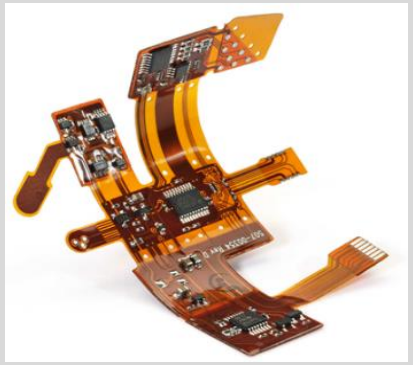
Catheter



TECHNOLOGIES FOR COMPONENT INTEGRATION ON FLEX

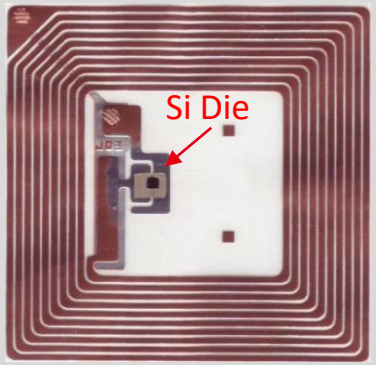
In production

Package on Flex



GC Aero Flexible Circuitry, Inc

Chip on Flex

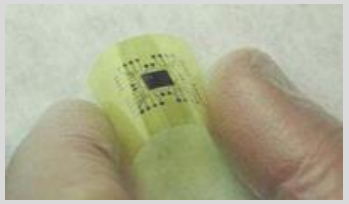


Tag RFID

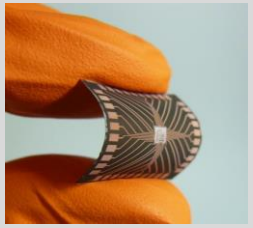
IC thickness > 120µm
Flexible only between components

In development

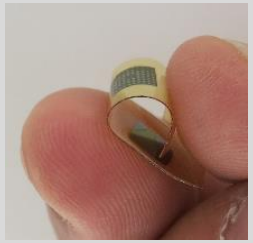
Embedded in Flex



imec



Fraunhofer EMFT



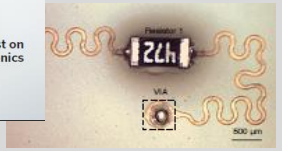
leti ceatech

IC thickness < 80 µm
Fully flexible (Silicon + substrate)

Stretchable electronic

UCLA

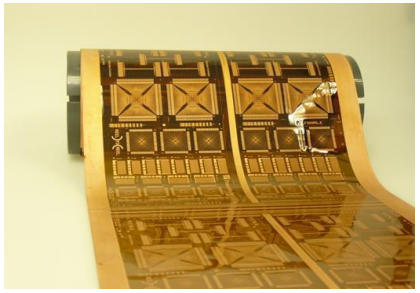
UCSD

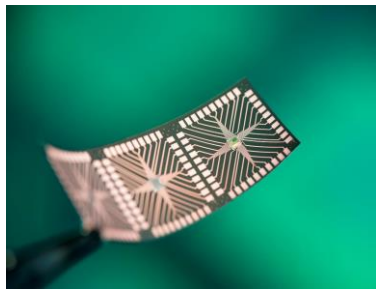


Stretchable only between components

TECHNOLOGIES FOR FLEXIBLE SUBSTRATE

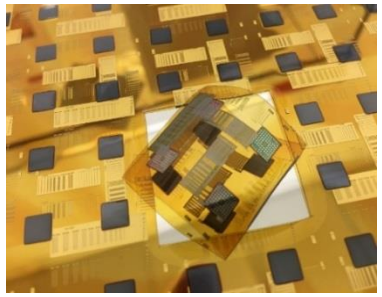
Roll to roll





Panel

Wafer

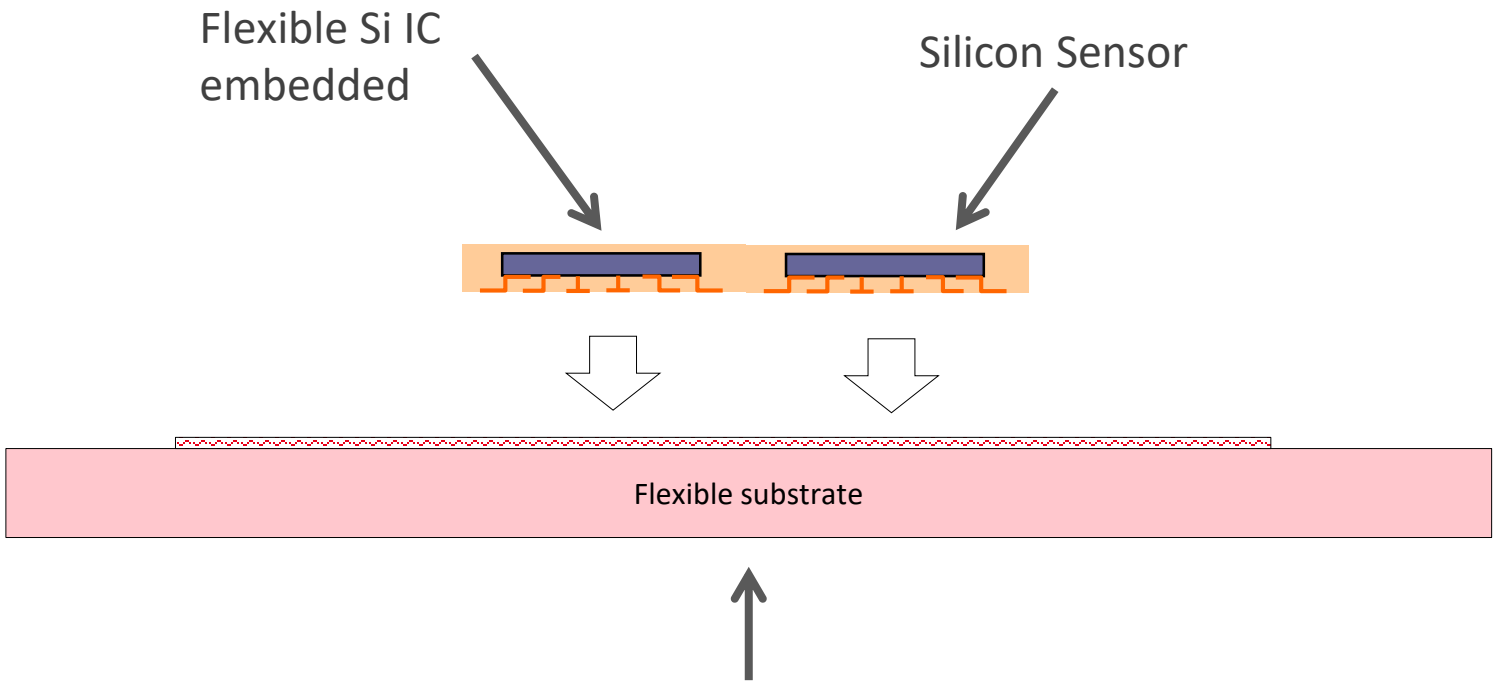


- Large device
- **Low resolution** pattern
  (100µm electrical line, positioning)
- Low cost
- High throughput

- Small device
- **High resolution** pattern
  (10µm electrical line, 1µm positioning)
- High cost
- Low throughput

OUR STRATEGY

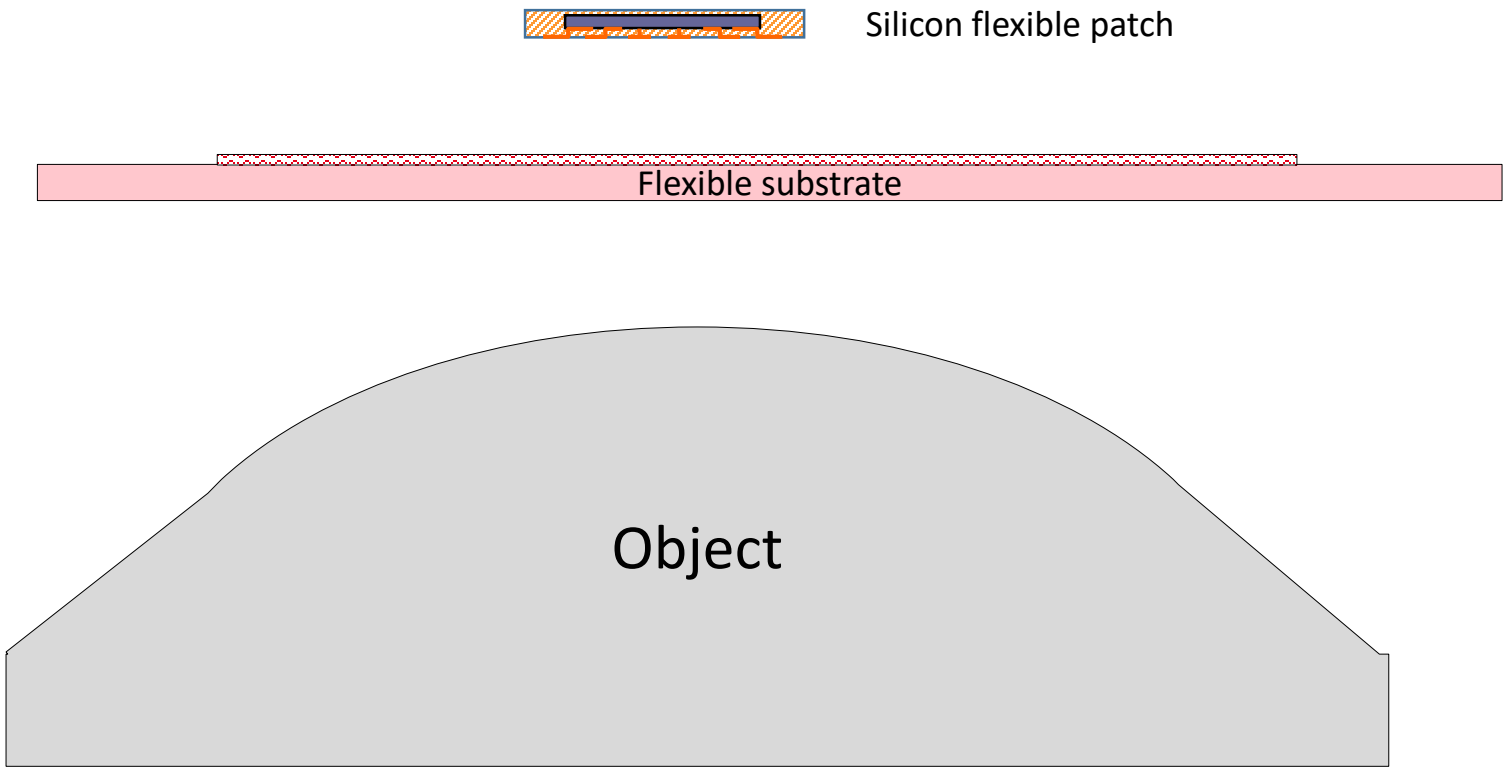
Hybrid Approach : High density flexible patch on Low cost flexible substrate



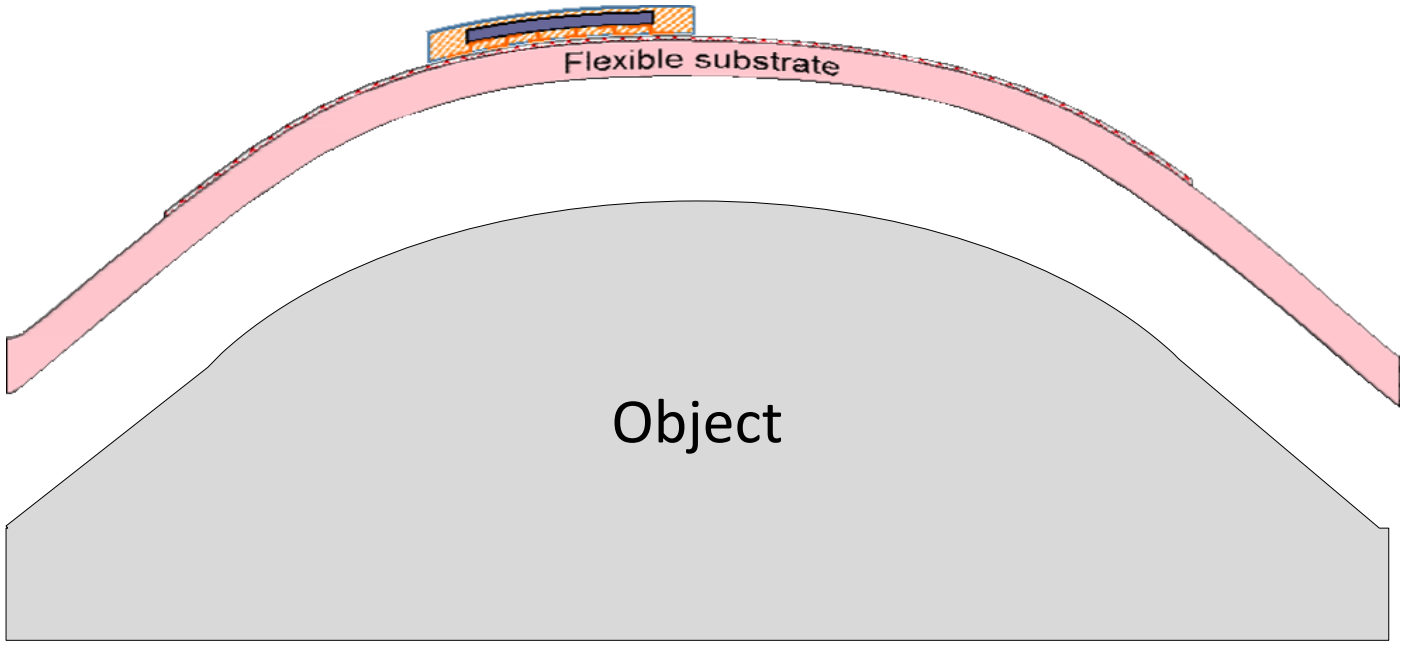
- Small area
- High resolution pattern

- Large substrate
- Low cost

CONFORMABLE ELECTRONIC



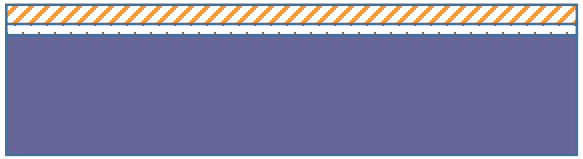
CONFORMABLE ELECTRONIC



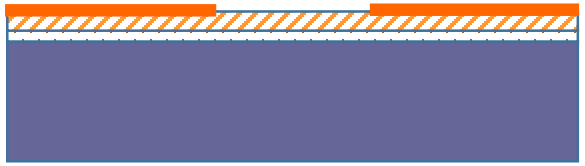
COLLECTIVE PATCH FABRICATION ON WAFER CARRIER

1- Wafer with sacrificial layer

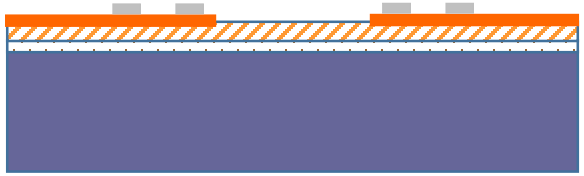
2- Coating with flexible layer



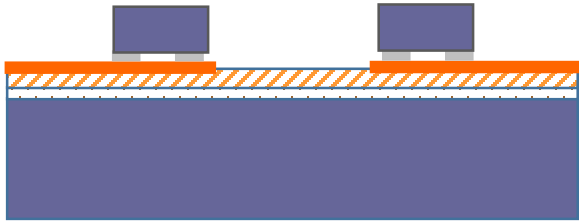
3- Deposition and structuration of metal



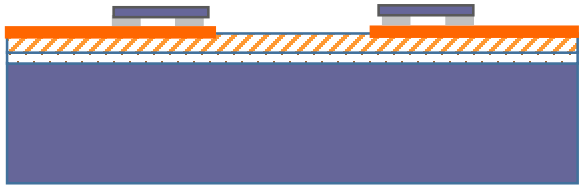
4- Deposition and structuration of pad



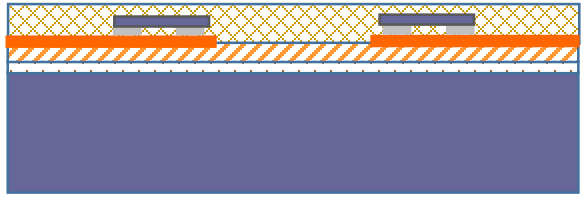
5- Dies Flip-chip bonding



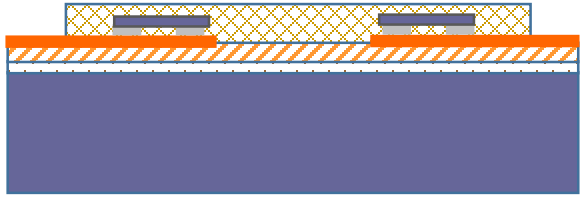
6- **Collective** Dies thinning



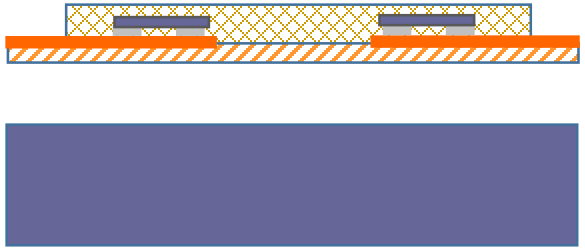
7- Coating with flexible layer



8- Flexible layer etching

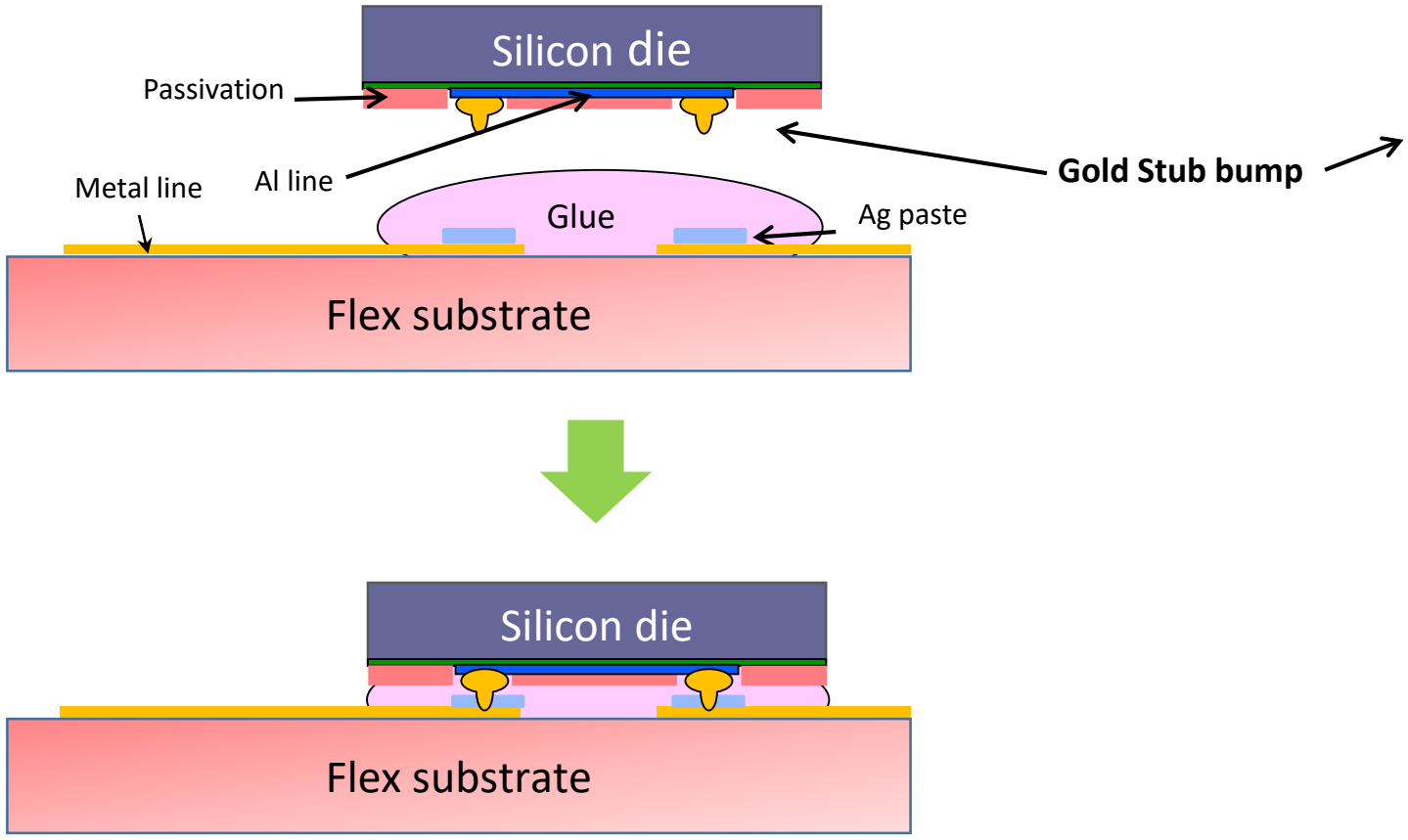


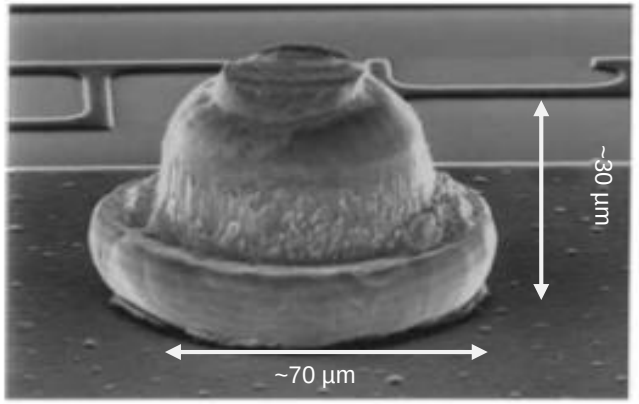
9- Separation from carrier



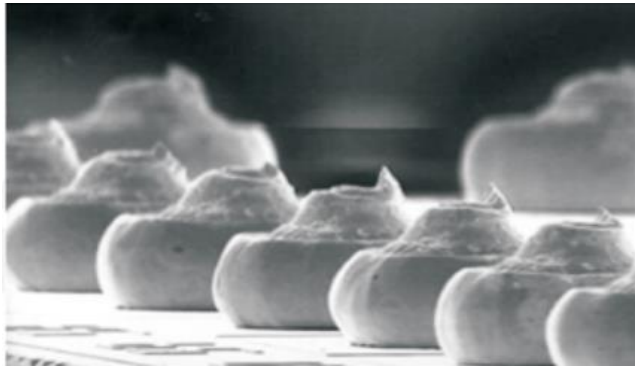
COLLECTIVE DIE ASSEMBLY ON WAFER CARRIER

- **Interconnection using Gold Stud bump on die**
- **<u>Collective</u> bonding by <u>low temperature</u> thermo-compression and glue (< 150°C)**



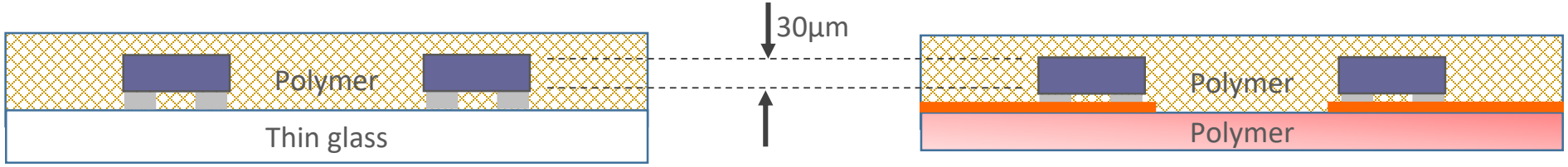


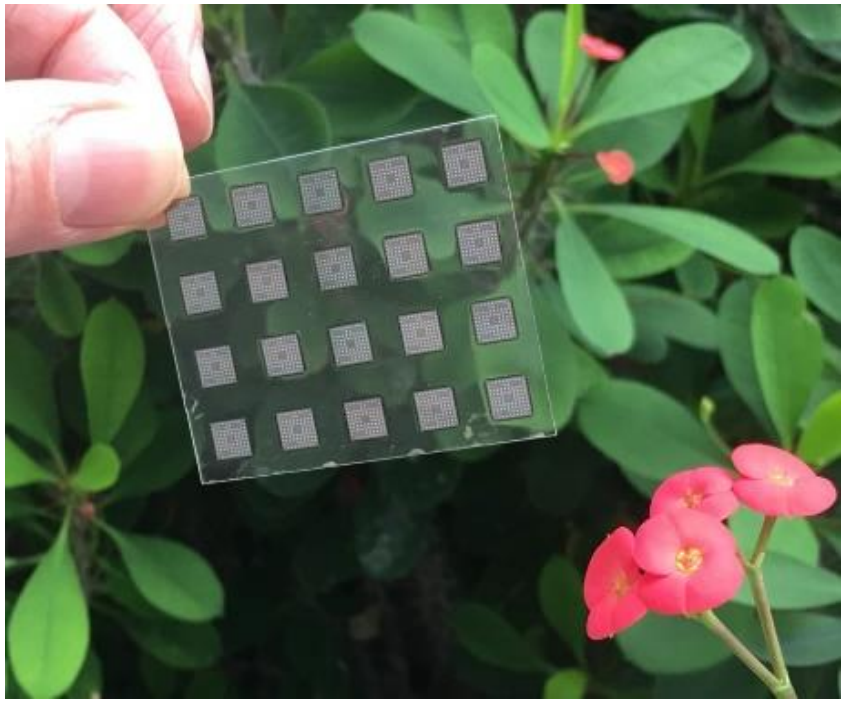
Accubump *Hybrid SA*



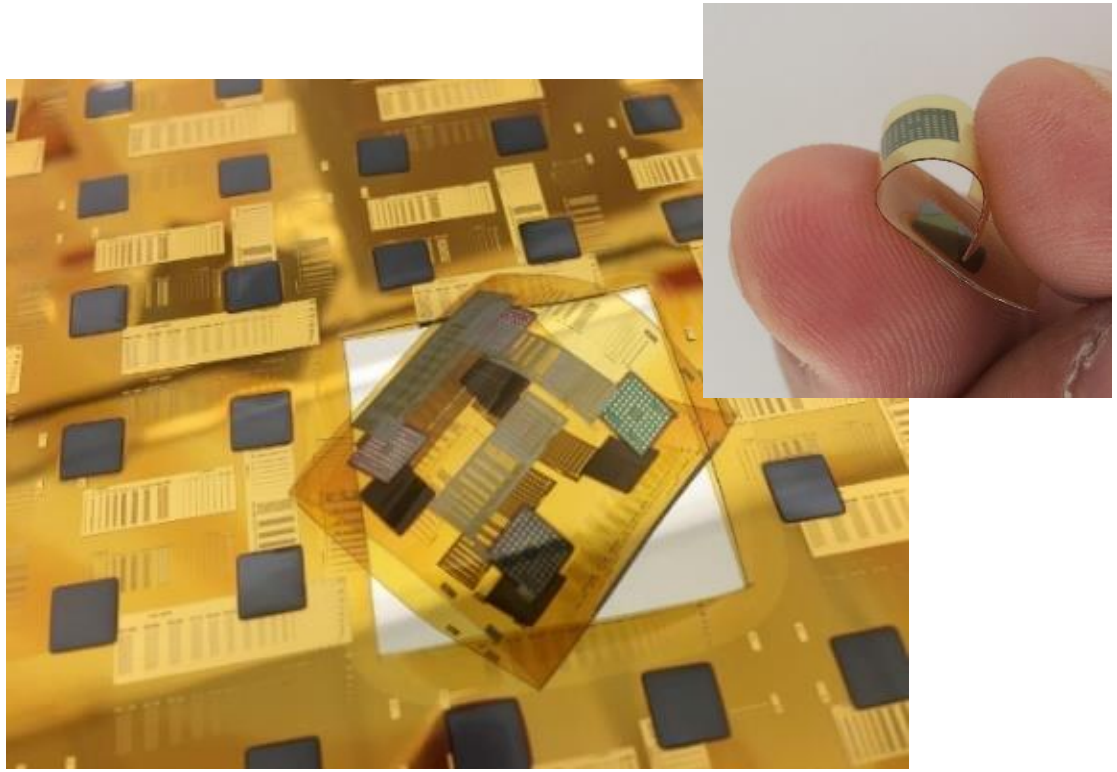
Hybrid SA

PATCH DEMONSTRATORS





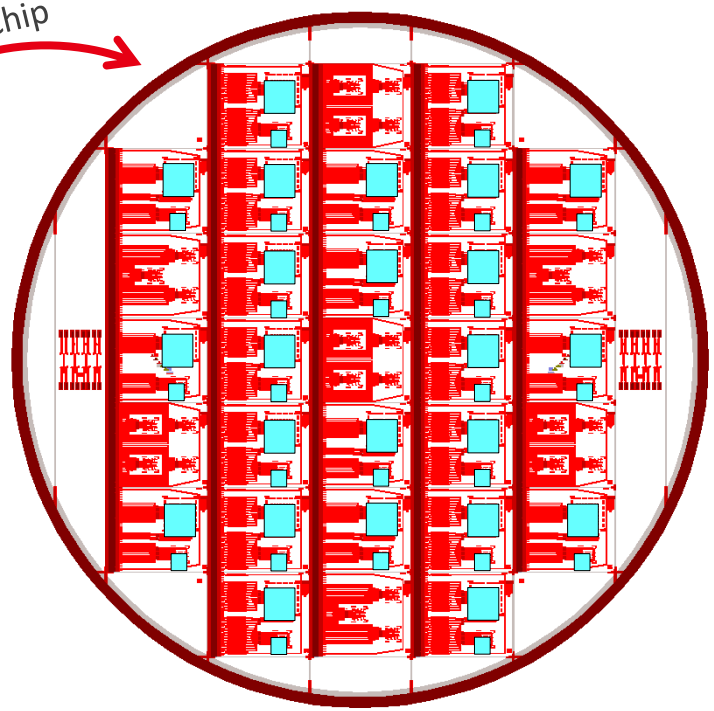
Polymer-glass film incorporating silicon chips thin down to **30µm**



Polymer-polymer film incorporating silicon chips thin down to **30µm**

ELECTRICAL PATCH TEST VEHICLE

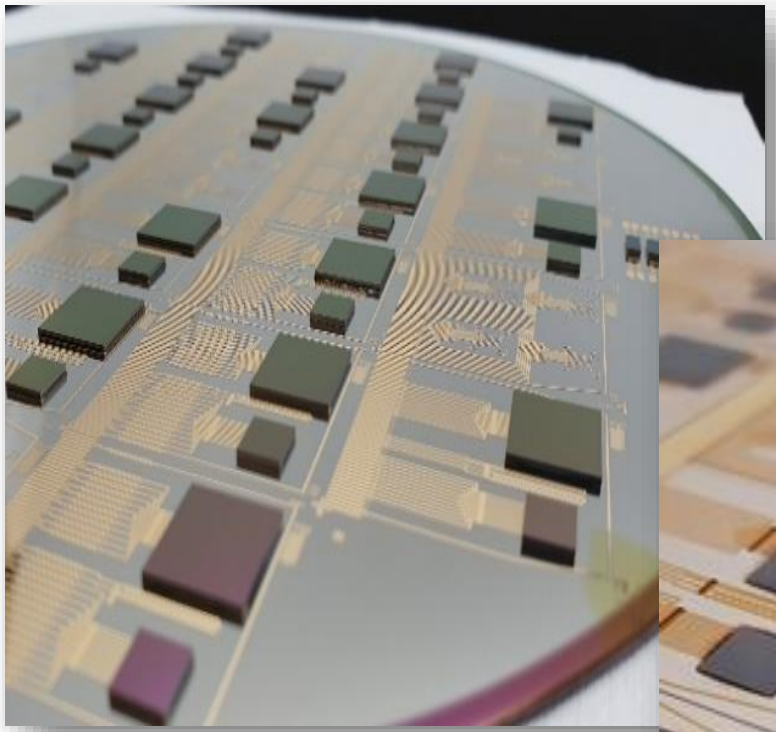
Wafer 200 mm

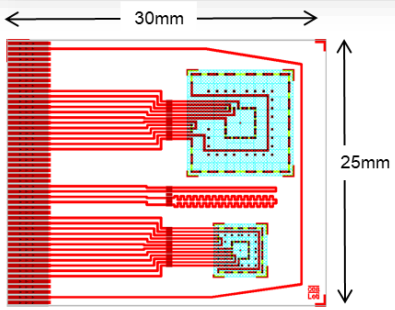


Die: 10x10 mm²

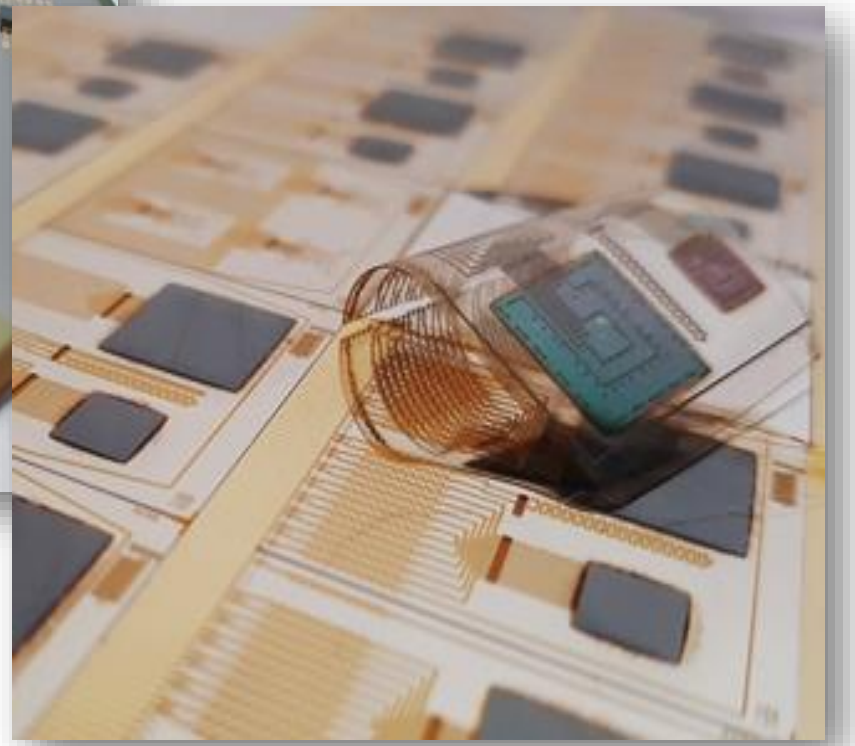
Die: 5x5 mm²

After Flip-Chip Dies bonding

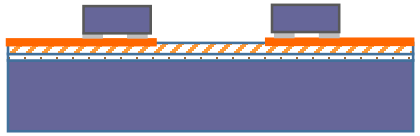
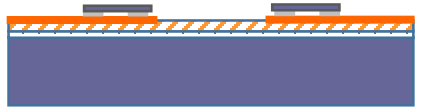
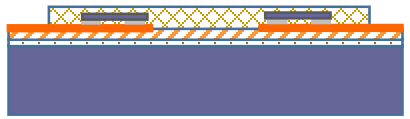


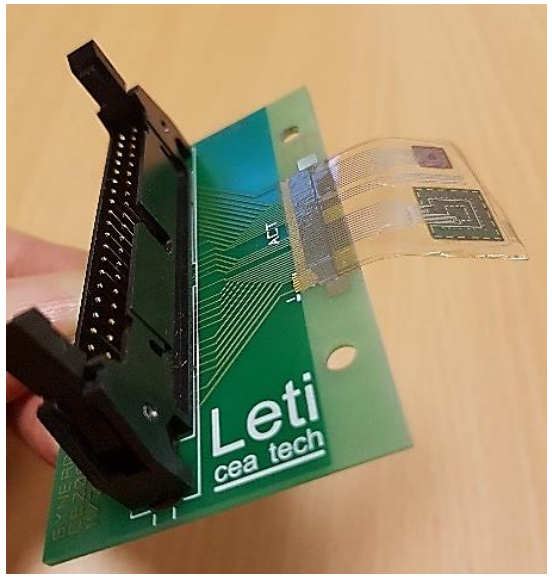


After thinning, polymer coating and final separation



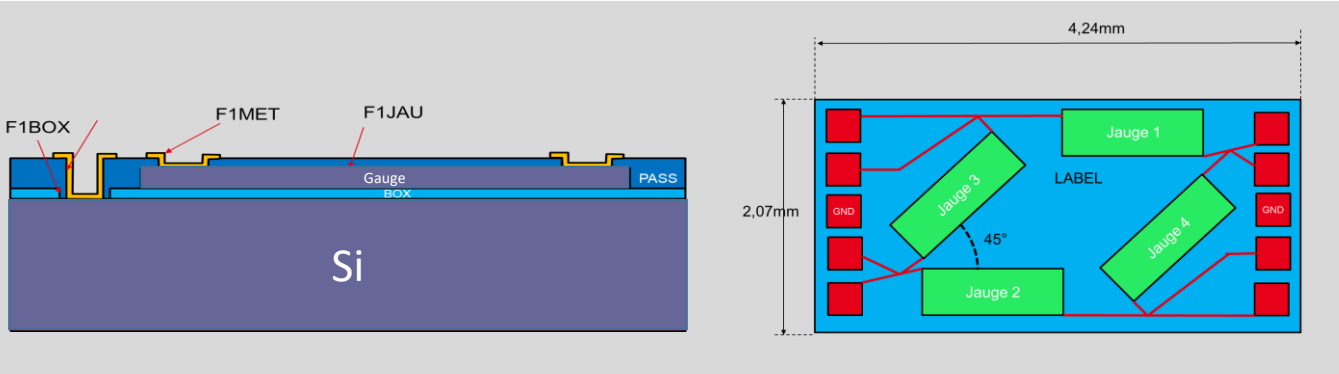
ELECTRICAL YIELD (DAISY CHAIN)

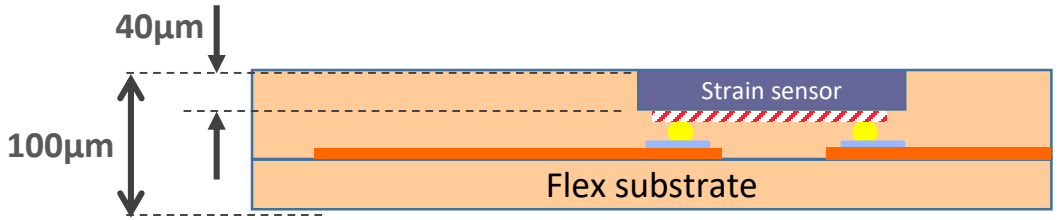
	Large dies		Small dies	
	Peripheral	Central	Peripheral	Central
After bonding 	100%	100%	100%	100%
After thinning 	100%	100%	100%	100%
After Coating 	100%	100%	100%	100%

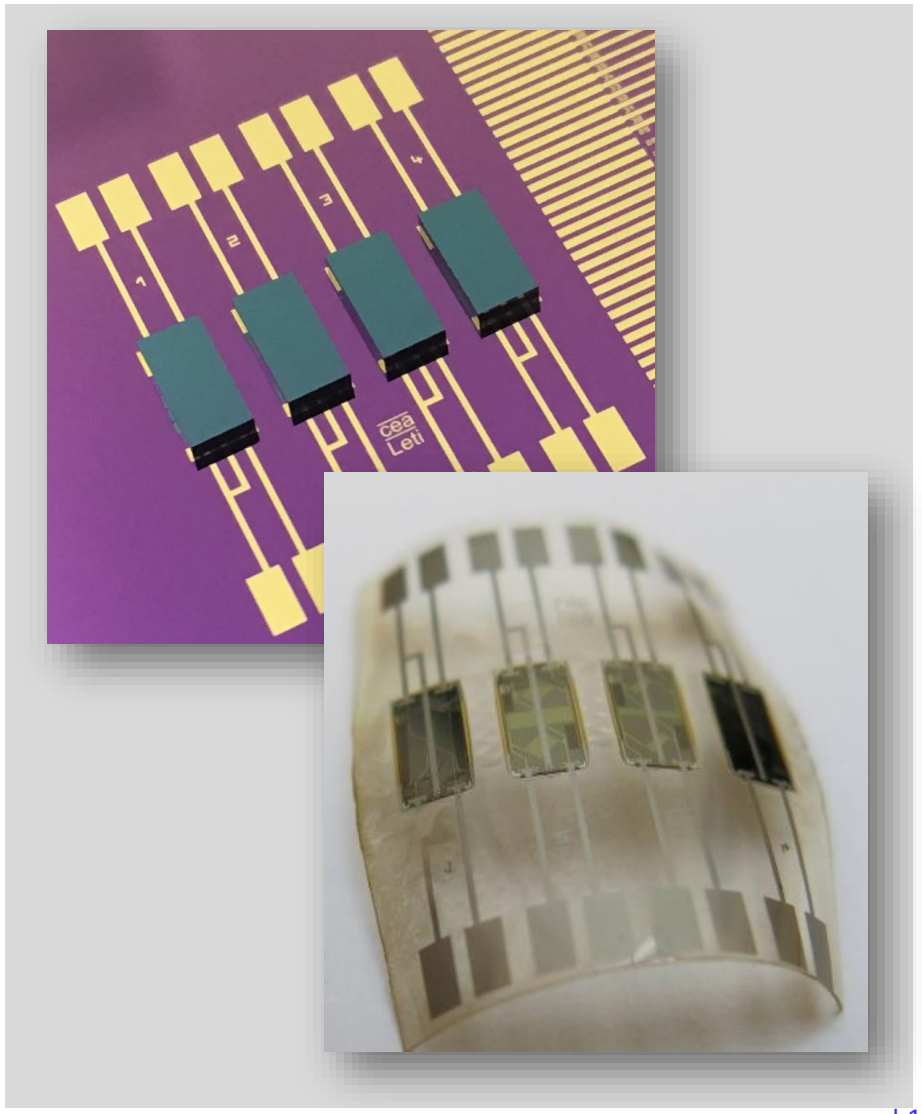


- First demonstration of silicon dies integration within a flexible film using a **collective thinning process**.

UNDER DEVELOPMENT : HIGH PERFORMANCE STRAIN SENSOR PATCH







- Electrical test OK
- Full sensor performance in progress

Thank you for your attention

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www.leti-cea.com