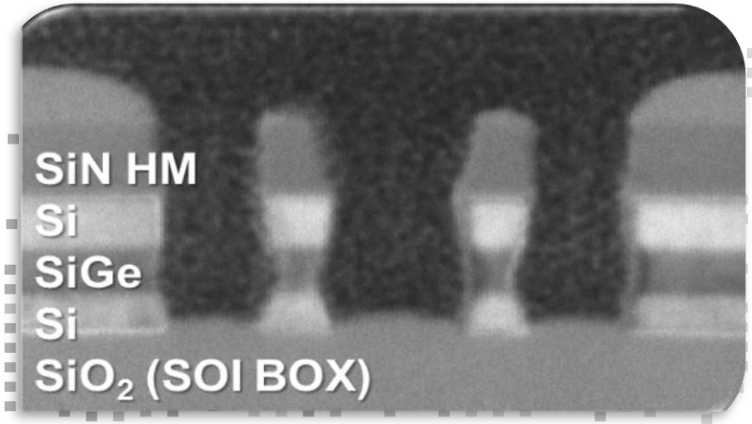


DIRECTED SELF ASSEMBLY OF BLOCK COPOLYMERS: FROM MATERIALS TO INTEGRATION

R.Tiron et al., Leti Litho wokshop, February 28, 2019

OUTLINE

DSA & Lithography

Contact hole

Line & space for nanowires

Chemo epitaxy for high chi

Non-CMOS applications

DSA PATTERNING OPORTUNITIES

International Roadmap for Devices and Systems (IRDS) 2017 for lithography

Next Generation Technology	First Possible Use in Mfg.	Feature Type	Device Type
Multiple Patterning Extension to >4X patterning	2019	Vias, contacts or cut patterns for high performance logic	"7nm" Logic Node
EUV	2018	22 to 24nm hp CH/Cut Levels back end metals at 18nm hp LS	"7nm" Logic Node
DSA (for pitch multiplication)	2021	Contact holes/cut levels for logic. Possibly nanowire patterning	"5nm" Logic Node

EUV & multiple patterning

Insertion for 7nm node

Expensive and complex

EUV Limitation: Stochastic effects on the exposed resist as feature size shrink

DSA patterning

Opportunity for **memory,** sub 5 nm logic node

Benefits: low cost, high resolution (pitch <20nm)

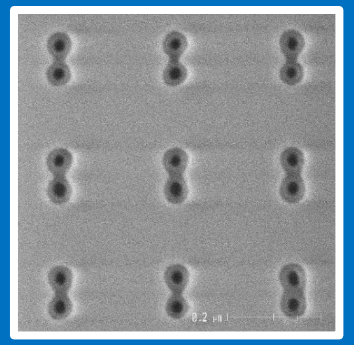
Main challenges: ensure perfect patterning (defectivity), design rules restriction

DSA can be a low cost & complementary solution for sub-5nm logic node
Potential applications: contact hole level, Nanowire (NW) patterning

DSA ADVANCES IN LETI

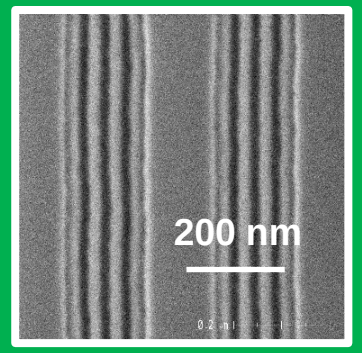
PS-*b*-PMMA

Graphoepitaxy for contact



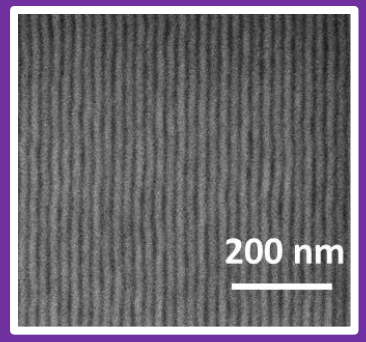
- Shrink and doubling
- Process stability monitoring
- Integration for Via0

Graphoepitaxy for L/S



- Benchmark materials
- Integration for NW
- Prepare metrology for high chi

Chemoepitaxy for L/S



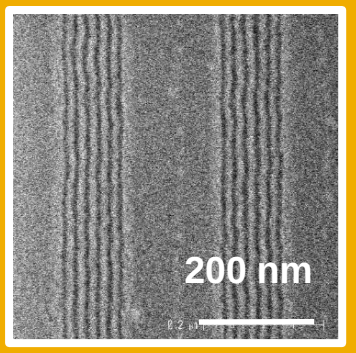
- Benchmark chemo vs grapho
- Prepare high chi

22nm < L_0 < 80nm

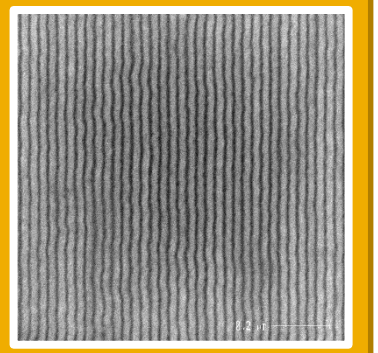
High - χ

High chi for L/S

Graphoepitaxy



Chemoepitaxy



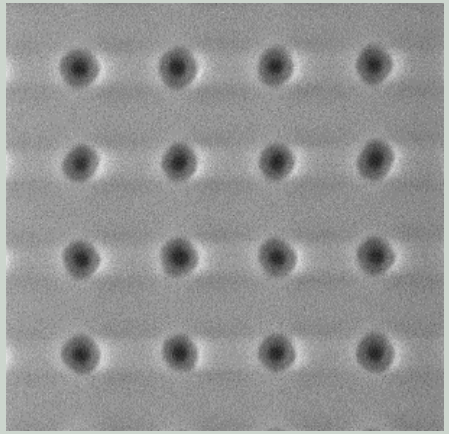
- Next generation material & processes

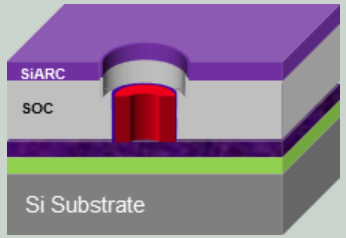
L_0 < 20nm

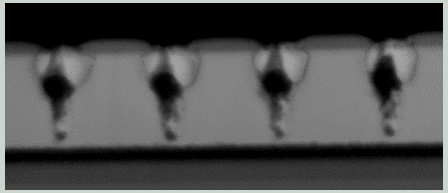
A wide array of materials and process flows available

THE MAIN ACHIEVEMENTS: PS-*b*-PMMA CH DSA FOR VIA0 PATTERNING

SiARC/SOC *Organic template*



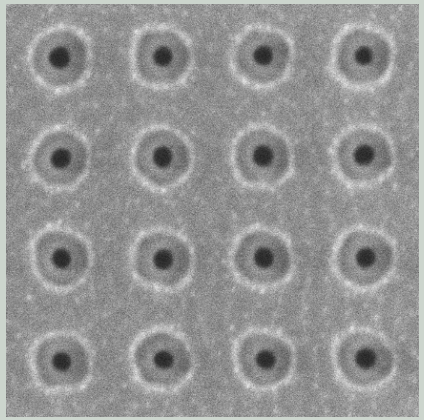


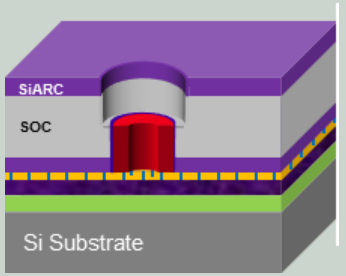


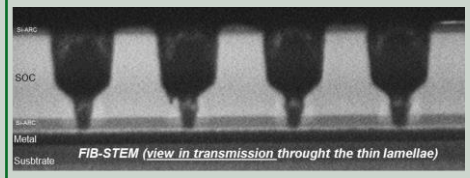
Guide template:
CD $_{guide}$ = 40.5 nm
CDU-3σ$_{guide}$ = 4.0nm

DSA:
CD = 17.2nm
CDU-3σ = 1.3nm
HOY = 100%
Planar: OK
Residue 3σ = 3.9nm
Rework : NO

SiARC/SOC *Embedded NL*



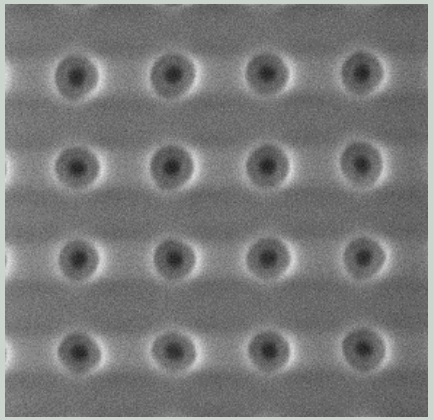


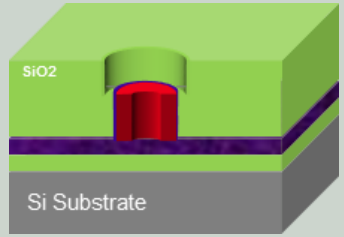


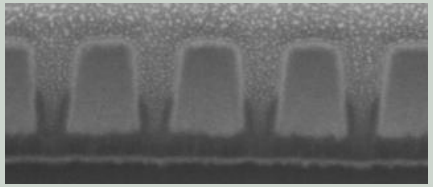
Guiding template:
CD $_{guide}$ = 50nm
CDU-3σ$_{guide}$ = 4.6nm

DSA:
CD = 22nm
CDU-3σ = 1.4nm
HOY = 100%
Planar OK
Residue 3σ = 0.6nm
Rework: NO

Silicon Oxide *Inorganic template*





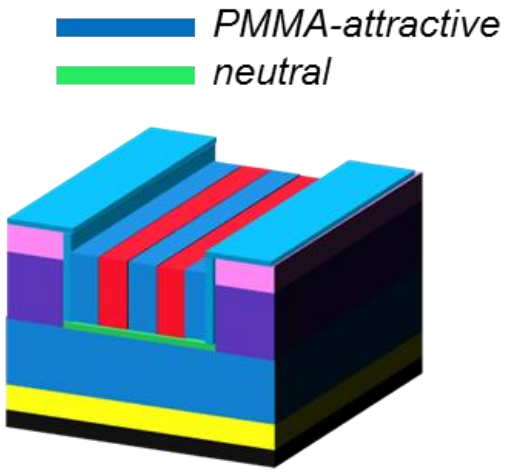


Guiding template:
CD $_{guide}$ = 40nm
CDU-3σ$_{guide}$ = 4.6nm

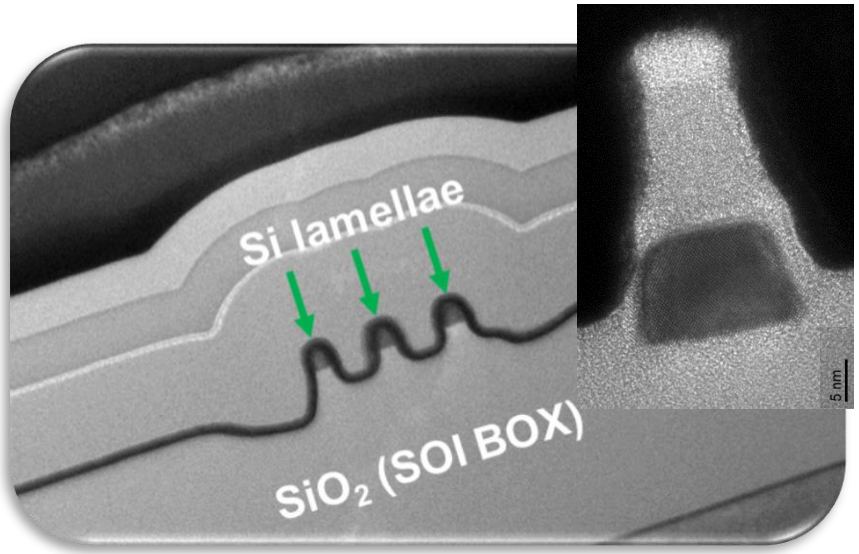
DSA:
CD = 17.6 nm
CDU-3σ = 1.4nm
HOY = 100%
Planar OK
Residue NA
Rework: OK

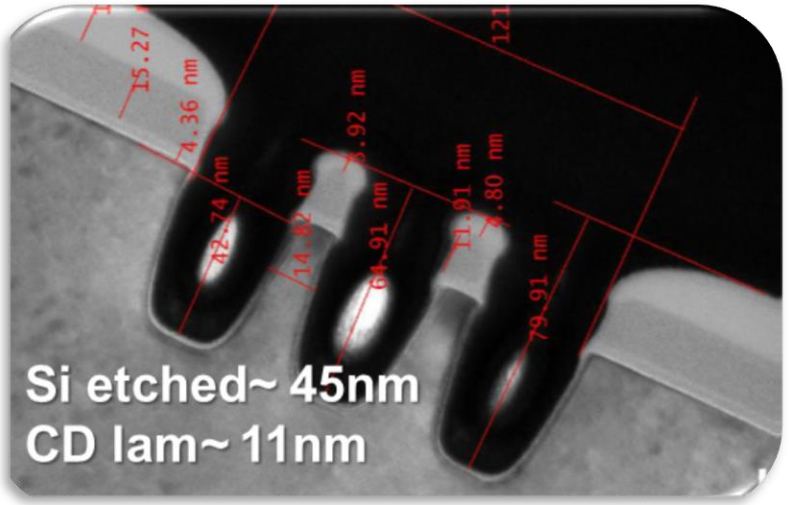
Several process options available for Contact hole integration

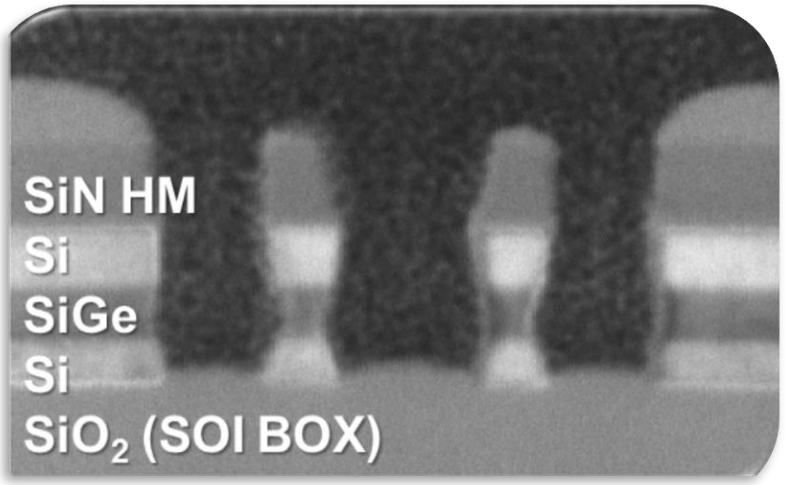
TOWARDS STAKED NANOWIRES



- **Demonstration of etching capabilities with Si bulk**
  - 45nm depth demonstrated
- **Transfer to Si/SiGe/Si stack (short loop)**
  - Capabilities demonstrated
- **Transfer to Si/SiGe/Si stack (electrical lot)**
  - Cut step demonstrated

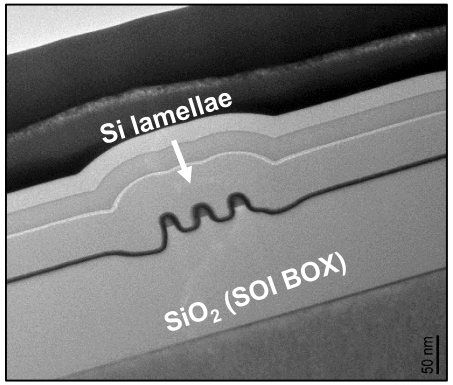




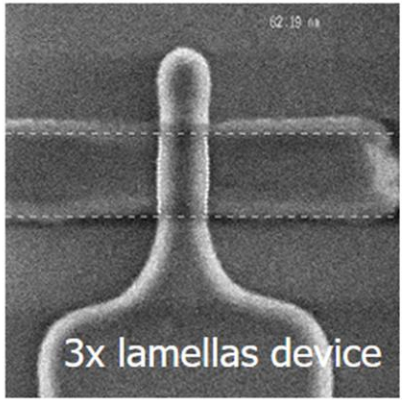


PS-*b*-PMMA GRAPHOEPITAXY FOR NANOWIRES

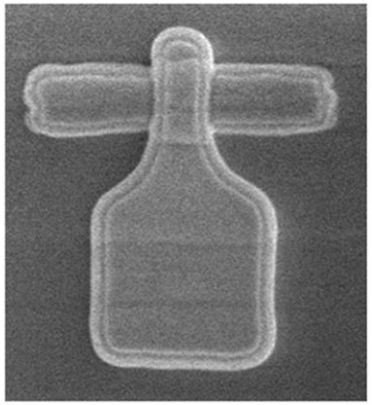
TEM cross section
(after Gate Stack)

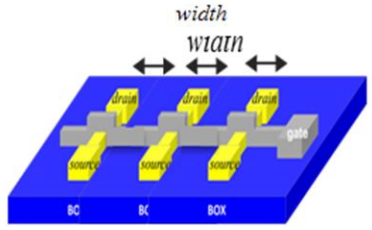


S/D Epitaxy



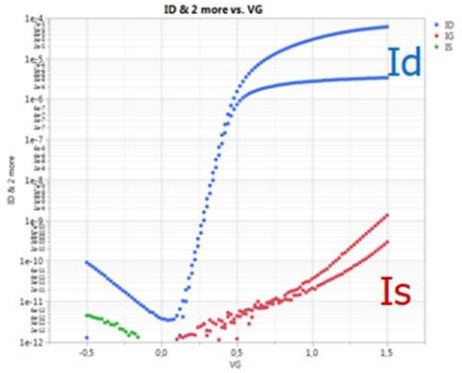
After Spacer "2"





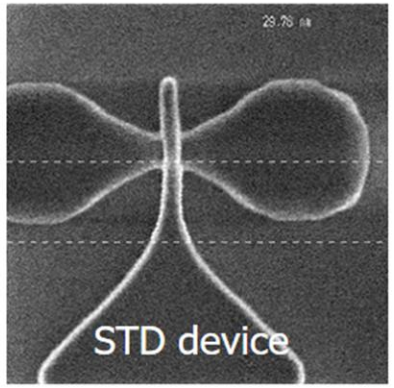
DSA device

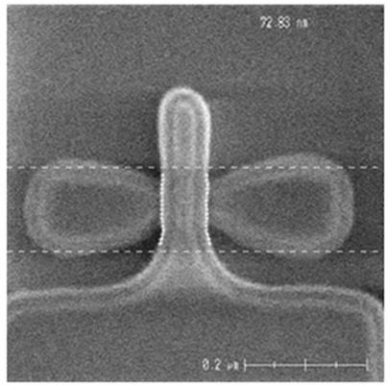
Example of Id=f(Vg)
(Vd=0,05;1,5V)

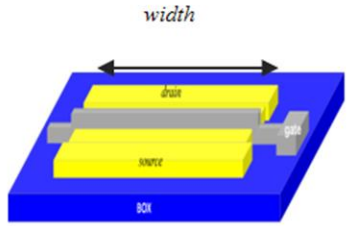


Reference "STD" single transistors →

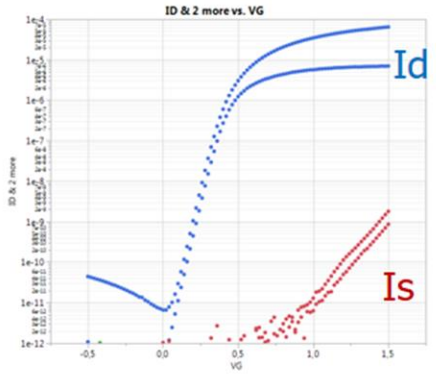
(fabricated in parallel by using Cut/Active mask on the same wafers)





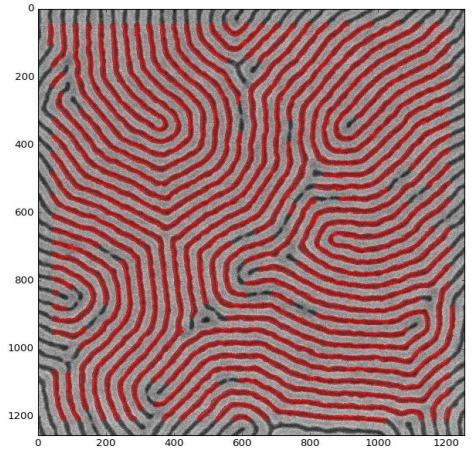


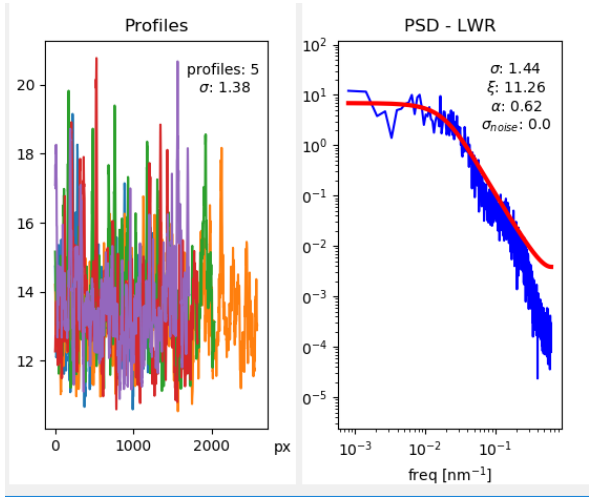
STD device



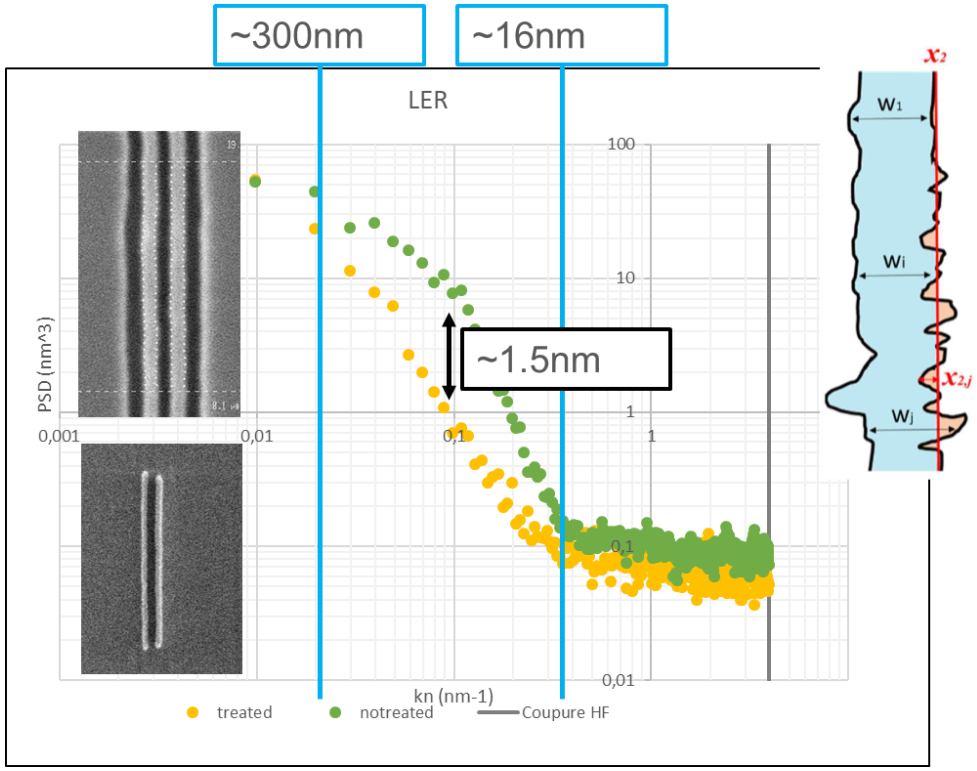
Electrical test on nanowire based devices patterned by DSA

DSA CHARACTERIZATION AND ASSOCIATED COMPUTATIONAL METROLOGY

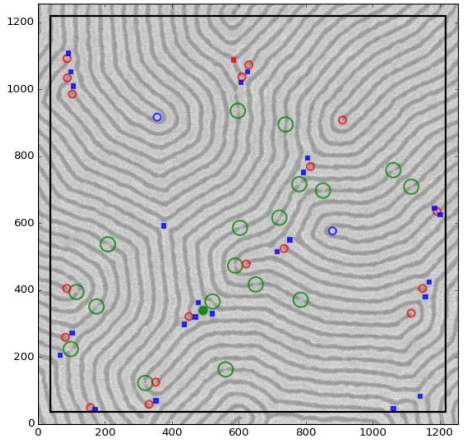


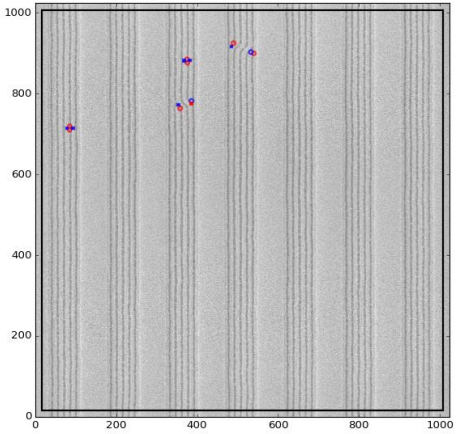


Roughness using PSD



Defectivity





Defectivity & roughness monitored on fingerprint and patterned surfaces

OUTLINE

Lithography in Leti

Contact hole

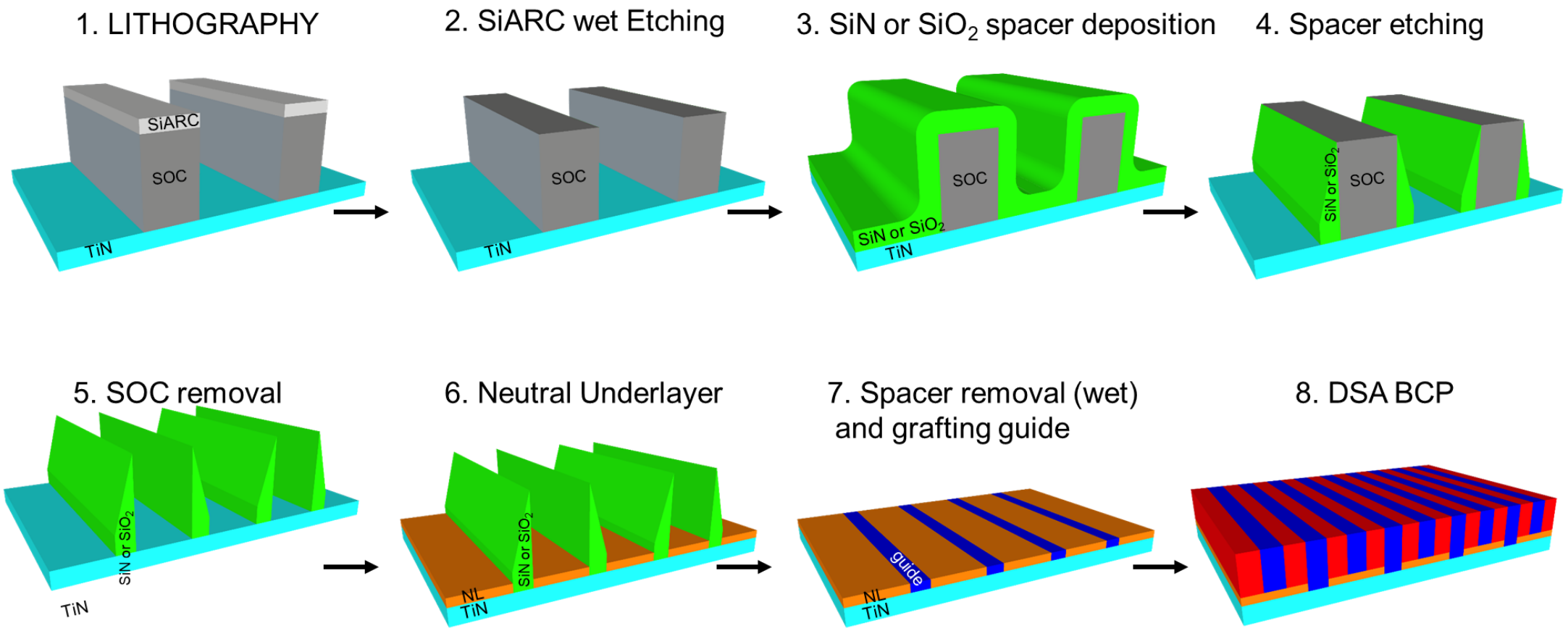
Line & space for nanowires

Chemo epitaxy for high chi

Non-CMOS applications

ACE PROCESS

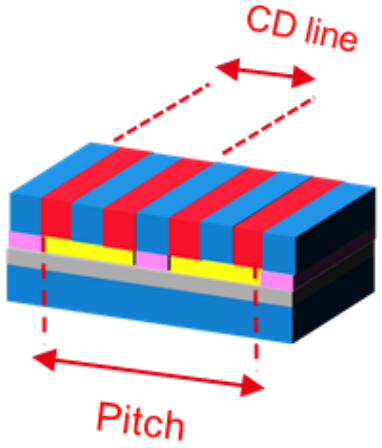
NL: neutral layer
BCP: block copolymer



A new chemoepitaxy process by spacer patterning
Compatible with high chi BCPs

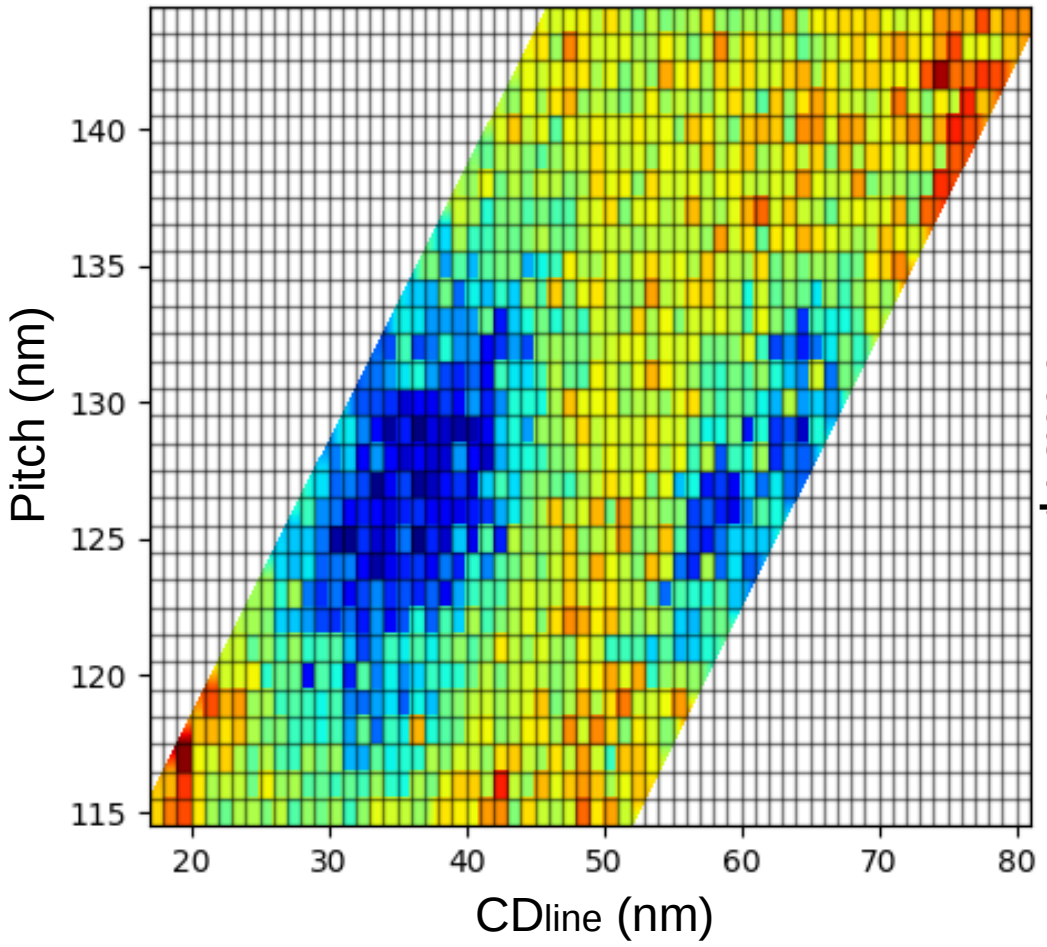
A.Paquet et al, SPIE2019, Paper 10958-21.

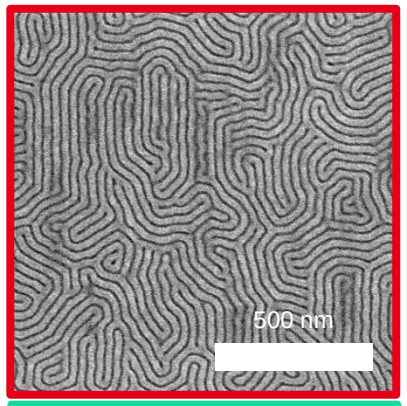
ACE PROCESS WINDOW

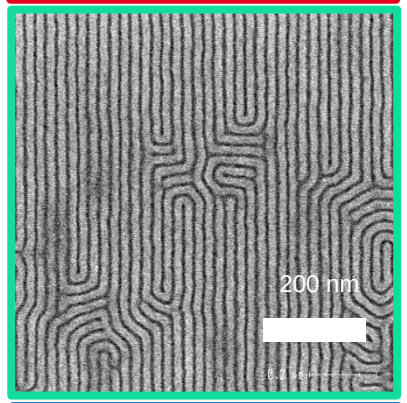


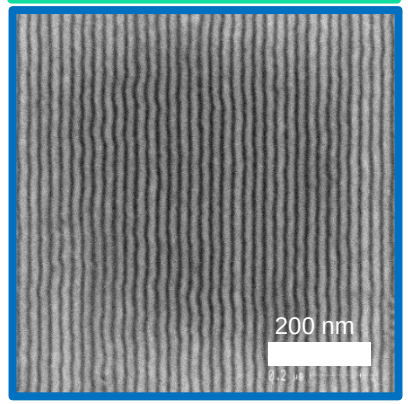
polymer intrinsic period
L_0 = 30 nm
CD_{spacer} = 15 nm

Defectivity mapping



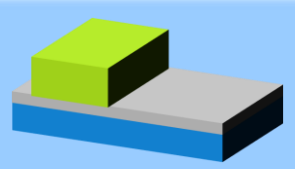




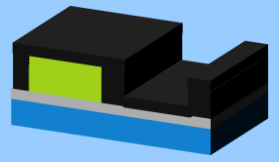


Process window determination for spacer-chemoepitaxy by L30 BCP

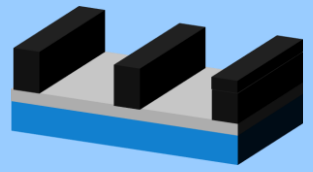
ACE PROCESS FROM PS-PMMA TO HIGH CHI



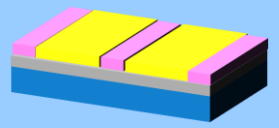
193i lithography



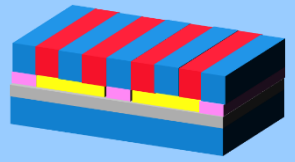
Spacer deposition



Spacer patterning



Selective grafting



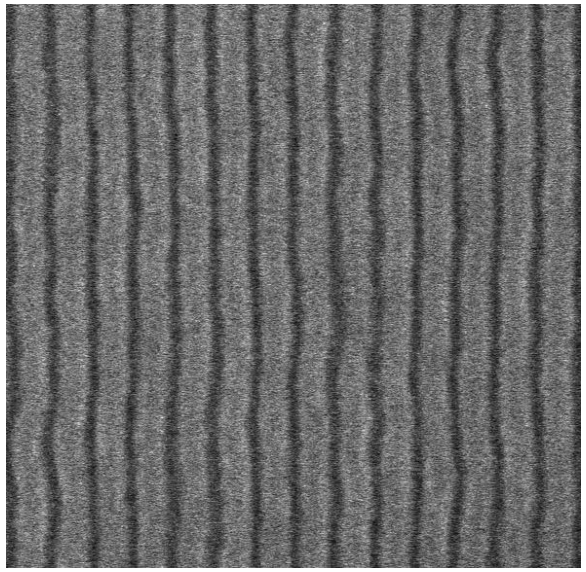
BCP self-assembly

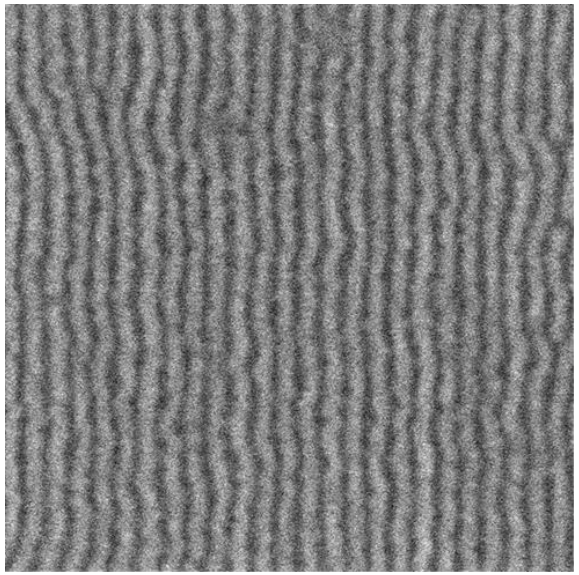
PS-PMMA lamellar 30nm pitch

L_0=30nm CD = 15nm	guide pitch	Multip. factor
	120	2
	180	3
	240	4

High chi lamellar 18nm pitch

L_0 = 18nm CD = 9nm	guide pitch	Multip. factor
	72	2
	108	3
	144	4

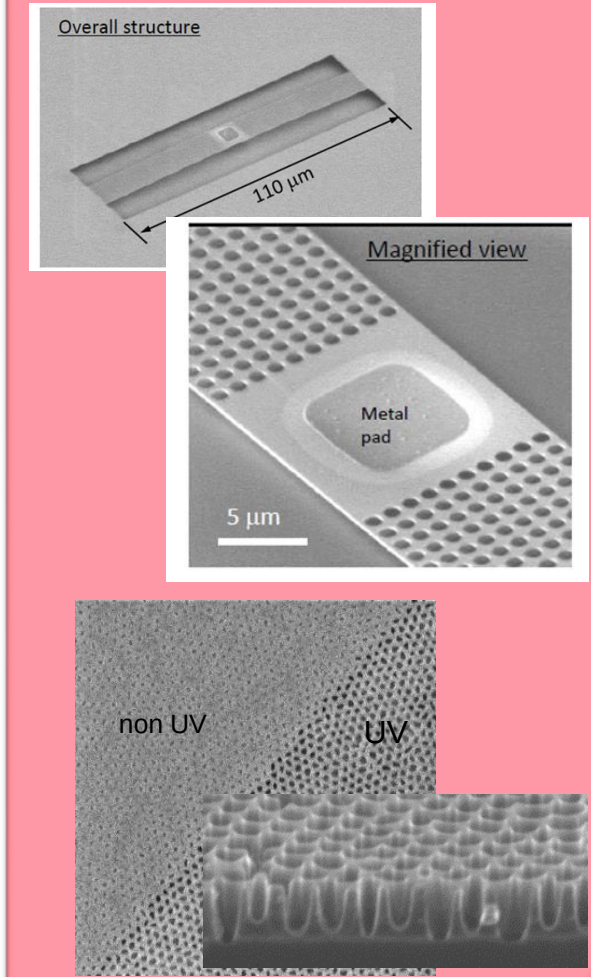




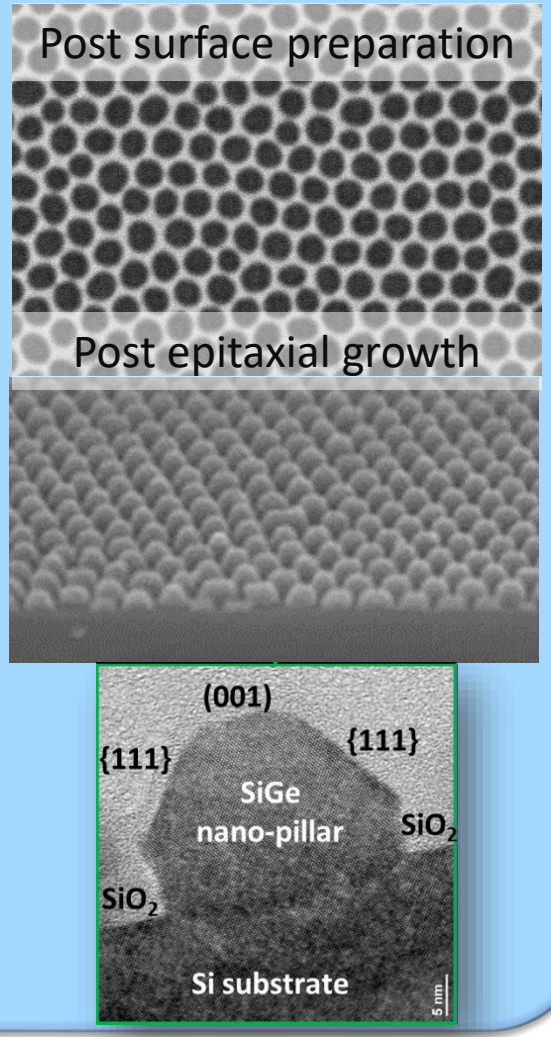
Template resolution & density constraints are relaxed

THE MAIN ACHIEVEMENTS : BEYOND CMOS APPLICATION

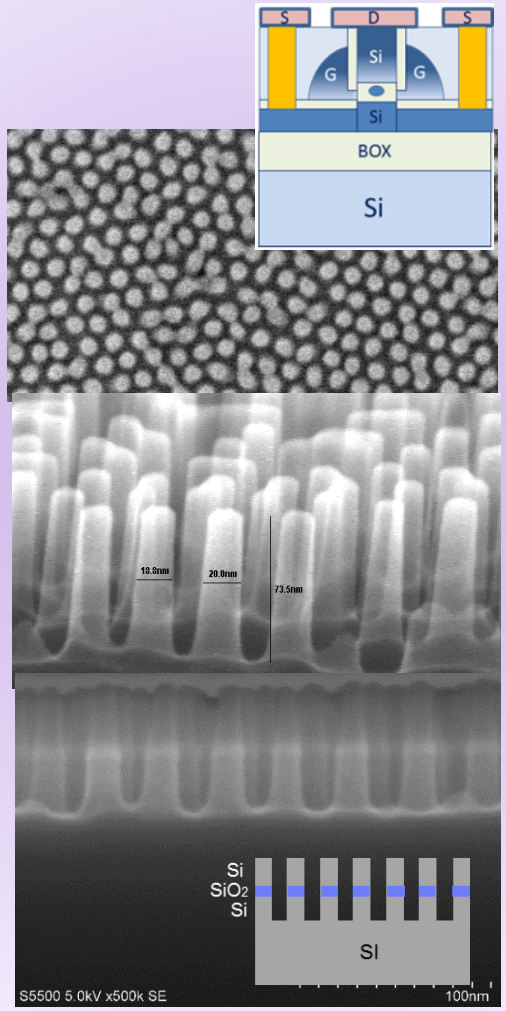
Nano-membrane manufacturing



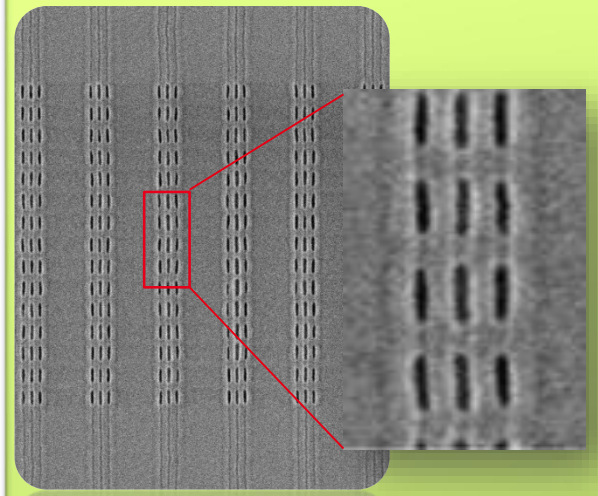
Epitaxial growth



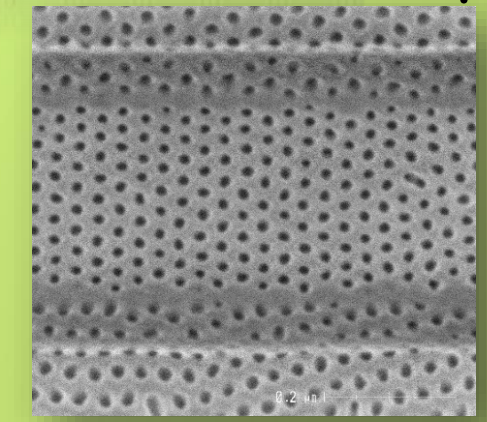
SET manufacturing



DSA+e-beam cut

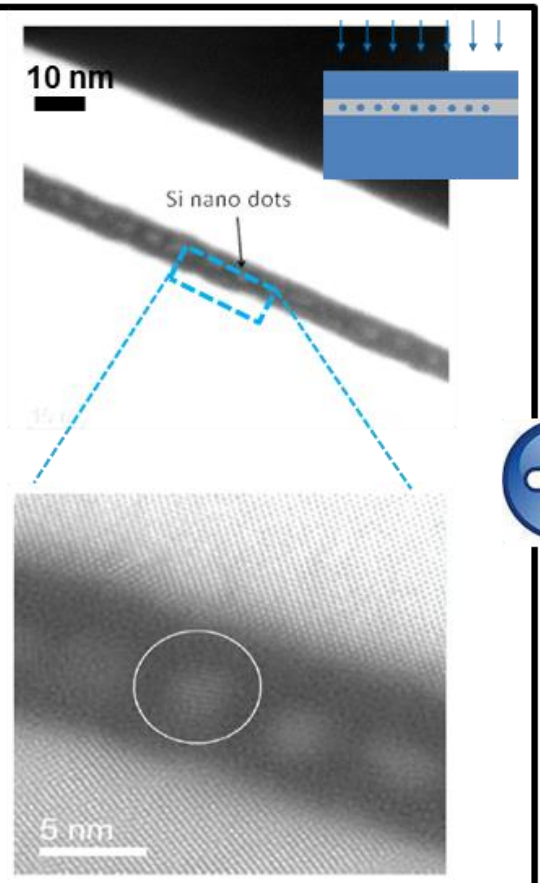


DSA+imprint

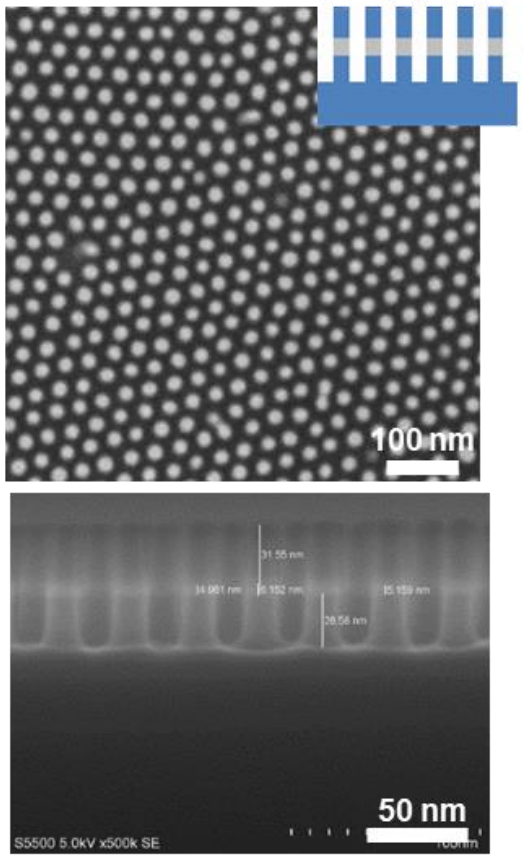


SI NANODOT AUTO-ALIGNEMENT FOR SET APPLICATION

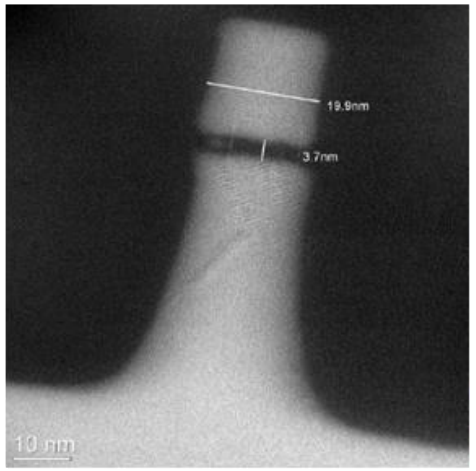
SI nanodot Auto-alignement for SET (Single Electron Transistor)

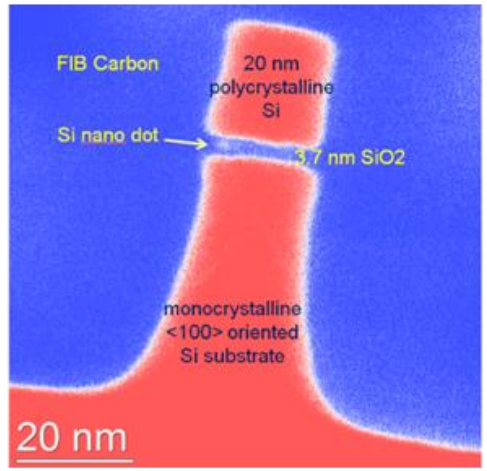


1. Ion-induced Si Nanodots self-assembly



2. Pillar fabrication by block copolymer self-assembly



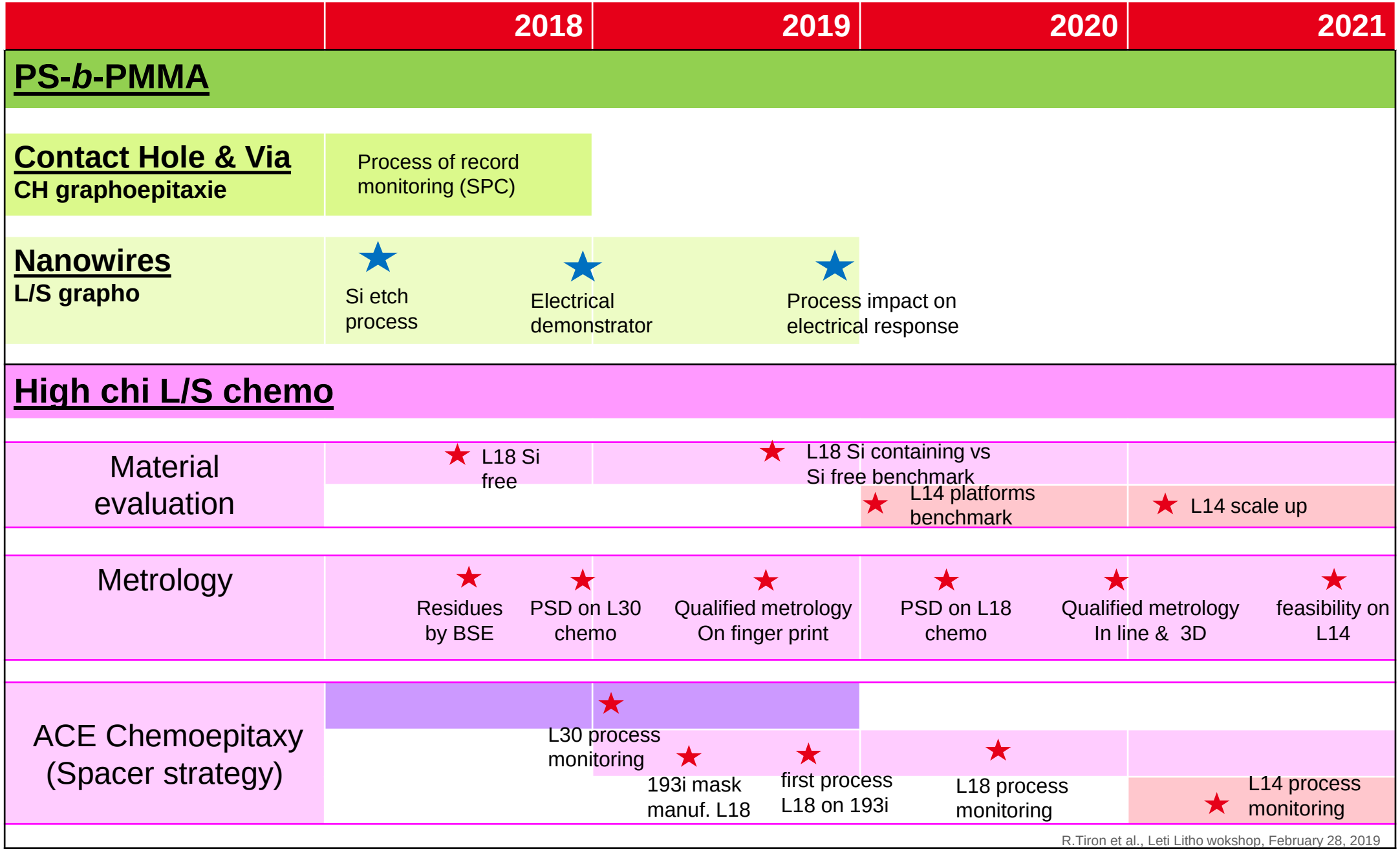


3. Si nanodot auto-alignement

A first proof of concept showwing Si nanocluster formation on nanopillar (using e-beam lithography)

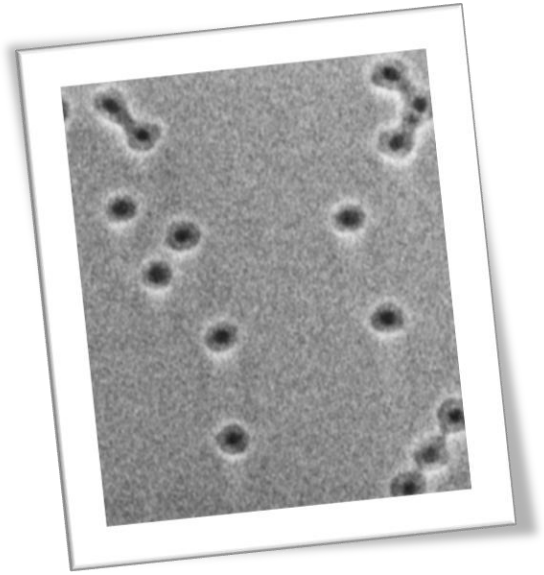
Goal: Directed Ion-Induced Self-Assembly (DIISA) of single Si nanodot (ND) in prefabricated DSA pillars

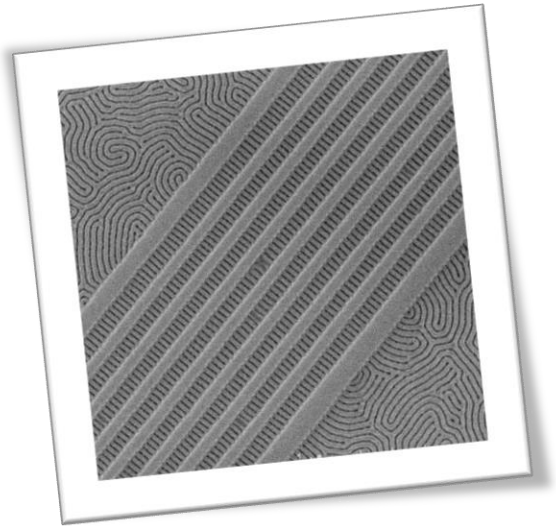
A. Gharbi et al., SPIE paper# 10960-57 , February 27 2019


2018
2019
2020
2021
PS-b-PMMA
Contact Hole & Via
CH graphoepitaxie
Process of record monitoring (SPC)
Nanowires
L/S grapho
Si etch process
Electrical demonstrator
Process impact on electrical response
High chi L/S chemo
Material evaluation
L18 Si free
L18 Si containing vs Si free benchmark
L14 platforms benchmark
L14 scale up
Metrology
Residues by BSE
PSD on L30 chemo
Qualified metrology On finger print
PSD on L18 chemo
Qualified metrology In line & 3D
feasibility on L14
ACE Chemoepitaxy (Spacer strategy)
L30 process monitoring
193i mask manuf. L18
first process L18 on 193i
L18 process monitoring
L14 process monitoring

SUMMARY

- DSA can easily meet resolution requirements down to N5.
- Different processes available to control selective surface modification.
- ACE: New chemoepitaxy approach using spacer patterning implemented
- DSA: extended beyond CMOS





DSA 2019

5th International Symposium on DSA
Milan - October 16-18, 2019

http://dsasymposium.org

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