The Challenges of Lithography

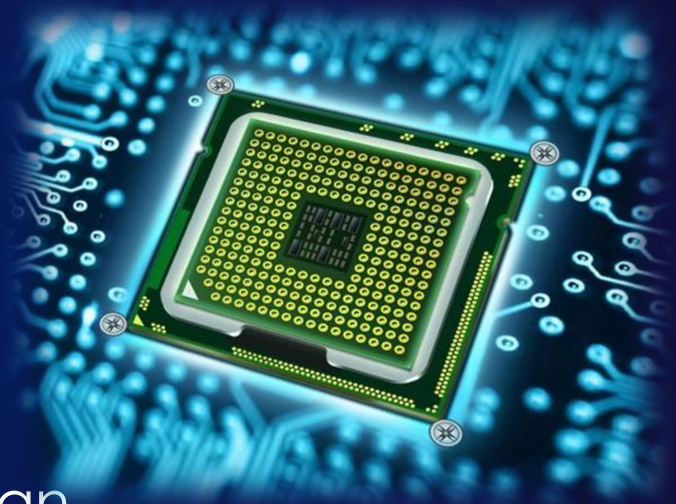
Jack Chen
NanoPatterning Technology Co.

We are creating the future!

INTERNET OF THINGS

What we want

- Faster, lighter
- More integrated functions
- Less power dissipation
- Cheaper



- Custom design/Personalized design
- Privacy and Security

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Moore's Law Keep Going…

IC Knowledge cost models: Chip industry is succeeding in scaling density and costs.

Cost Projections

Relative Wafer Cost

Relative wafer cost: 9.00, 8.00, 7.00, 6.00, 5.00, 4.00, 3.00, 2.00, 1.00, 0.00

Node: 130nm, 90nm, 65nm, 40nm, 28nm, 20nm, 16nm, 10nm, 7nm, 5nm, 3.5nm, 2.5nm

2 layer CFET no litho shrink

HNW

EUV

Beginning of multi-patterning

1st FinFET no shrink

Relative Density

Relative density: 1000.00, 100.00, 10.00, 1.00

Node: 130nm, 90nm, 65nm, 40nm, 28nm, 20nm, 16nm, 10nm, 7nm, 5nm, 3.5nm, 2.5nm

No shrink at 16nm for first FinFET

Relative Cost Per Unit

Relative cost: 1.000, 0.100, 0.010

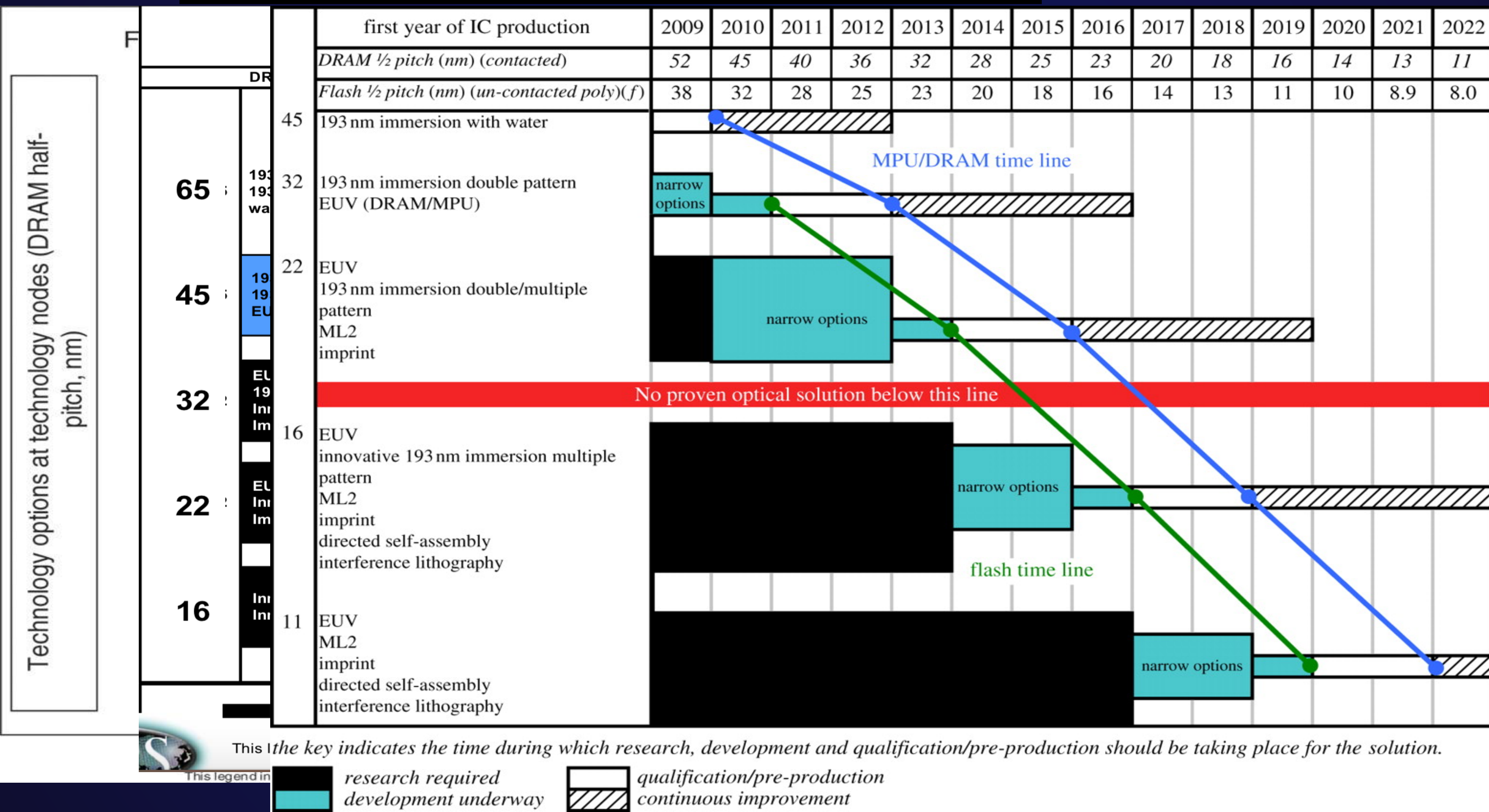
Node: 130nm, 90nm, 65nm, 40nm, 28nm, 20nm, 16nm, 10nm, 7nm, 5nm, 3.5nm, 2.5nm

No shrink with FinFET cost adder

(Source: Scotten Jones presentation at 2017 SEMI ISS)

SEMI Industry Strategy Symposium (ISS)

ITRS roadmap 2009



“The limit of lithography will not be in resolution but in economy.”

– Dr. Burn J. Lin, in 1987

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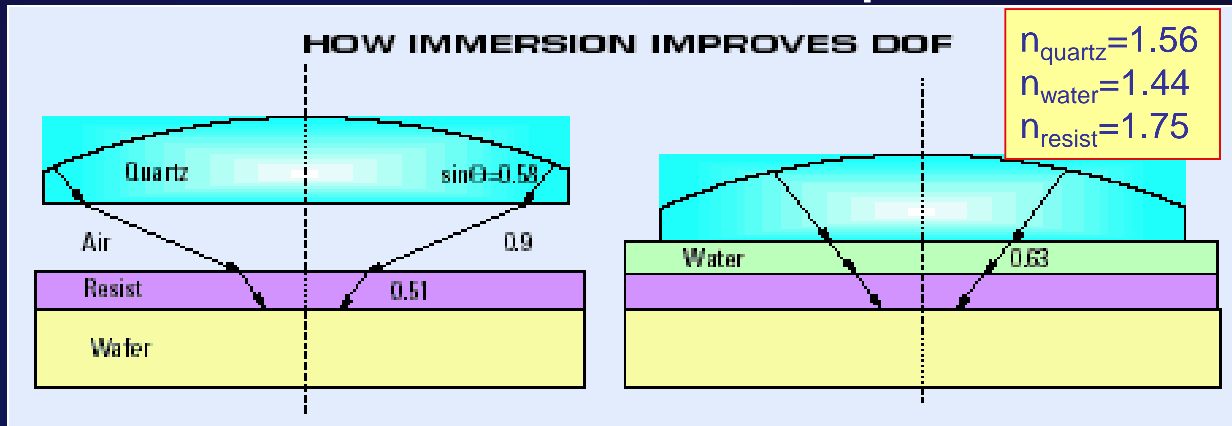
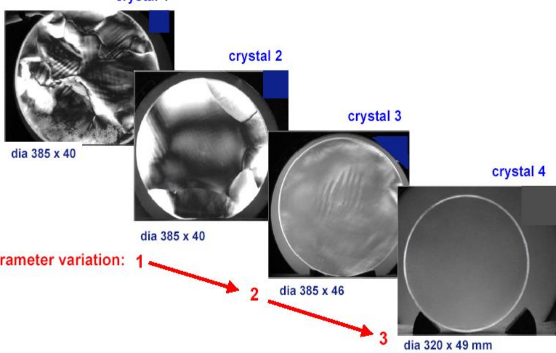
All about **Money / Time**!

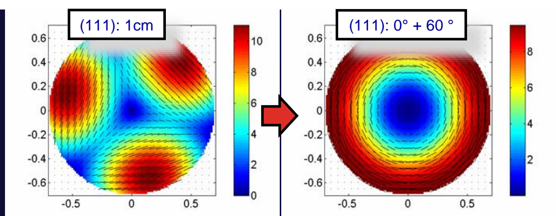
- R&D, Capital investment and Readiness in time

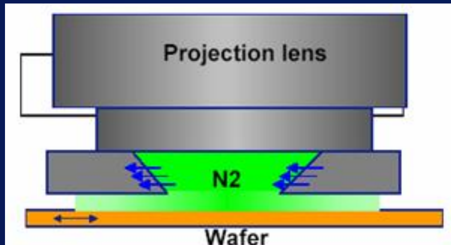
Innovation-1: Immersion stop 157nm

Burn Lin, Plenary talk in Immersion Workshop 2002, Antwerp









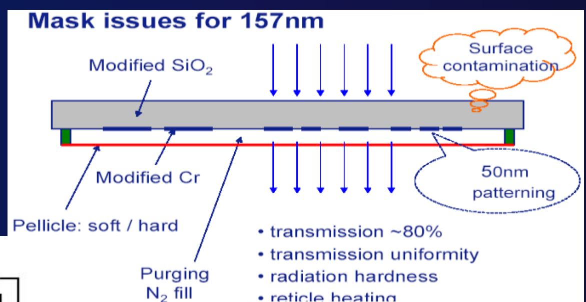
Best Performance Data –PSM

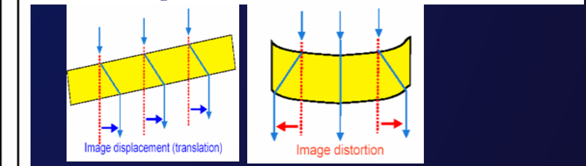
NA =0.6 PC = 0.3	90 nm 1:1	80 nm 1:1	60 nm Isolated
3Q01 — 112 nm Si containing resist (On organic arc)			
2Q02 — 120 nm NBHFA F-Polymer (On organic arc)			
3Q02 — 100 nm Low absorbing Si containing resist (On organic underlayer)			
3Q02 — 200 nm Highly Transparent resist (On organic arc)			

Sept 5, 2002

INTERNATIONAL SEMATECH

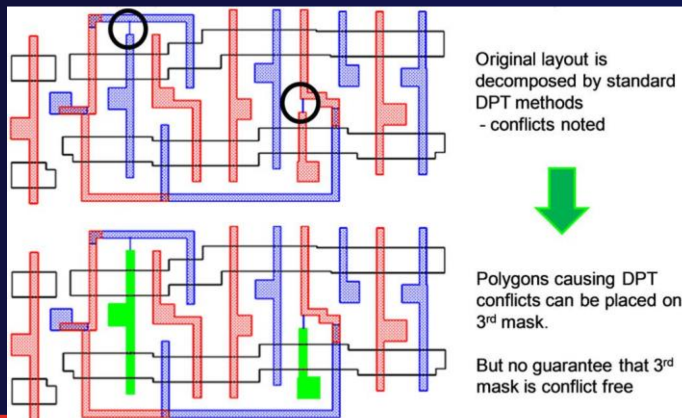
Exposure done on Exitech 0.6 NA stepper at ISMT 13

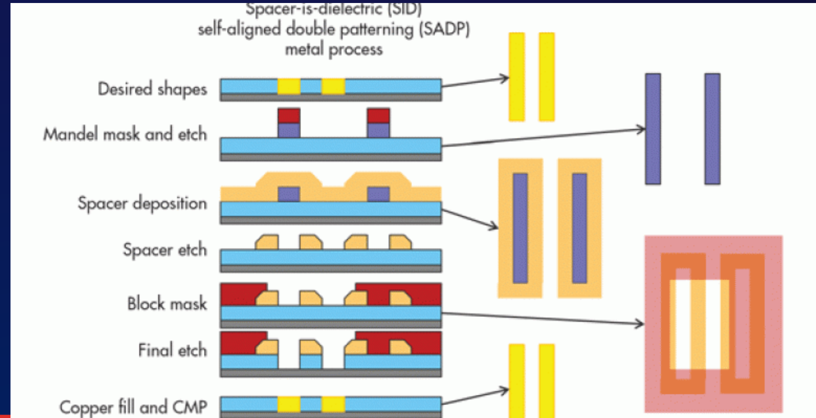


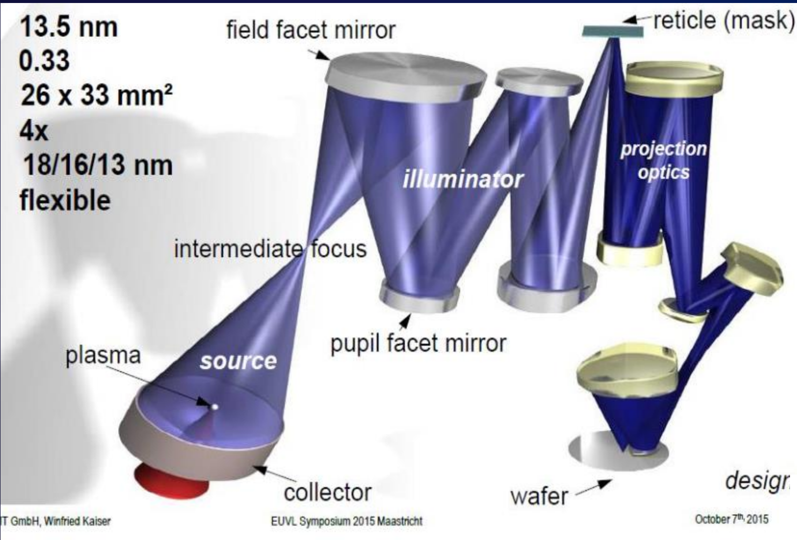


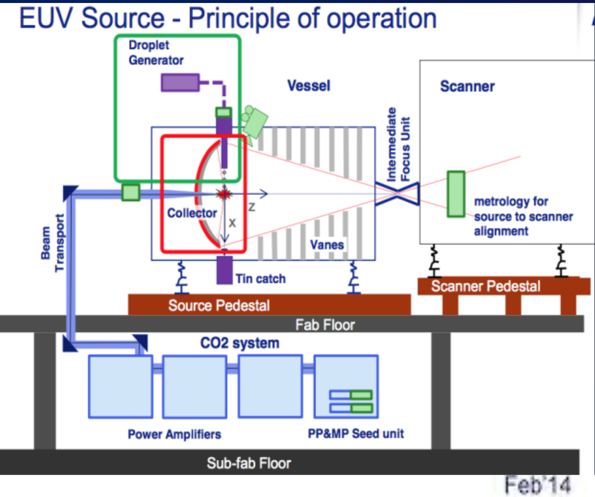
First scanner was ready to ship!

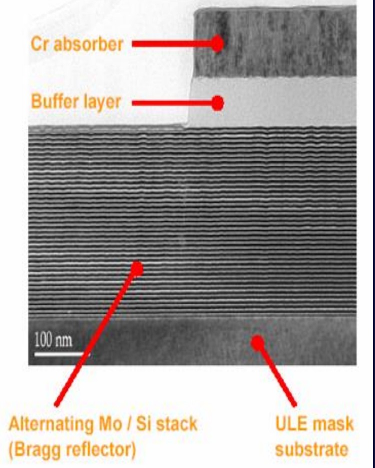
Innovation-2: SADP push out EUV

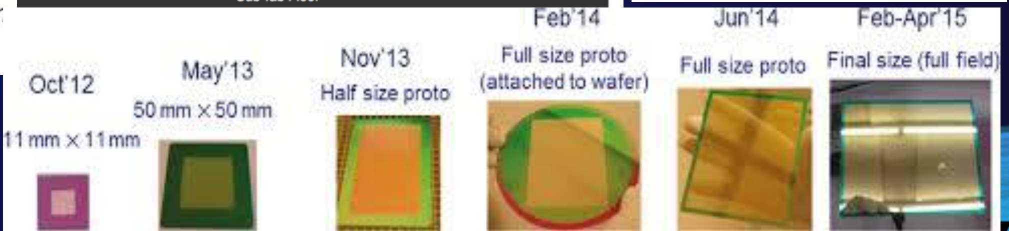












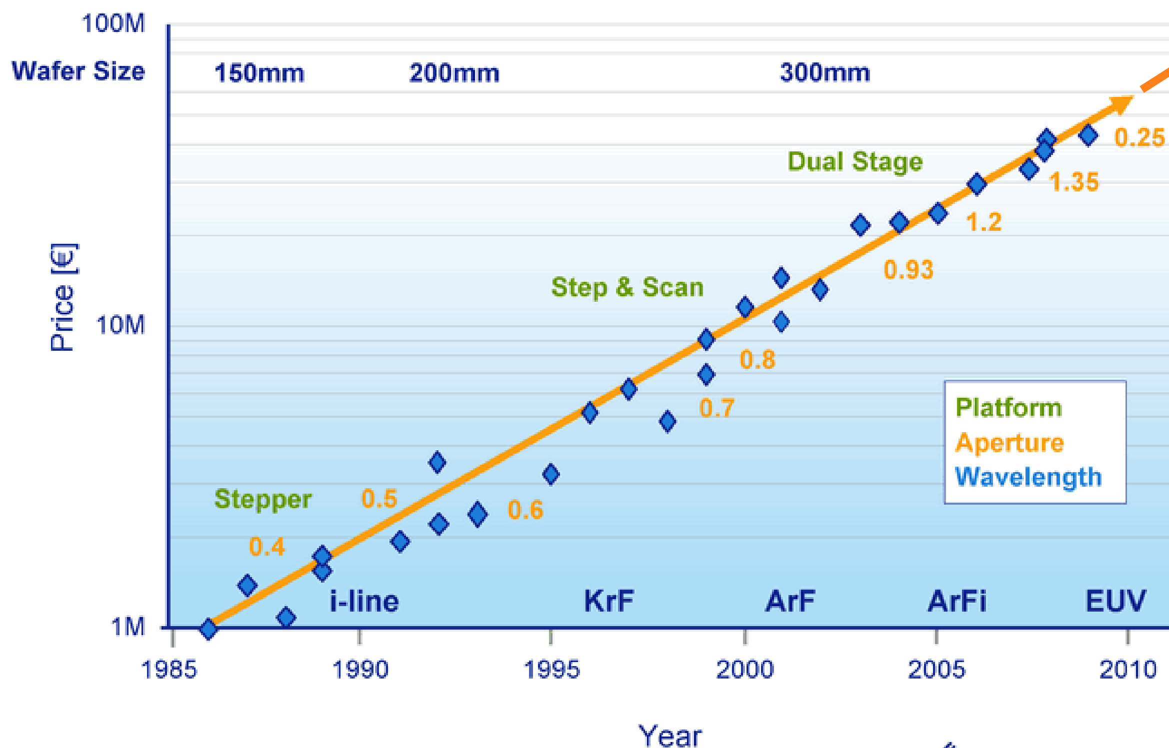
All about **Money / Time**!

- R&D, Capital investment and Readiness in time
- Wafer cost
- Cycle time

$$Contribution\ of\ Capital\ to\ Wafer\ cost = \frac{Capital\ depreciation}{Throughput \times Uptime}$$

Tool price doubles every ~4.5yrs

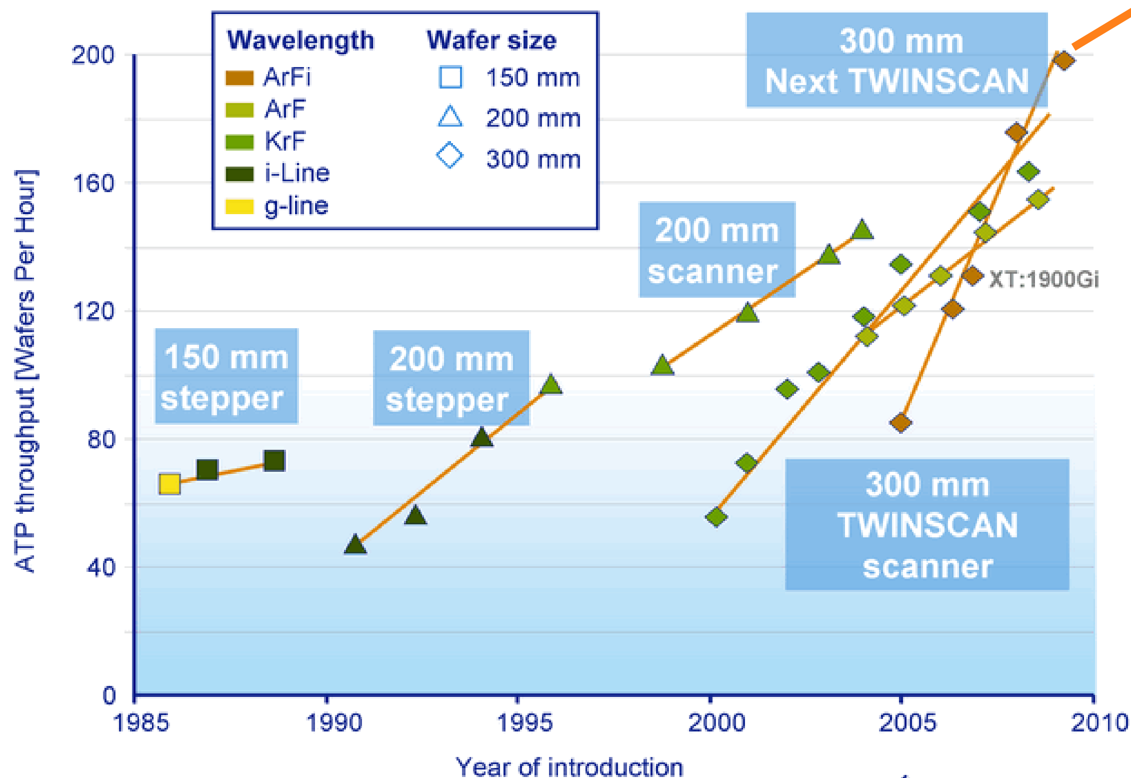
120M @ 2018



Martin van den Brink
Executive Vice President Marketing & Technology

May 20, 2008

Area Throughput doubles every ~ 7.4yrs



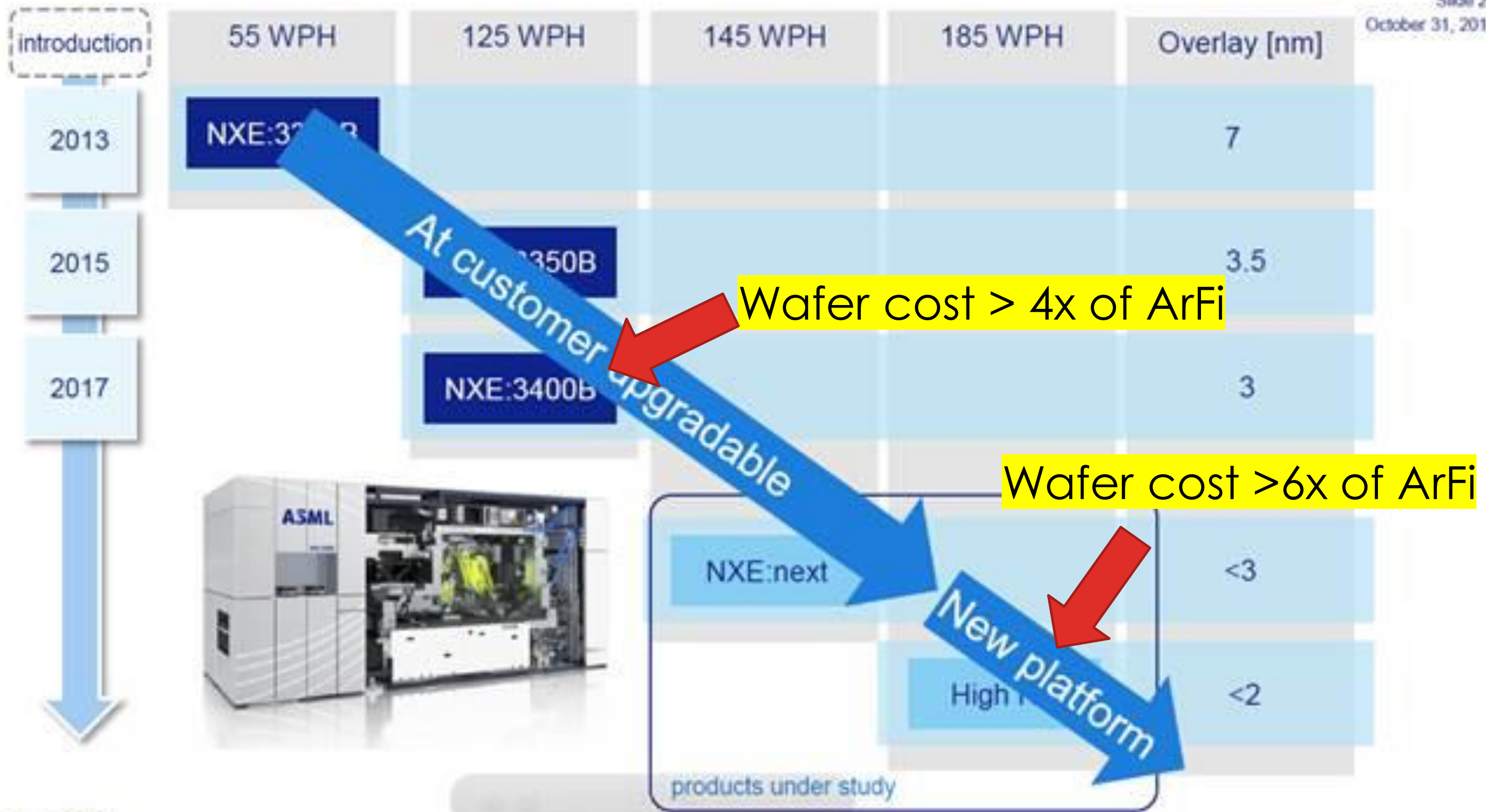
Martin van den Brink
Executive Vice President Marketing & Technology

May 20, 2008

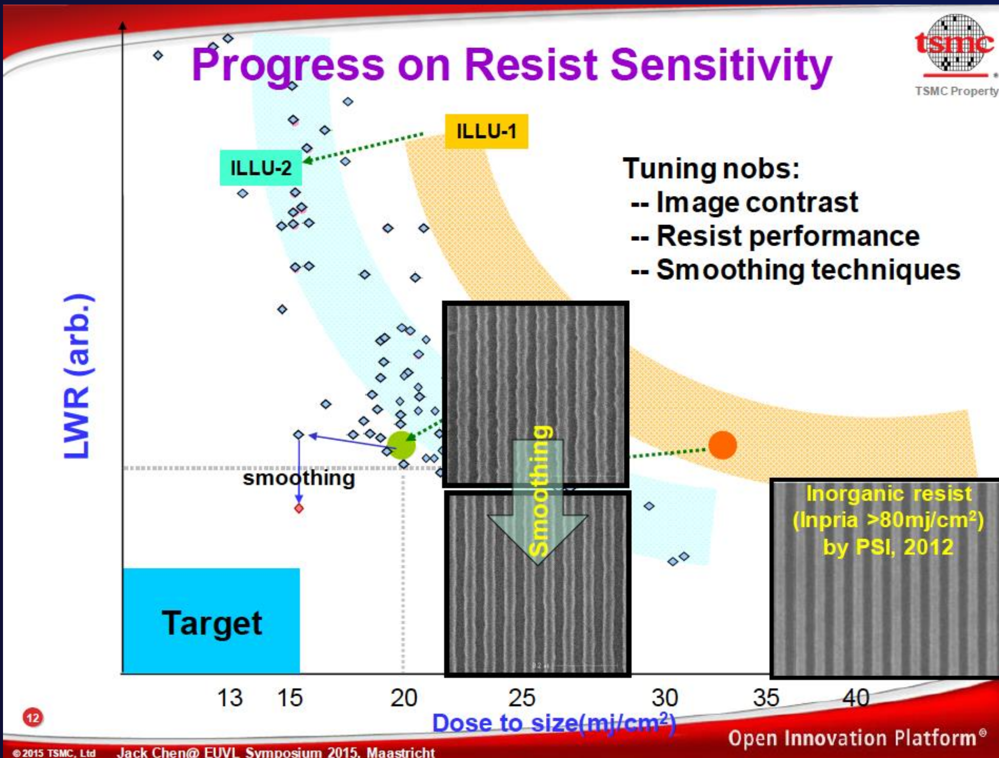
275wph @ 2018
NXT:2000i

125wph @ 2018
NXE:3400B

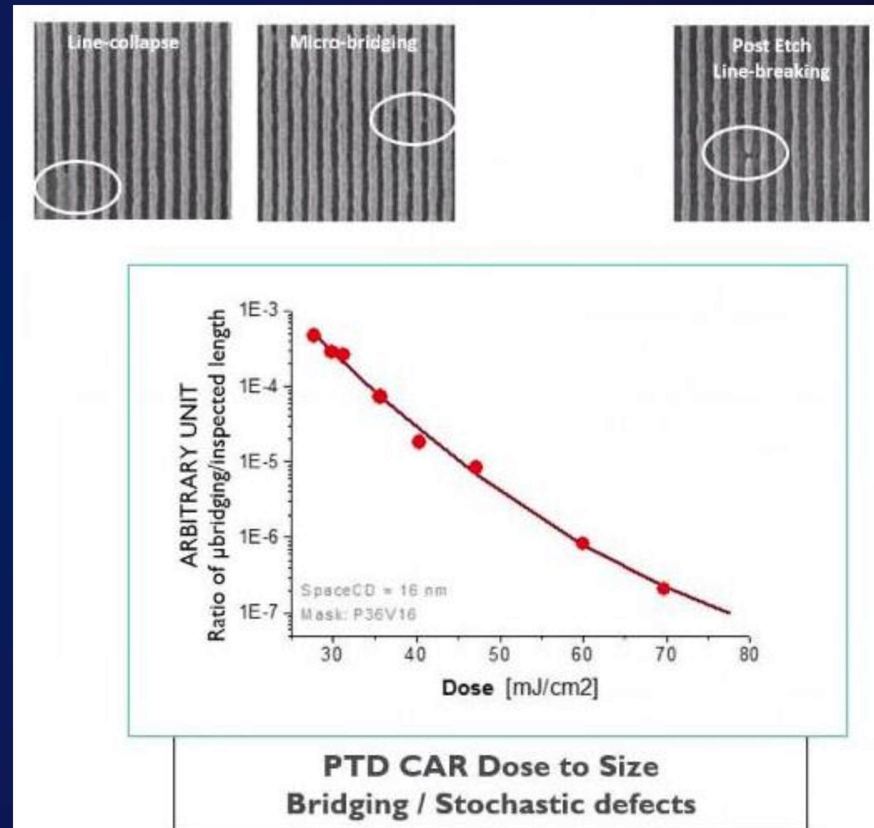
EUV may not save cost!



Resist Performance trade off Throughput!

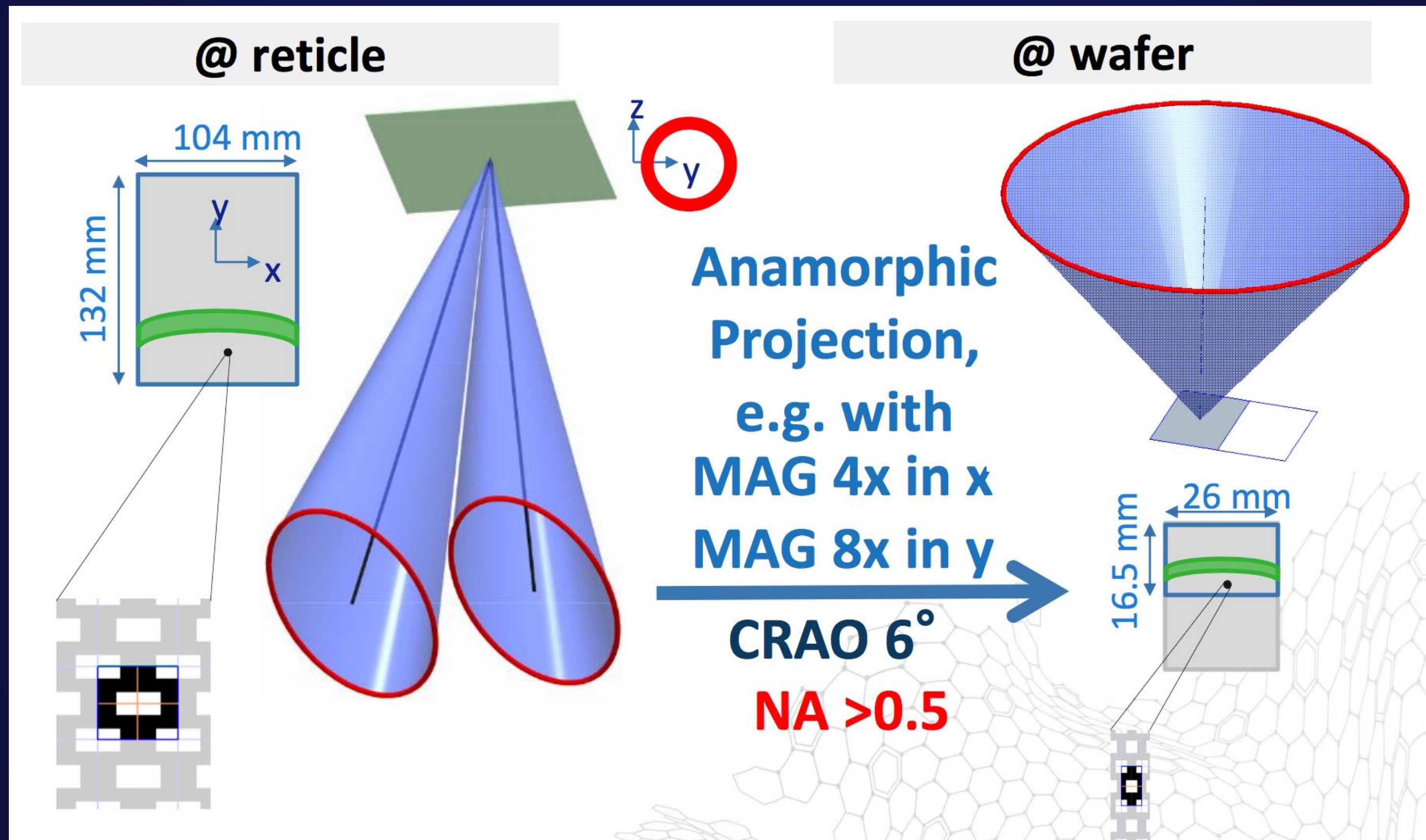


Jack Chen, EUVL Symposium 2015



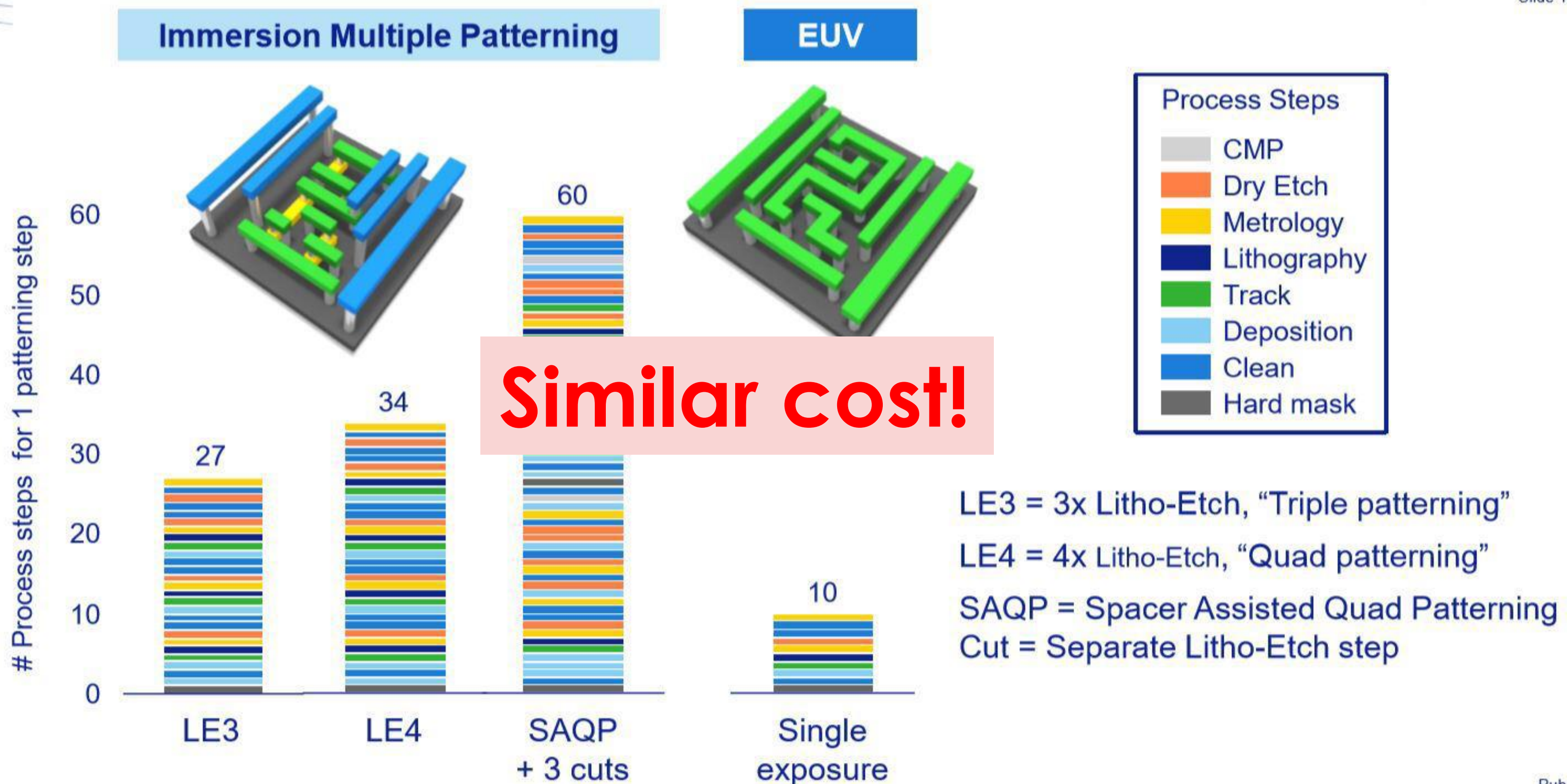
Peter De Bisshop, IMEC 2015

Hi-NA EUV has a half field!



➔ Half field or double masks!

EUV simplify process and shorten cycle time!



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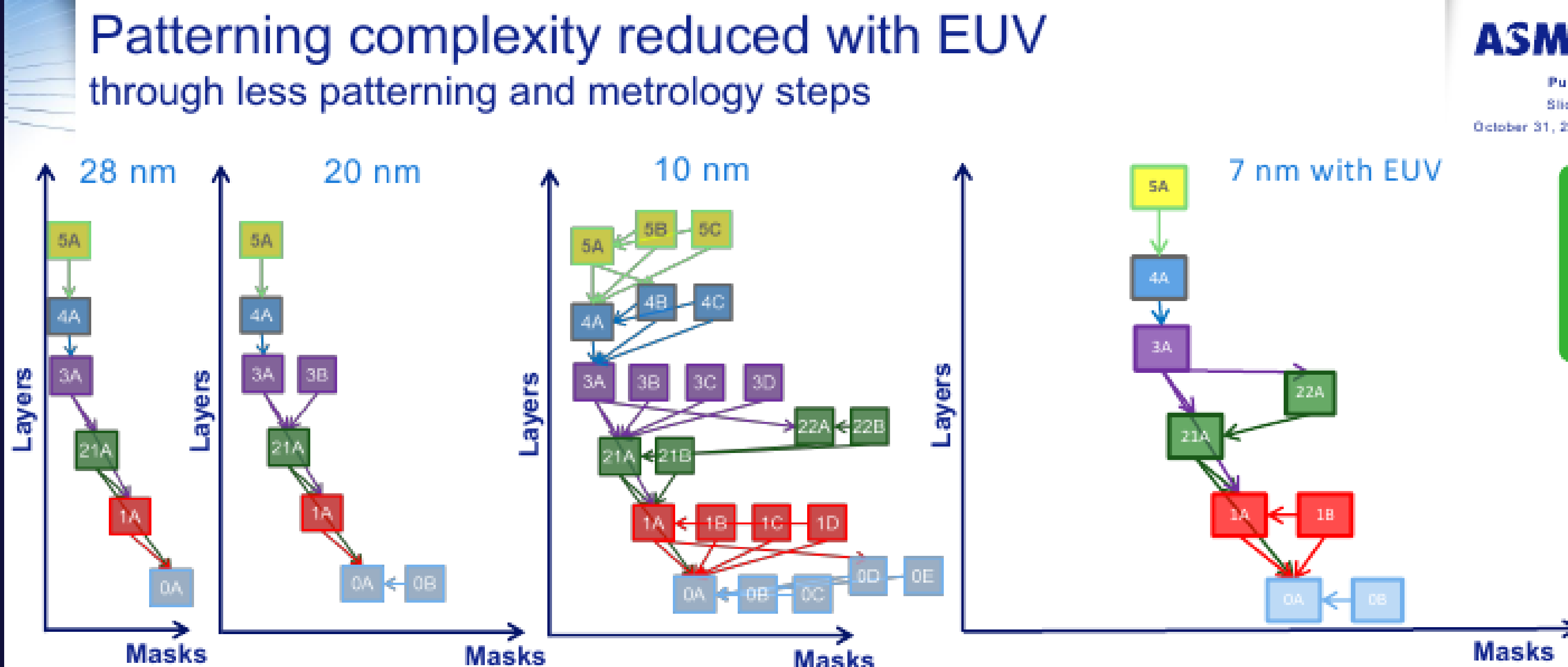
EUV simplify overlay tree!



Node	28 nm	20 nm	10 nm	7 nm all immersion	7 nm all EUV
#: lithography steps	6	8	23	34	9
→: critical alignment overlay step	7	9-11	36-40	59-65	12

- "The limit of lithography will not be in resolution but in economy."

  – Dr. Burn J. Lin, in 1987

- "The devil is in the mask!"

  – Dr. Burn J. Lin, in 2007

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All about **Money / Time**!

- R&D, Capital investment and Readiness in time
- Wafer cost
- Cycle time
- Mask cost

$$Contribution\ of\ Capital\ to\ Wafer\ cost = \frac{Capital\ depreciation}{Throughput \times Uptime}$$

$$Contribution\ of\ Mask\ to\ Wafer\ cost = \frac{Mask\ cost}{Wafers\ \#}$$

Transistor cost?

Chip/function/device price!

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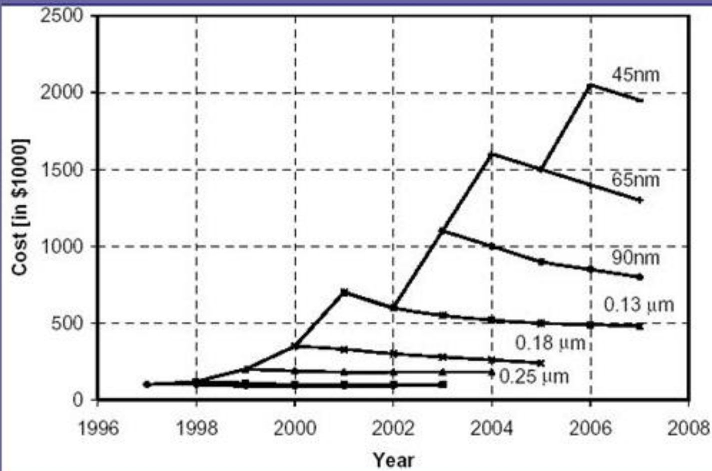
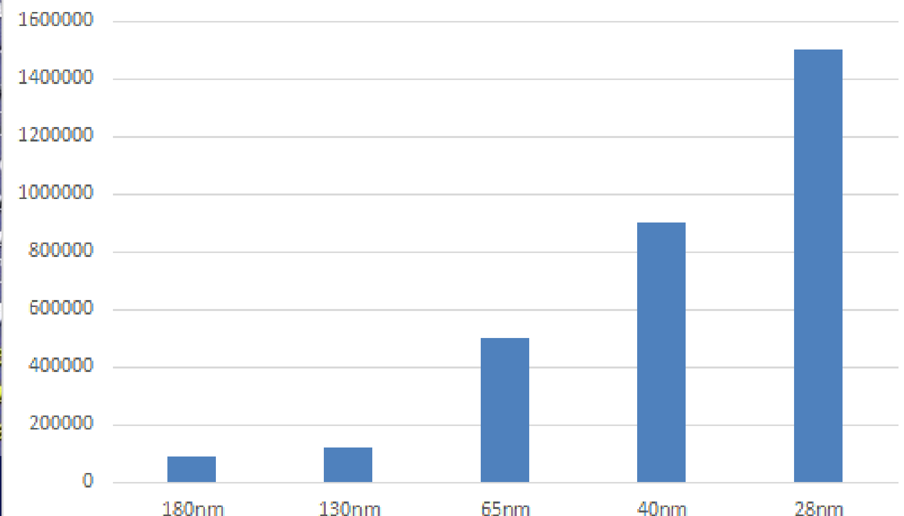
Escalating cost of a mask-set

Process (microns)	2.0	0.8	0.6	0.35	0.25	0.18	0.13	0.1
Single Mask Cost ($K)	1.5	1.5	2.5	4.5	7.5	12	40	60
# of Masks	12	12	12	16	20	26	30	34
Mask Set cost ($K)	18	18	30	72	150	312	1000	2000



- A f ma $1-
- Ro AS 7 y *An Sa "T key*
- ***Ne wh sha***



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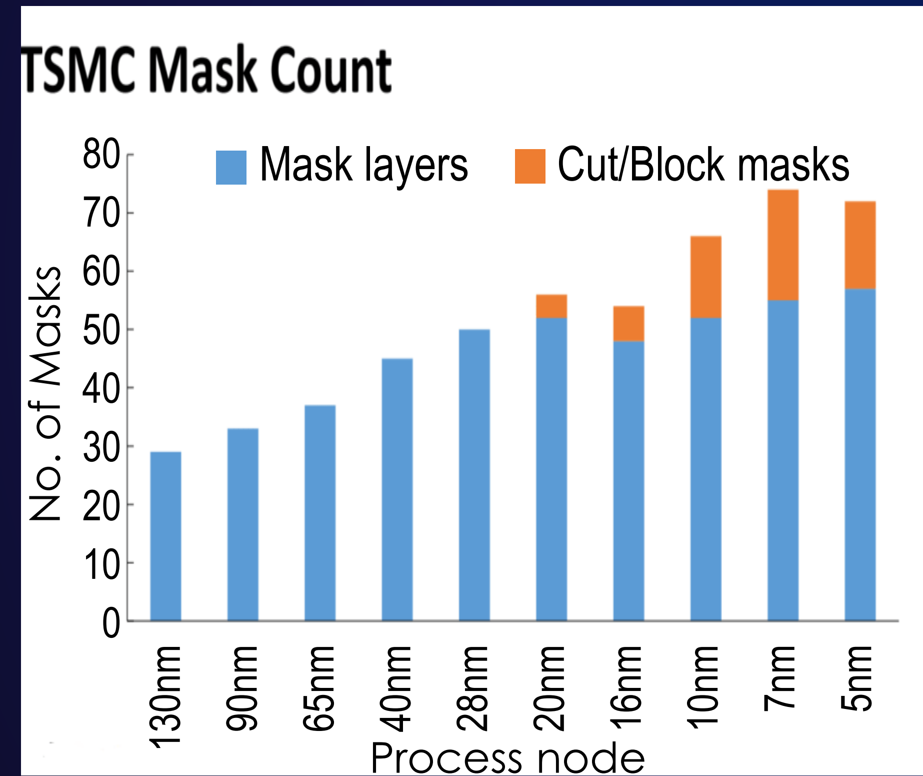
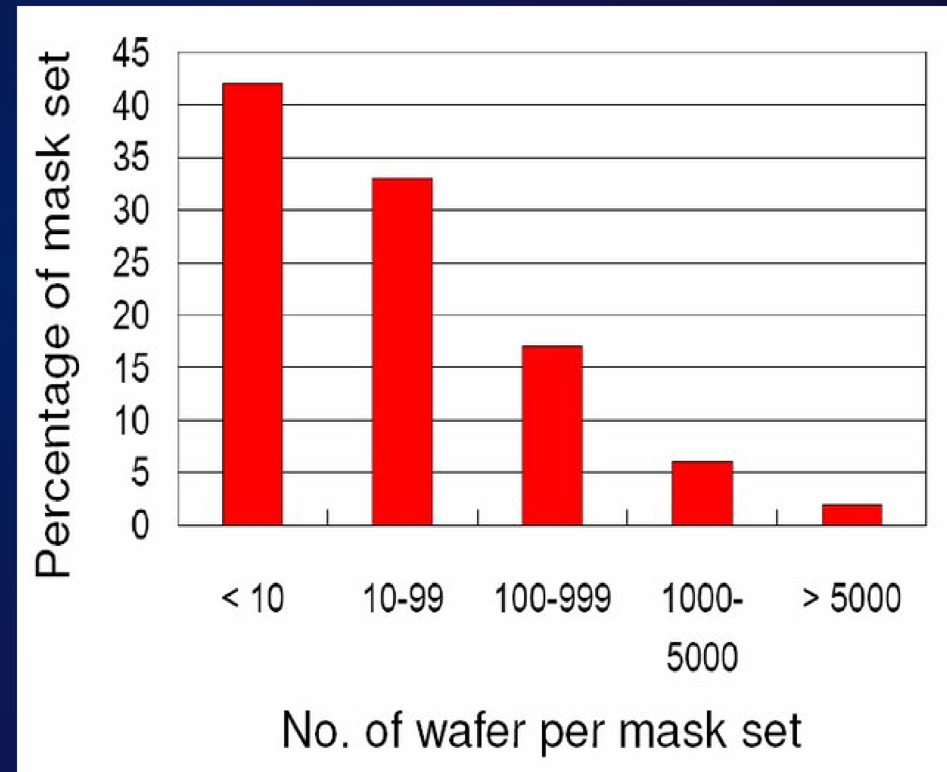
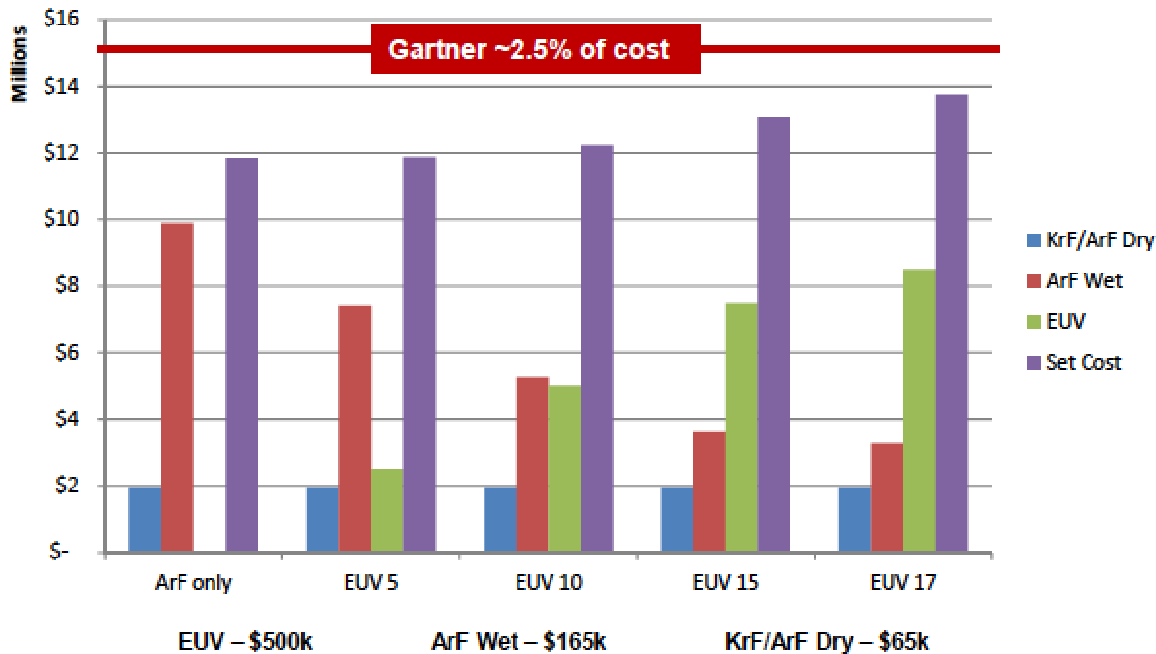
TSMC Mask and Wafer Counts





Source: IC Knowledge LLC

Less Masks doesn't save money!



General industry consensus:

- Cost of EUV mask <= Cost of 3x ArFi masks

Life Cycle of a EUV Mask

Anthony Yen EUVL Symposium 2013

OOS: Out of Spec; FS: Front Side; BS: Back Side

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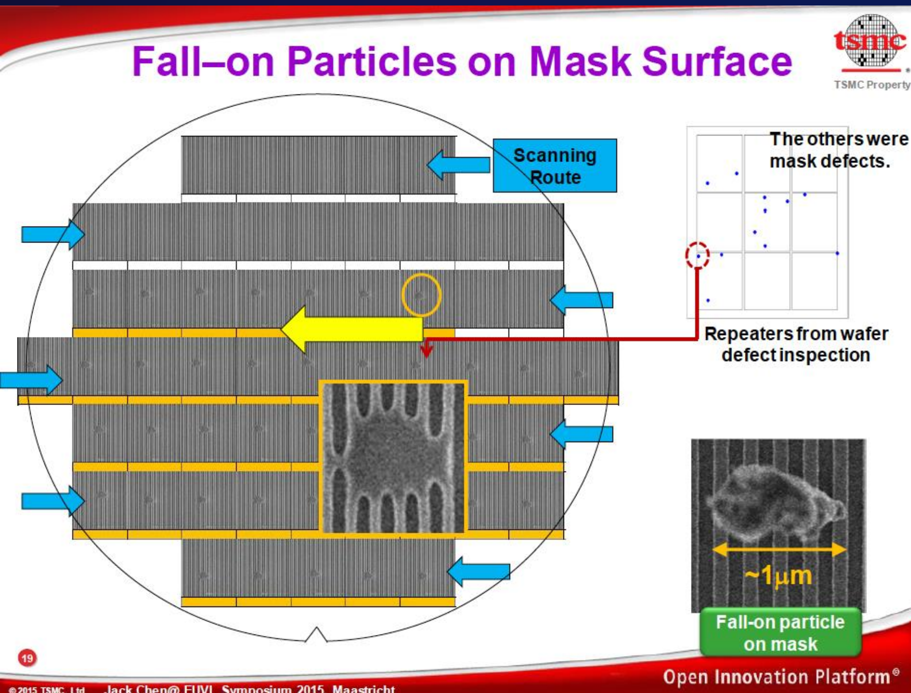
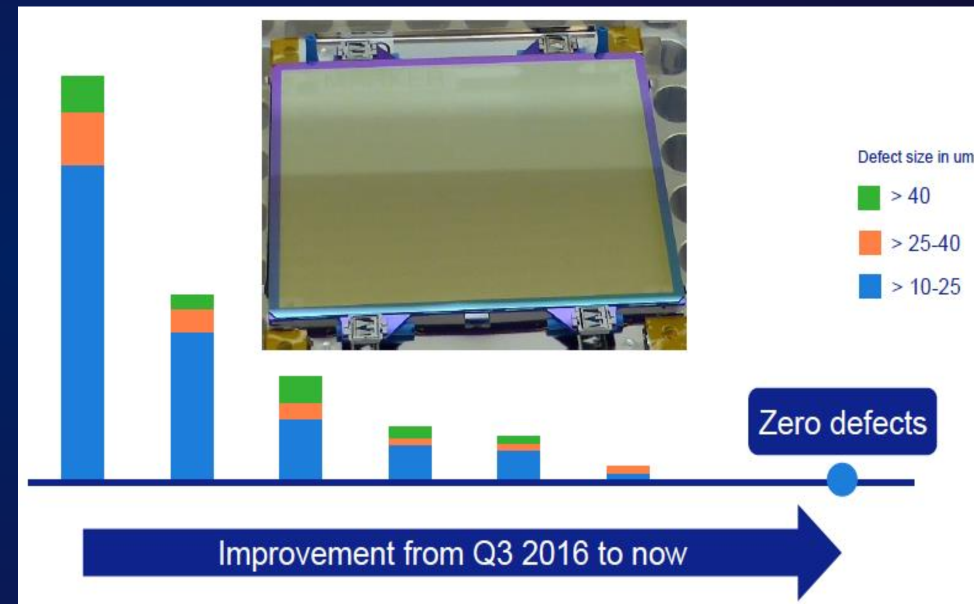
Open Innovation Platform®

EUV Pellicle Life Time is concern!

Jack Chen, EUVL Symposium 2015



EUV Pellicle: film produced without printing defects. -- M. Lercel, 2017



- The fragile <30-nm membrane has to be strong enough to against high G-force, thermal loading, and H*!
- Broken pellicle becomes flake particles inside the scanner
- Re-mounting pellicle takes long time due to inspection!

Unhealthy Eco-System!

- Sole (EUV) scanner supplier, and very expensive EUV scanner
- Only 3 giant ICMs
- Mask inspection, pellicle, and new resists still need further development
  - Can only pre-test at IMEC and a few academic sites
  - High risk in developing new materials
- Extremely high mask cost for new product development and prototyping

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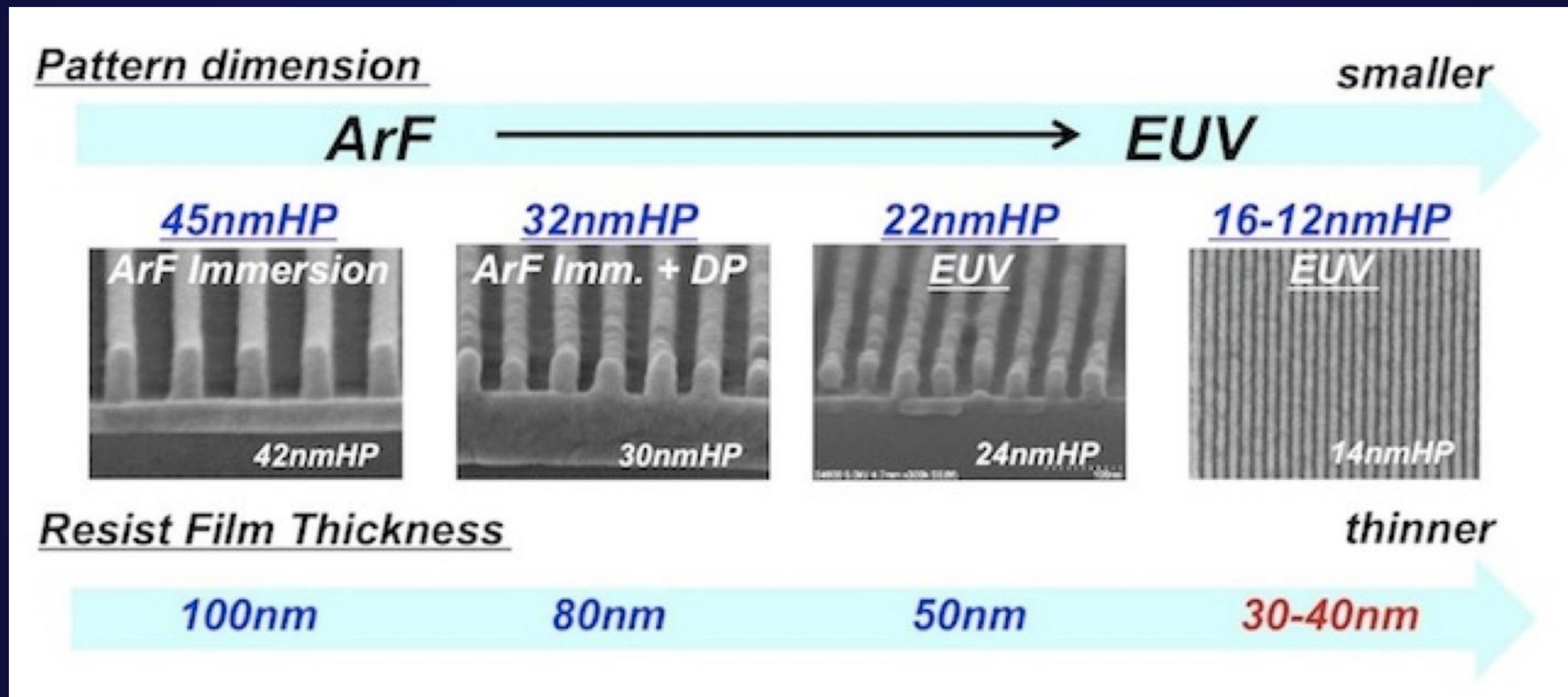
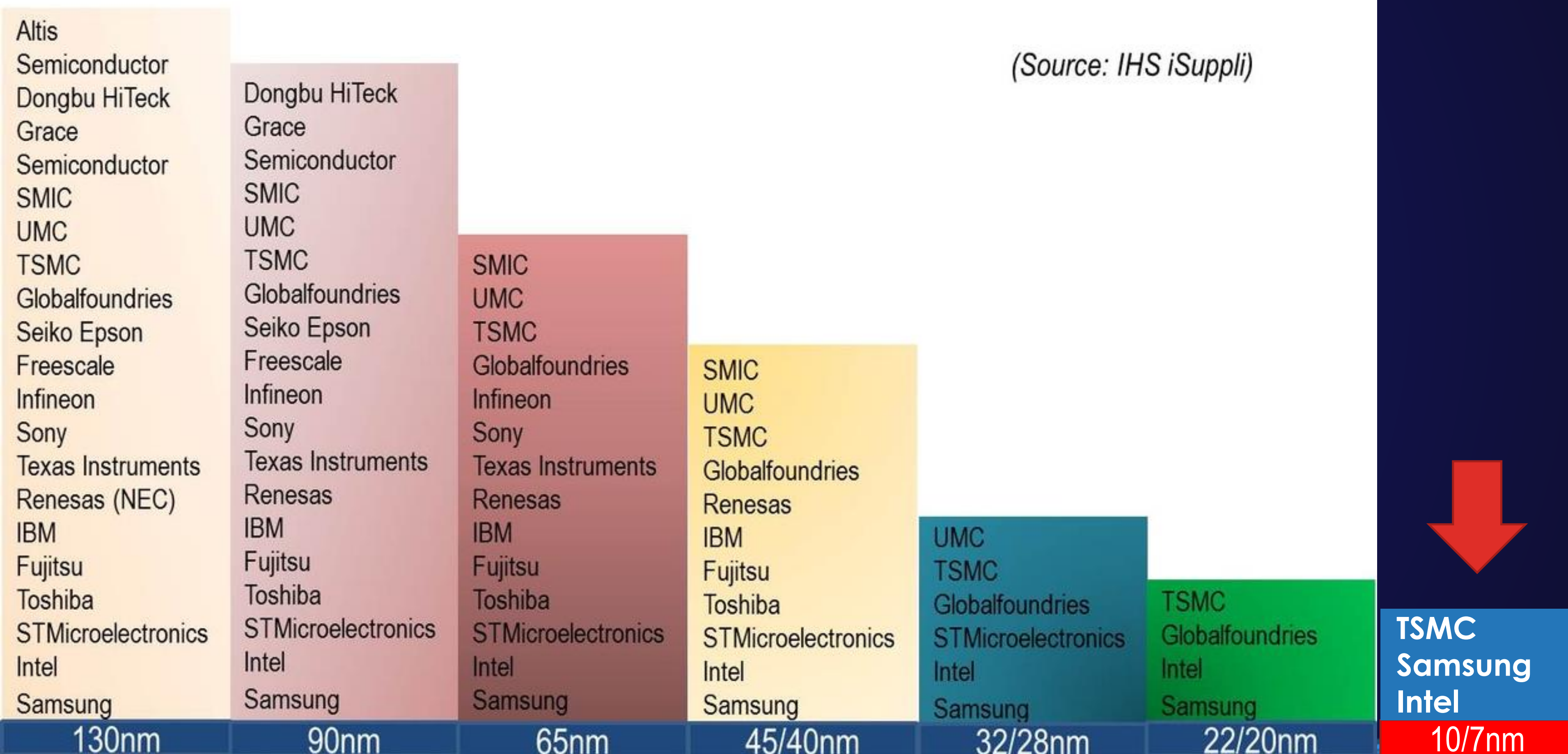
Stronger resist is required, but…



(Source: JSR Micro)

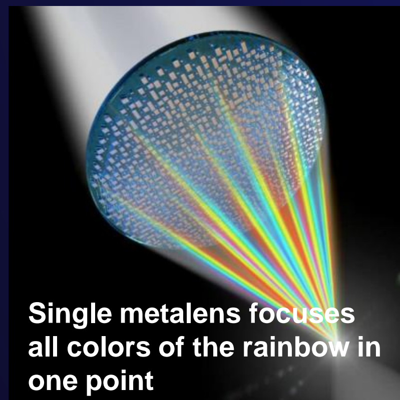
Risk or Opportunity?



Demand for Maskless Lithography

- Niche applications for < 100nm Lithography
  - Prototyping and low-volume special applications using existing 8” or 12” Si technology
  - 5G mmWave, RFID on III-V wafers
  - Photonics, flat optics, spectral filters
  - Large size devices, ex: NIL mold

Low volume for each custom design!


Single metalens focuses all colors of the rainbow in one point

Sub-50nm Wire Grid Polarizers (WGP)

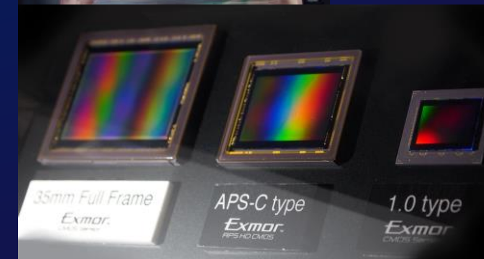
Second Polarizer
First Polarizer

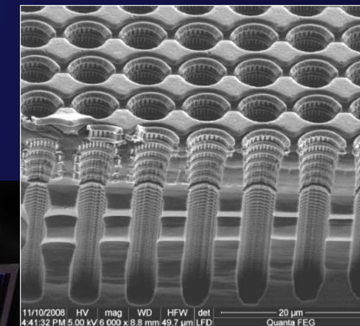
Traditional Organic Polarizer
Absorptive film that is laminated on LCD glass
Backlighting

Aluminum lines of a WGP
50nm half pitch

Large Area Wire Grid Polarizer
Brighter and higher contrast with less backlighting
- Improved Contrast Ratio
- Longer Battery Life
- Thinner Display
- Reduced BoM

Backlighting




Mapper Blanker chip

Unique ID for Chip Security

Data security

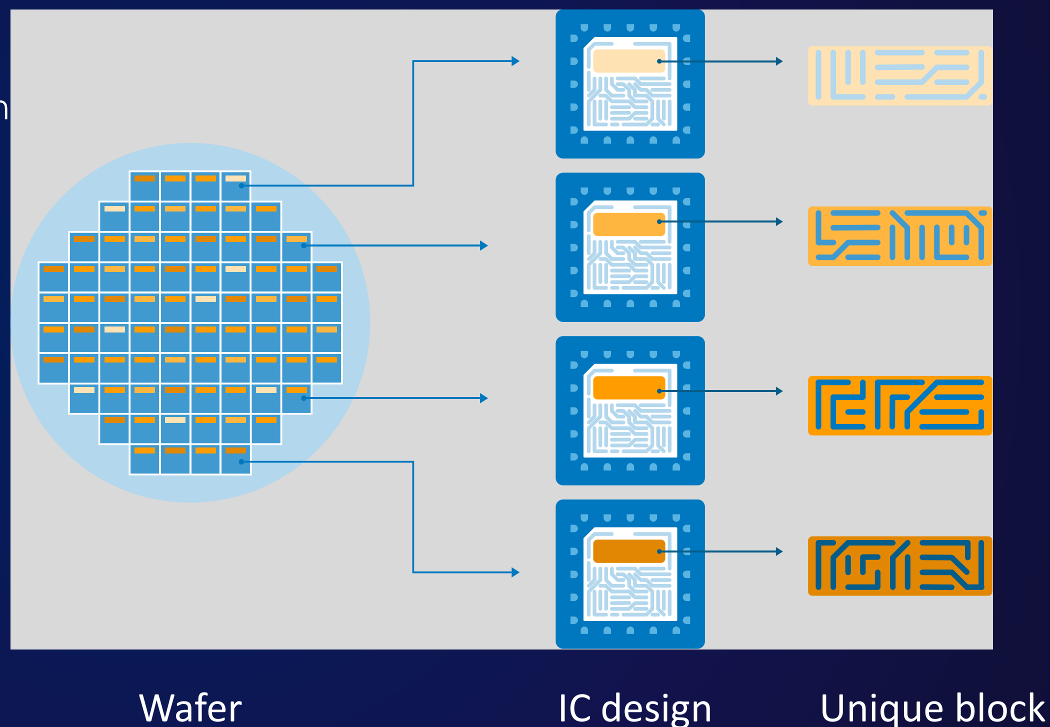
- Industrial infrastructure
- IoT gadgets
- Digital rights managemen
- Mobile storage
- Smart cards

Traceability

- Automotive
- Aviation
- Medical
- Postal
- Retail

Anti-counterfeiting

- Defense spare IC's for 20+ year old equipment
- Luxury goods
- Bank bills, coins

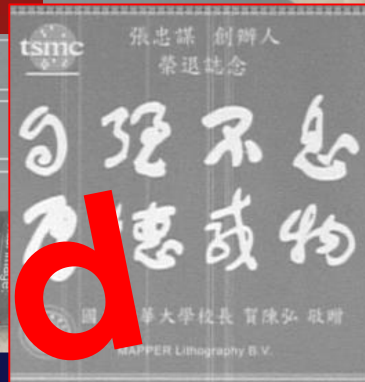


MEB300 University-Industry Alliance

Since Oct'17

Experts

by FLX1200



Member companies including ICMs, III-V foundry, Optronics…

Project Closed

Security IC for IoT, Foundry service for prototyping

Leading-edge Suppliers and tools

Location: NTHU, Hsinchu

Summary

- Giving enough money and time, with all experts and efforts in this SPIE society, any lithography issues can be resolved!
  - Impressive progress of EUV pellicle and NIL!
- EUV, mask-based lithography is a game for rich, big companies and only good for high volume products.
- Considering economy, if no absolutely advantage shown in time, then the existing technology with the least change will most likely do.
- To incubate the innovative niche applications, maskless lithography with resolution <50nm is crucial.

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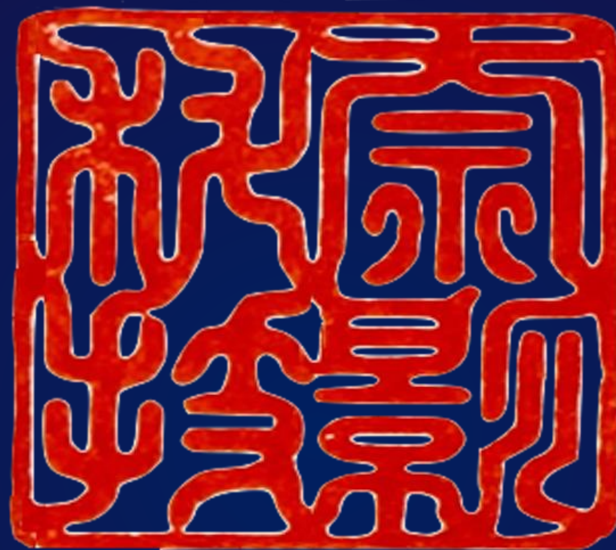

Thank you for attention!