PRESS RELEASE

LETI SHOWS THE WAY TO FABRICATING CMOS DEVICES FOR 5-NM NODE USING NANOWIRE TECHNOLOGY BRICKS

IEDM 2016 Papers Demonstrate Novel Responses to Problems Of Performance and Parasitic Capacitances

SAN FRANCISCO – Dec. 5, 2016 – Leti, an institute of CEA Tech, presented two papers at IEDM 2016 today that demonstrate its ability to provide industry with all the elements required for building a competitive 5-nm node with nanowire architectures.

Nanowire architectures are seen as the best candidates for that node, and Leti is addressing some of its biggest challenges, such as of performance and parasitic capacitances. Its results suggest that strain can be introduced into stacked nanowire and that parasitic capacitances can be reduced thanks to inner spacer integration.

The paper, "Vertically Stacked-Nanowires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source/Drain", is the first demonstration of functional devices with SiGe source and drain to induce strain in the channel to boost performance, and inner spacer to reduce parasitic capacitances. Both building blocks are required for the 5-nm node. This MOSFET architecture extends the scaling limits of CMOS technology, and is also seen as a possible extension to FinFET.

Leti, at IEDM 2008, was among the world's first organizations to report stacked nanowire and nanosheet results.

The second paper, "NSP: Physical Compact Model for Stacked-planar and Vertical Gate-All-Around MOSFETs", presents a predictive and physical compact model for nanowire and nanosheet gate-all-around MOSFETs.

"This is the first compact model, or SPICE model, that can simulate stacked nanowire and nanosheet devices with various geometries," said Olivier Faynot, Leti's microelectronics section manager and a co-author of both papers. "It also enables the simulation of vertical nanowire, which is one of the key achievements of this model."

The paper presents a physically based SPICE model for stacked nanowires that can enable circuit designers to accurately project their existing circuits into the 5-nm node, and investigate novel designs.

About Leti (France)

As one of three advanced-research institutes within the CEA Technological Research Division, Leti serves as a bridge between basic research and production of micro- and nanotechnologies that improve the lives of people around the world. It is committed to creating innovation and transferring it to industry. Backed by its portfolio of 2,800 patents, Leti partners with large industrials, SMEs and startups to tailor advanced solutions that strengthen their competitive positions. It has launched 59 startups. Its 8,500m² of new-generation cleanroom space feature 200mm and 300mm wafer processing of micro and nano solutions for applications ranging from space to smart devices. With a staff of more than 1,900, Leti is based in Grenoble, France, and has offices in Silicon Valley, Calif., and Tokyo. Follow us on www.leti.fr/en and @CEA_Leti.

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