eMRAM: From Lab to Fab

CEA-Leti Memory Workshop 2017
June 27, 2017

Dave Eggleston, VP Embedded Memory

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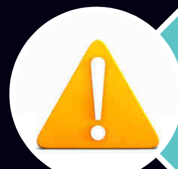
Markets & Requirements


eMRAM Limitations

eMRAM Enabling Features

Competing Solutions

Cost Effective Manufacturing

Future eMRAM

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Markets & Requirements
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High Volume New Markets Driving the Opportunities

All data, except for 5G, refer to 2020.

Sources: 5G: Mobile Experts; Automotive and Mobility: Average of IHS and other market research firm data; AR/VR: GLOBALFOUNDRIES analysis of Goldman Sachs, Bank of America, and some market research data; Commercial Drones, Data Centers, and IoT: GLOBALFOUNDRIES analysis and interpretation of market research data; Robotics: GLOBALFOUNDRIES analysis of Bank of America and some market research data.

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High Volume New Markets Driving the Opportunities

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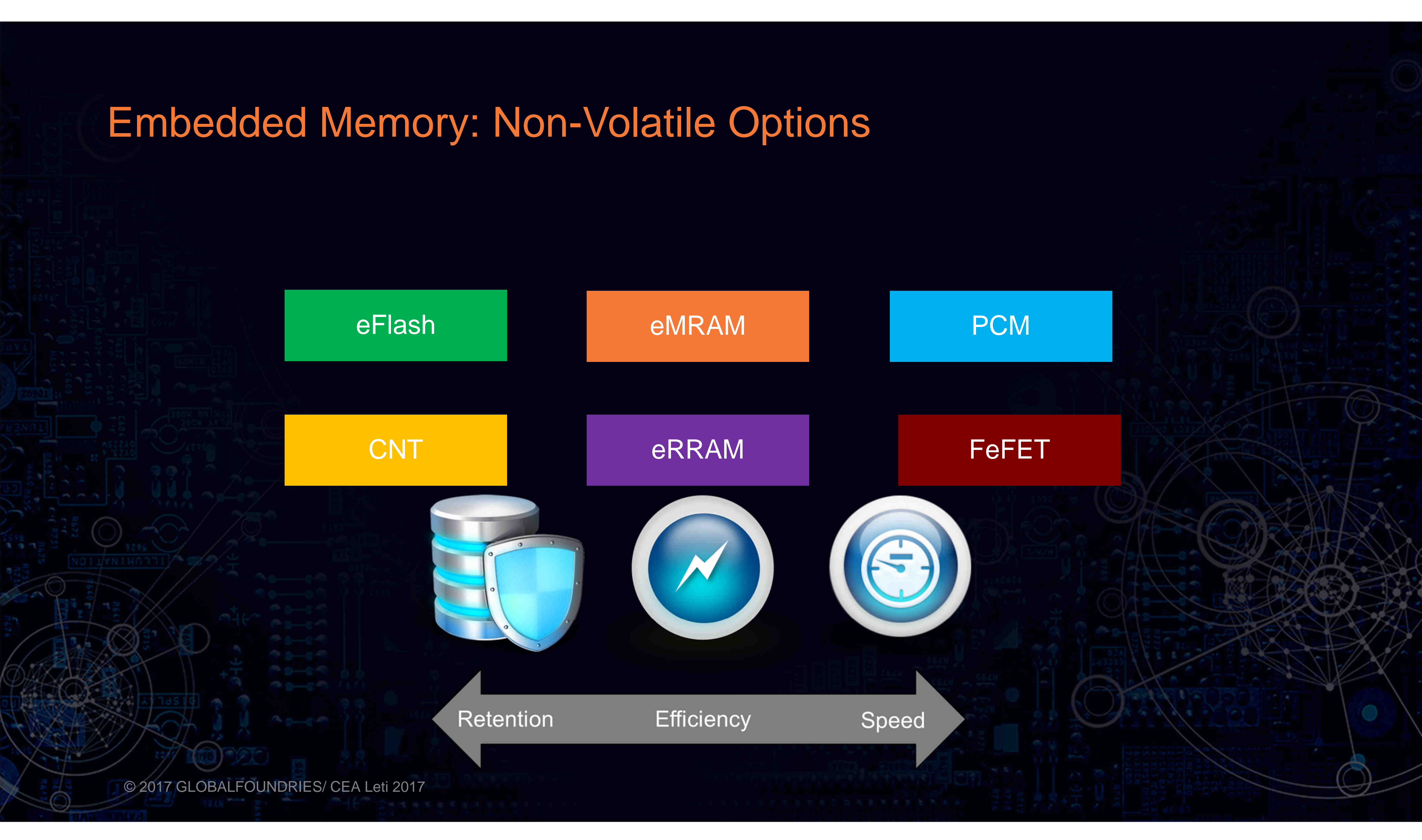

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Embedded Memory: Non-Volatile Options

eMRAM

Pro: speed, endurance, versatility, masks
Con: complex stack, data retention

eFlash

Pro: data retention
Con: speed, masks

eRRAM

Pro: simple stack, masks
Con: speed, endurance, data retention

Retention ← Efficiency → Speed

Not (yet) Suitable for eNVM	PCM Specialized
CNT Immature	FeFET Immature

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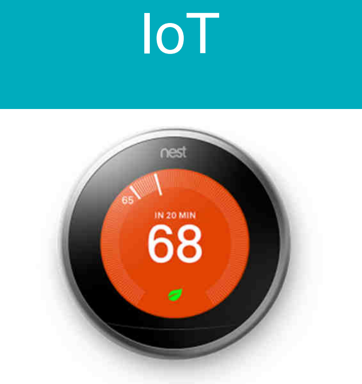
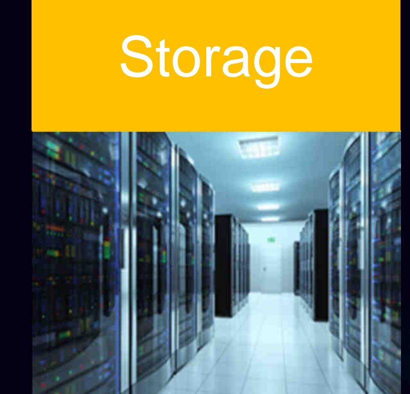
Embedded Memory: Application View

Automotive	MCU	IoT	Storage	Compute
				

eFlash → **eMRAM**

Retention ⟵ Efficiency ⟶ Speed

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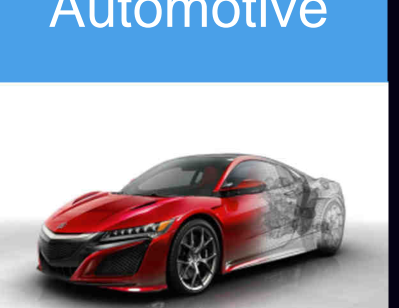
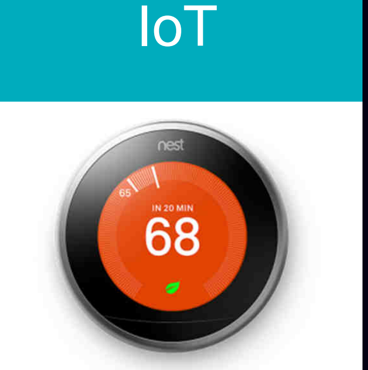
Embedded Memory: <28nm Application View

Automotive

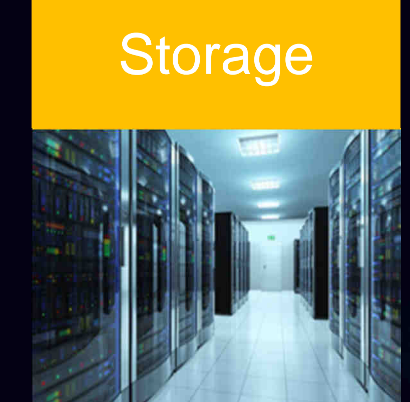


MCU

IoT



Storage



Compute

eMRAM?

Retention — Efficiency — Speed

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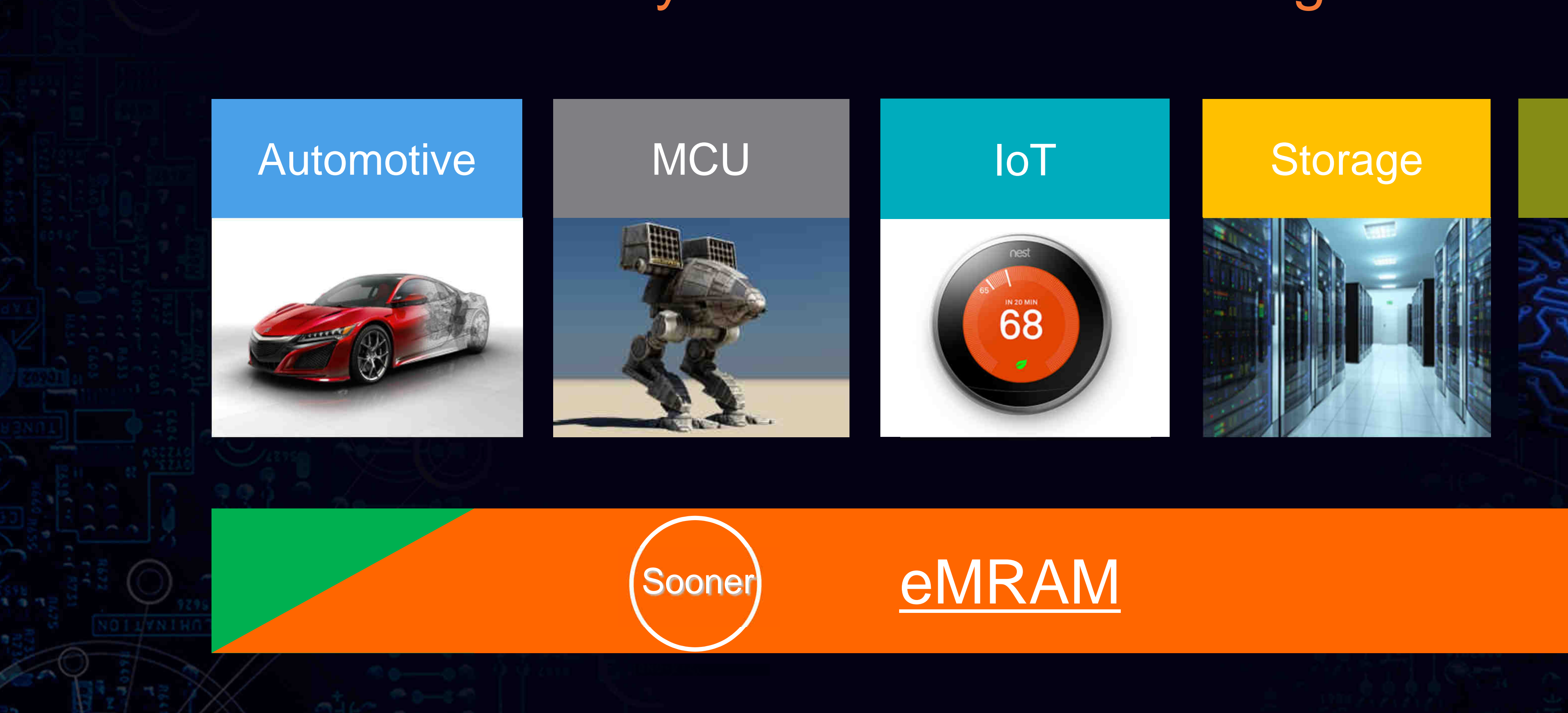
Embedded Memory: eMRAM market timing



Retention Efficiency Speed

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Embedded Memory: eMRAM markets

Automotive	MCU	IoT

68

eMRAM

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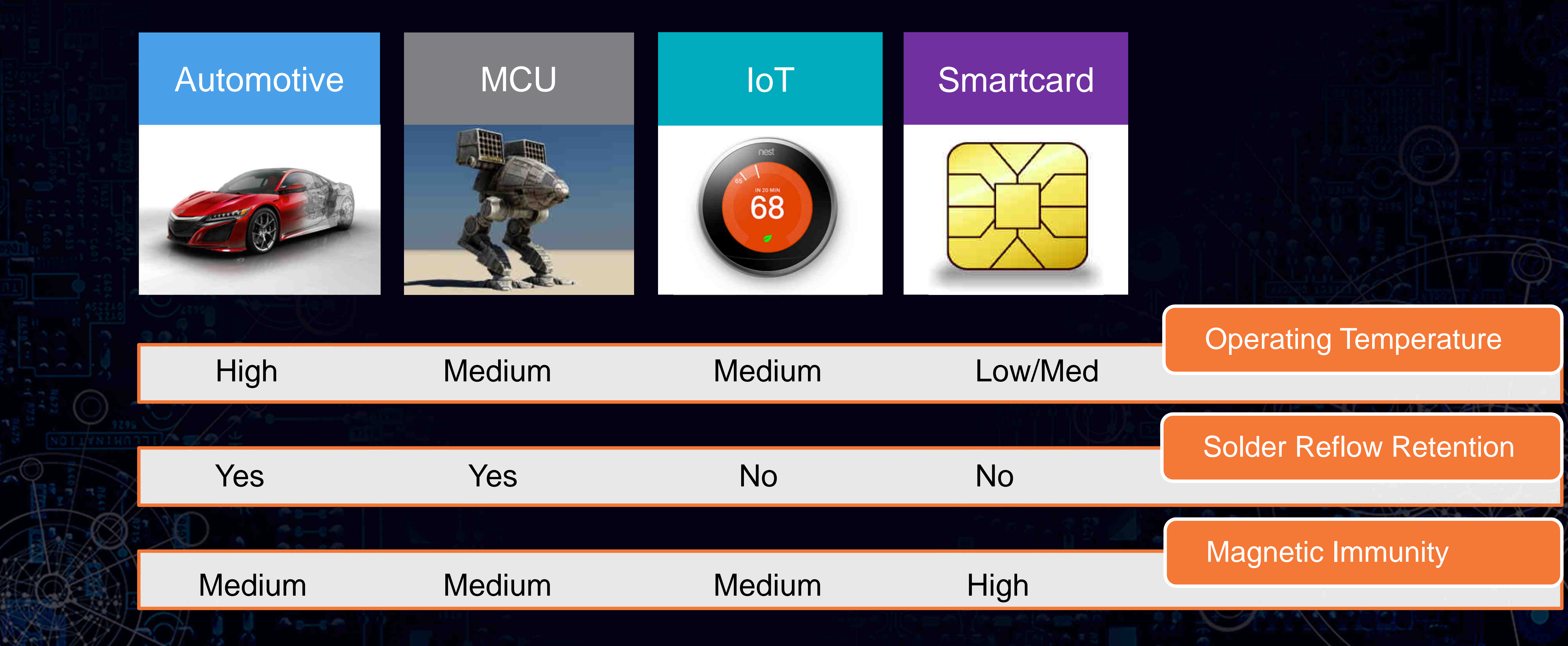
Embedded Memory: eMRAM market requirements



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eMRAM Limitations
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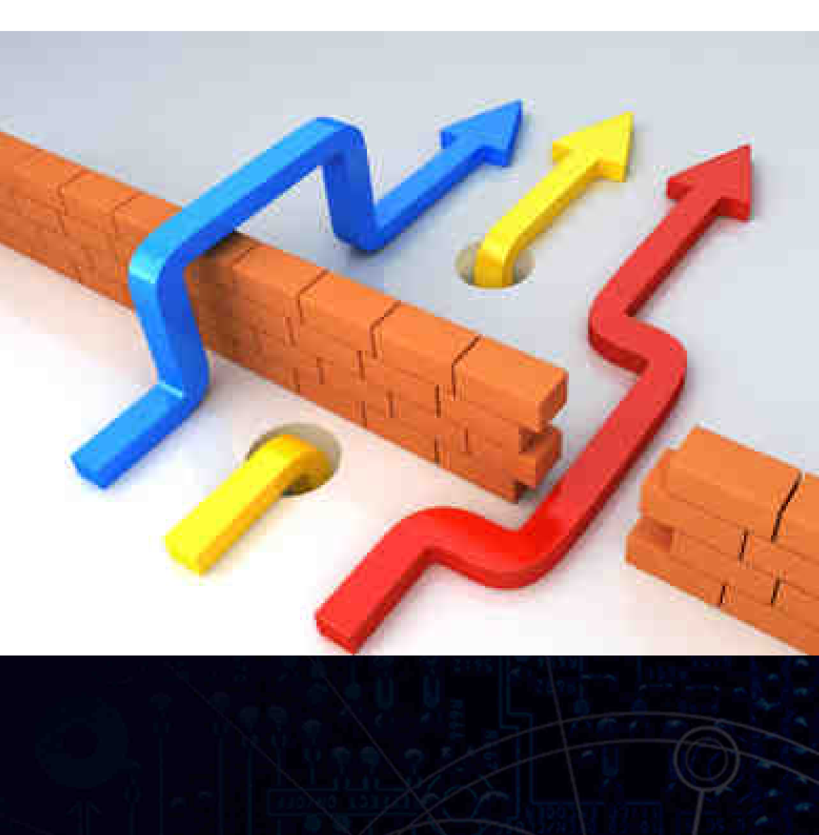
eMRAM Technical Barriers



Operating Temperature

- Small memory window (TMR)
- Larger/complicated sense amp; Slower read speed

Solder Reflow Retention

- 260°C, 5 min data retention
- Must raise Eb, without increasing bitcell size
- Difficult challenge; requires tradeoffs

Magnetic Immunity

- New issue unique to magnetic memory
- 500 Oe – 1000 Oe (100mT) without shielding
- Customer specs still evolving

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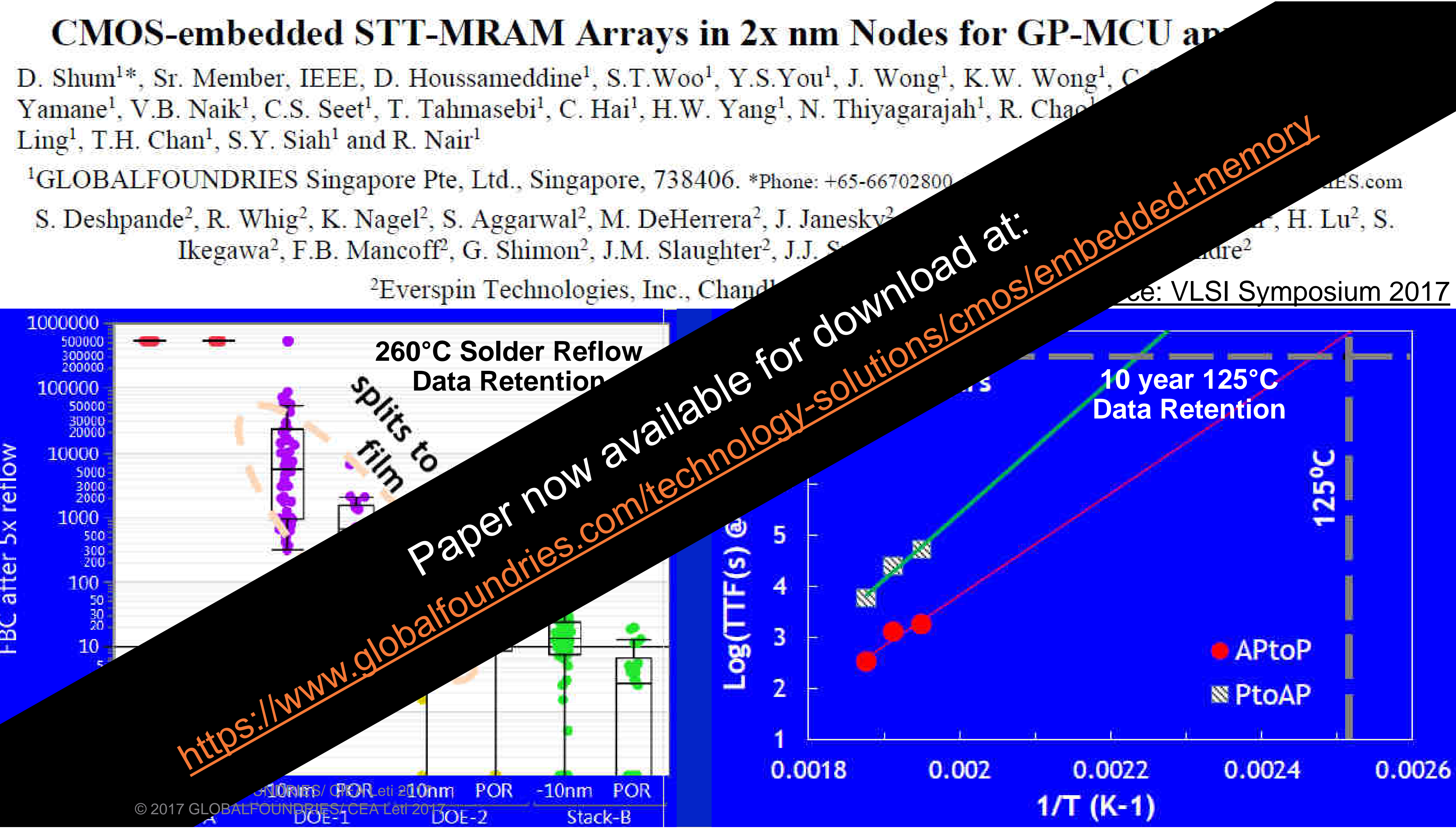

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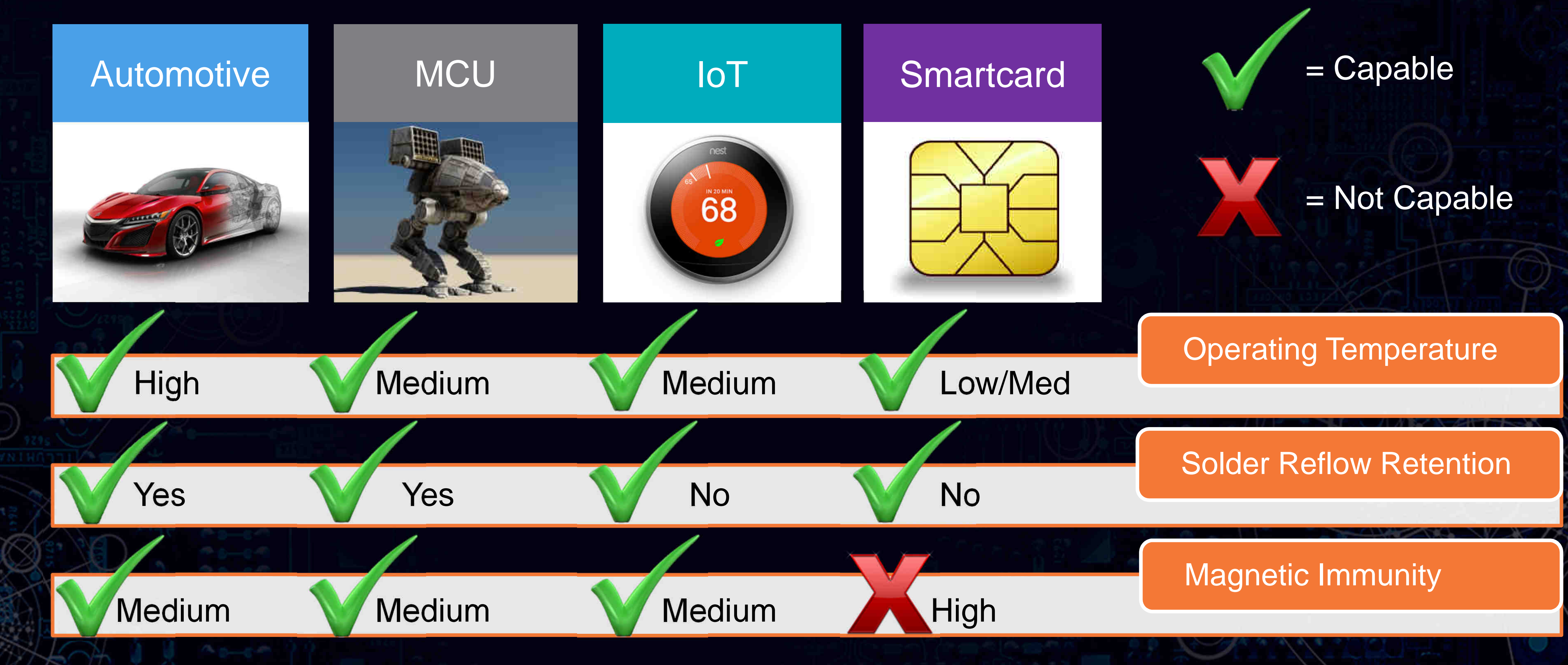
Embedded Memory: eMRAM capabilities



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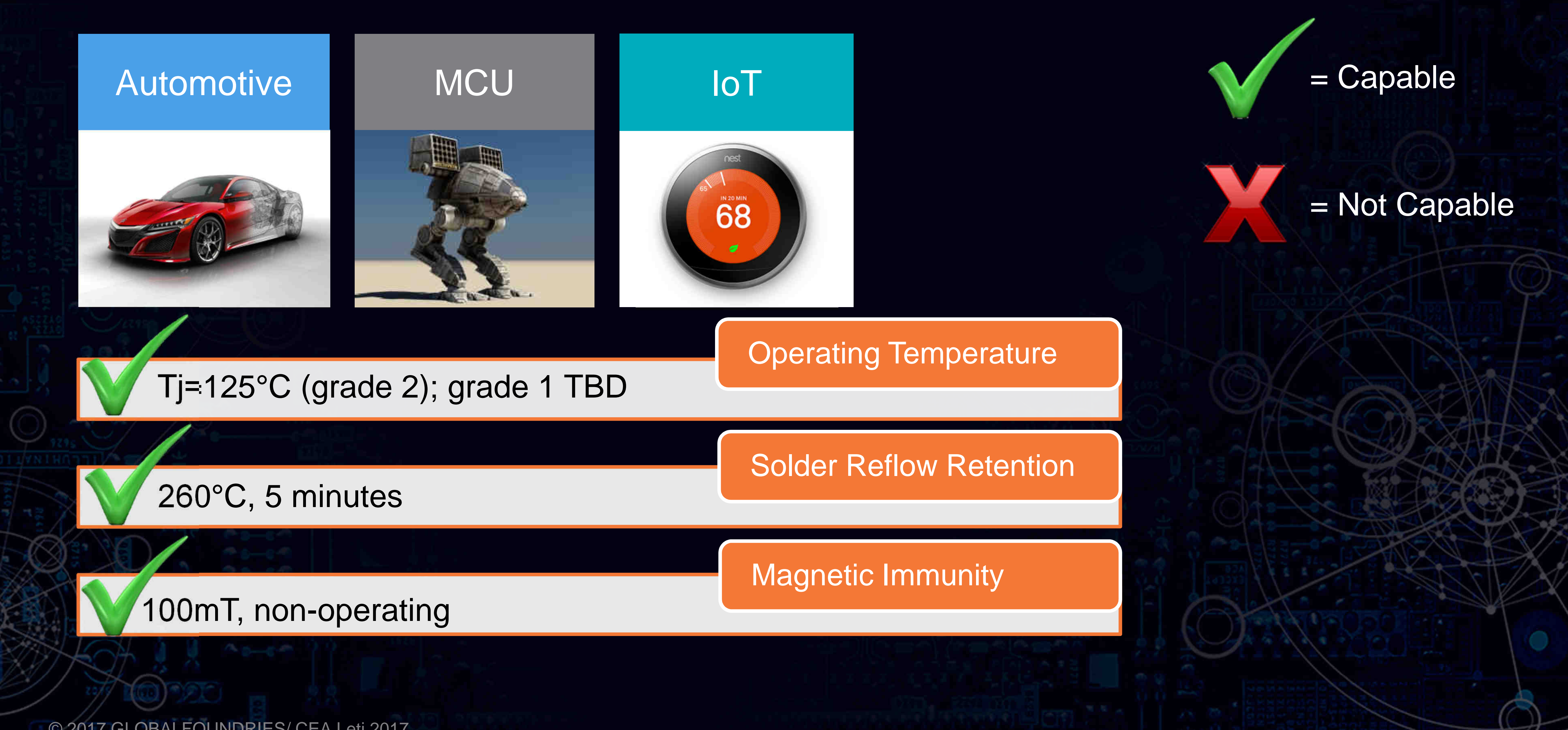
Embedded Memory: eMRAM capabilities



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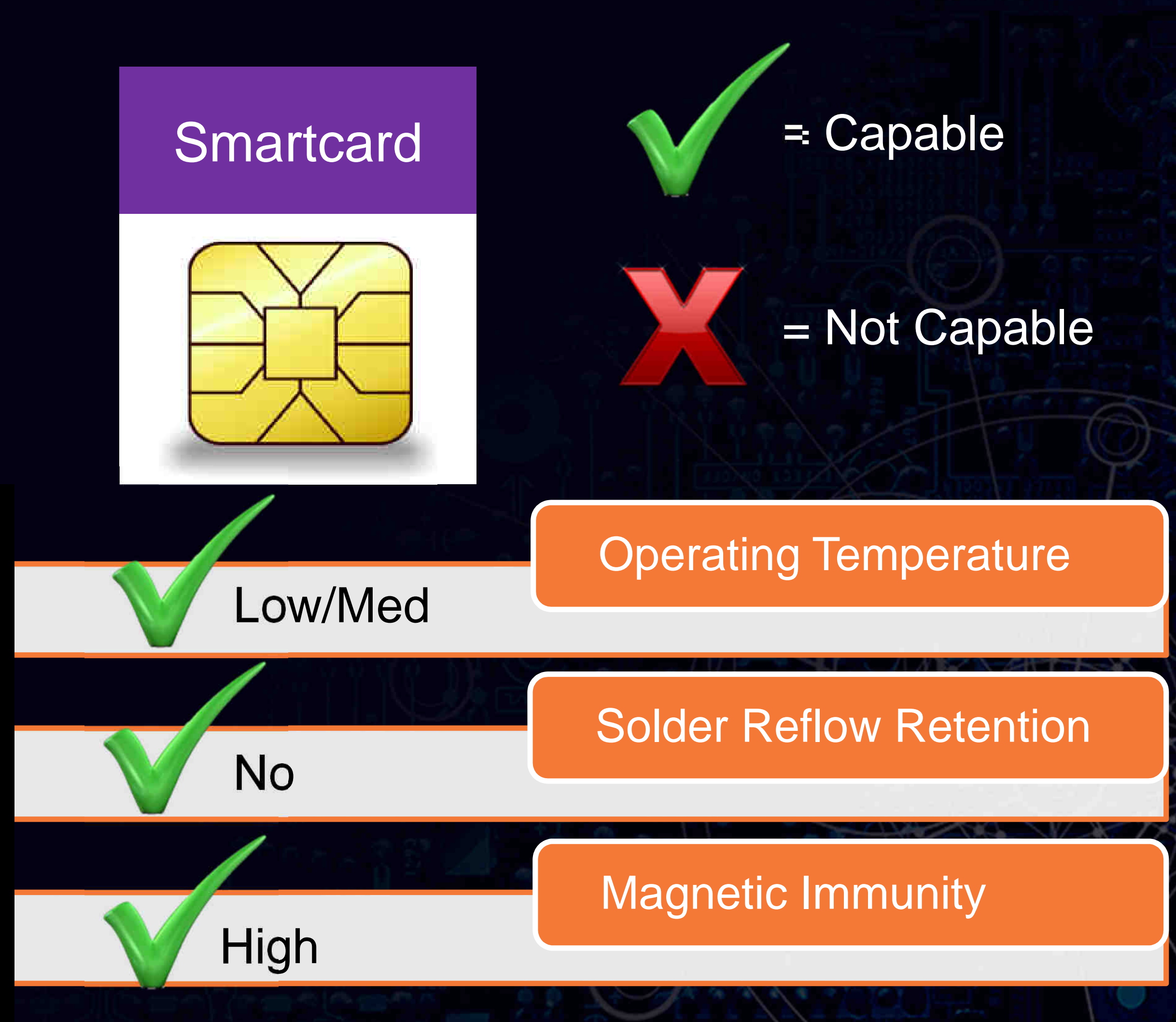
Embedded Memory: non-eMRAM Opportunity



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eMRAM Enabling Features
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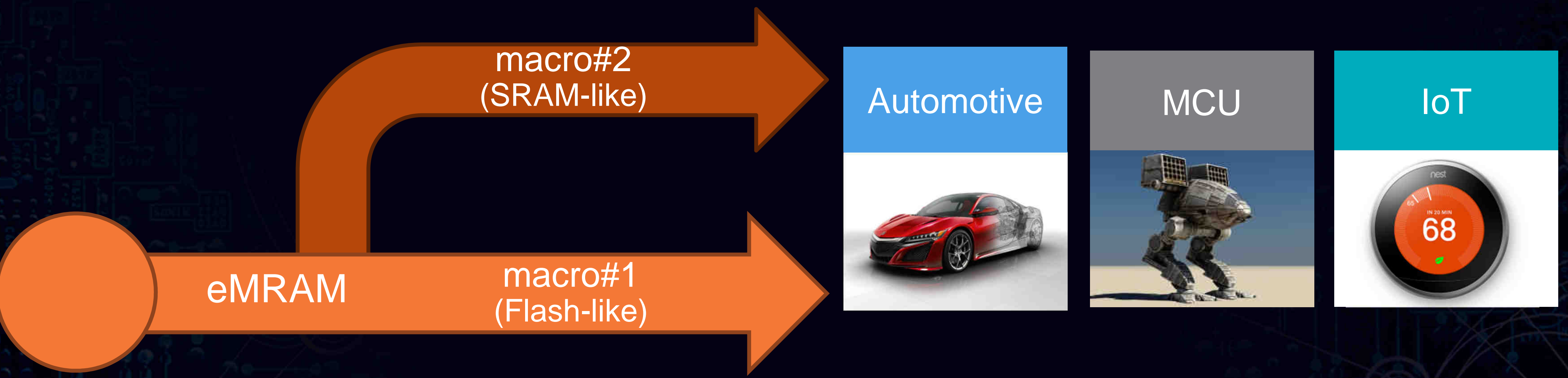
Differentiation using Design



eMRAM: Two functions on the same wafer

- By varying the cell configuration and macro design, both code/data storage and working data functions are achieved!

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Versatility of eMRAM enhances Architecture

Architecture

- Change around eMRAM
- Both code and data/state
- Great for normally-off systems

Energy Savings

- New ultra-efficient memory subsystem
- Power cycle without time or energy penalty
- 1/3rd power of standard SOC

CPU
CPU
CPU
CPU

SRAM
eMRAM (data/state) macro#2

SRAM
eMRAM (data/state) macro#2

SRAM
eMRAM (data/state) macro#2

SRAM
eMRAM (data/state) macro#2

eMRAM (code) macro#1

eMRAM (data/state) macro#2
SRAM

eMRAM (data/state) macro#2
SRAM

GPU

VPU

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	eFlash	eMRAM (macro#1)	eMRAM (macro#2)
Speed (Rd/Wr)	10ns / 20us	25ns /200ns	12.5ns /40ns
Cell size	$40F^2$	$45F^2$	$70F^2$
Endurance	10^5	$\approx 10^8$	$\approx 10^{10}$
Data Retention	>20 years	10 years	10 years
Solder reflow (260C/5min)	Yes	Yes	Yes
Op Temp (Tj)	155C Auto grade 1	125C Industrial/ Auto grade 2	125C Industrial/ Auto grade 2

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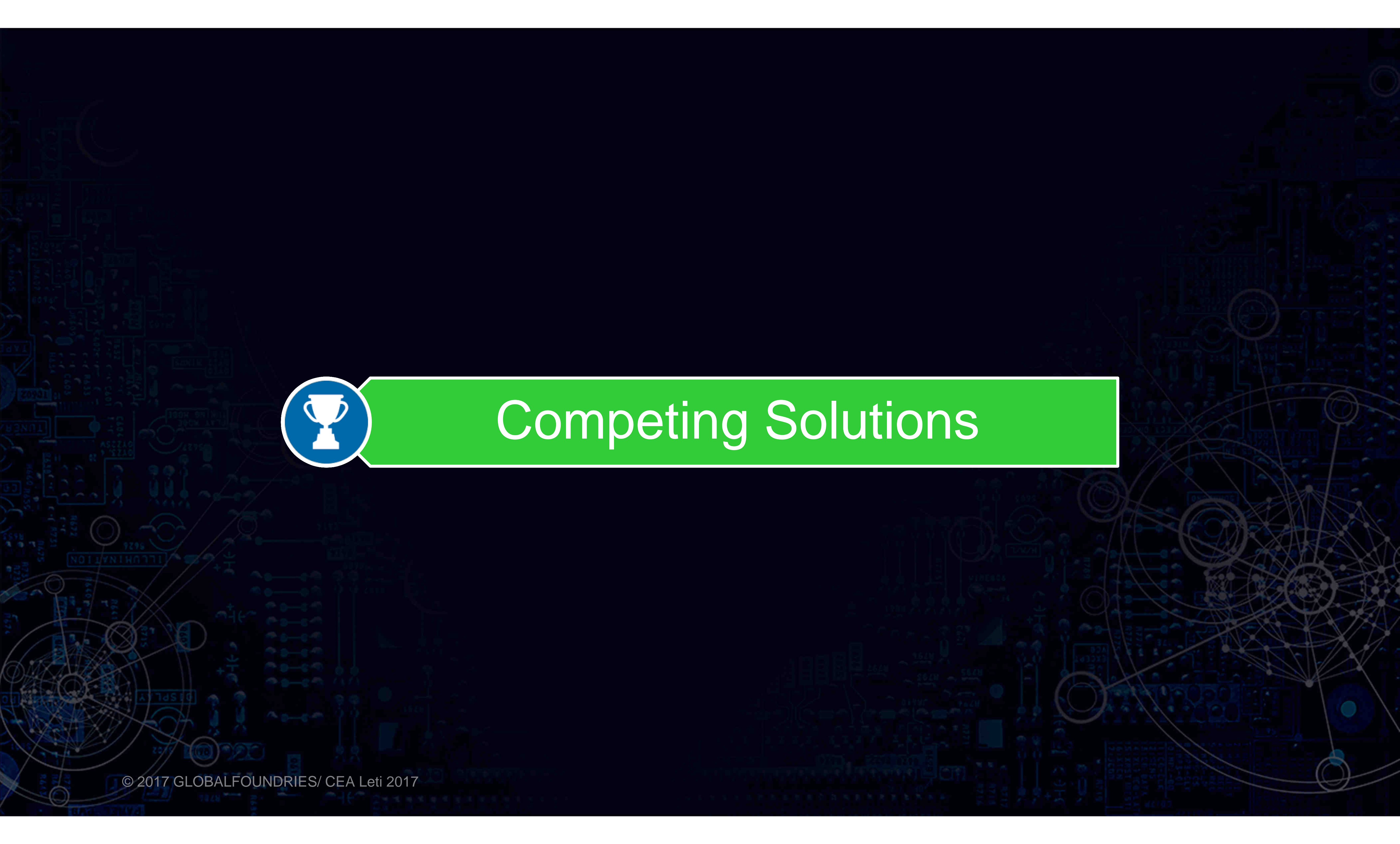

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eMRAM competing solutions

RISK

eRRAM, CNT, FeFET

eMRAM

eFlash

SIP Flash

TTM = Time To Market

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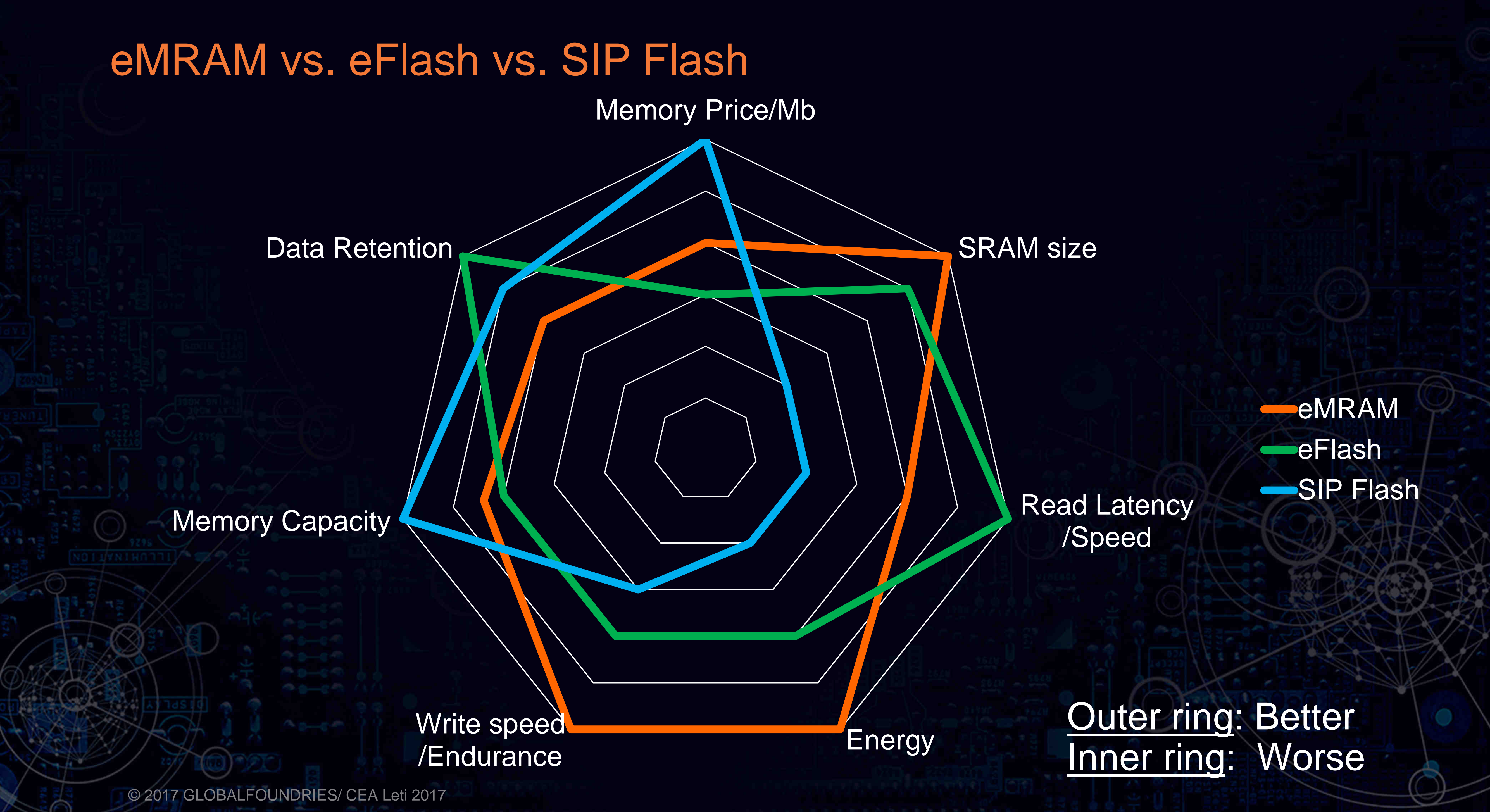

eMRAM vs. eFlash vs. SIP Flash
Memory Price/Mb
SRAM size
Data Retention
Read Latency /Speed
Memory Capacity
Write speed /Endurance
Energy
eMRAM
eFlash
SIP Flash
Outer ring: Better
Inner ring: Worse
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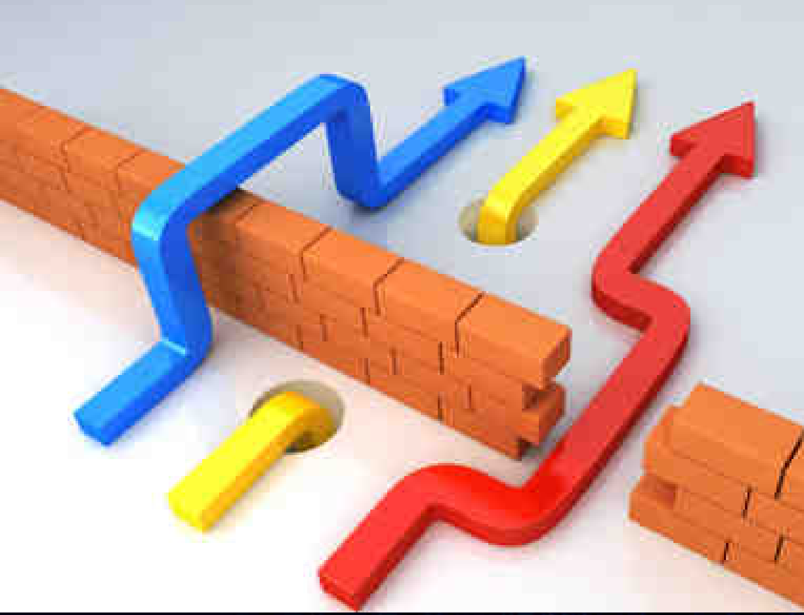
eMRAM Commercial Barriers

Capital Equipment
- Expensive, unique eMRAM CapEx
- Deposition, etch, magnetic anneal

Throughput and Yield
- Must achieve 20+ wph
- Must achieve typical 95%+ yield; <1E^{-6} RBER

Customers
- Will not pay for write speed/endurance benefits
- Want a cost reduction vs. eFlash
- Taking a schedule and reliability risk



"Still a desire for higher throughput and lower complexity/cost"

As an industry, we are not there yet!

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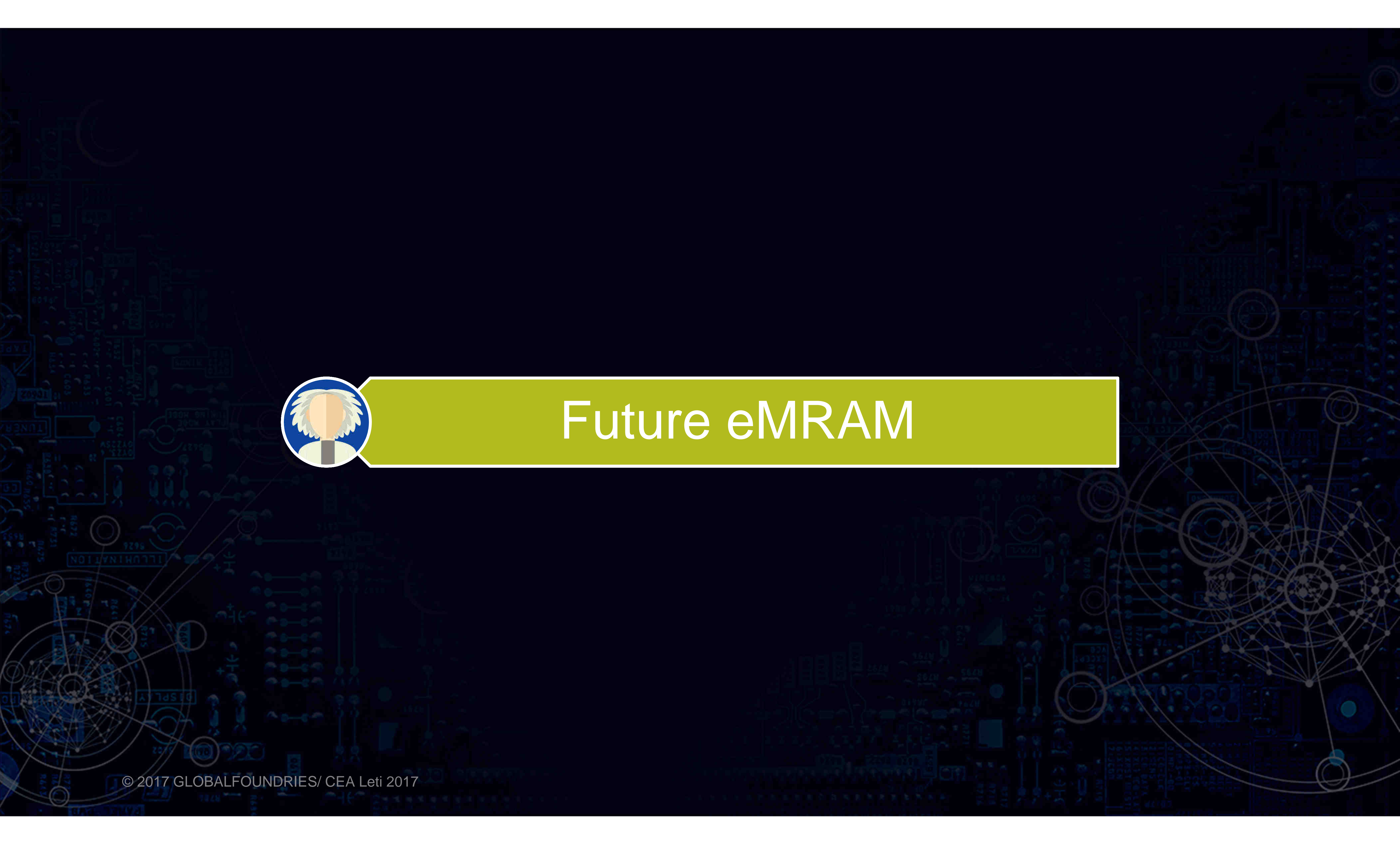
Future eMRAM
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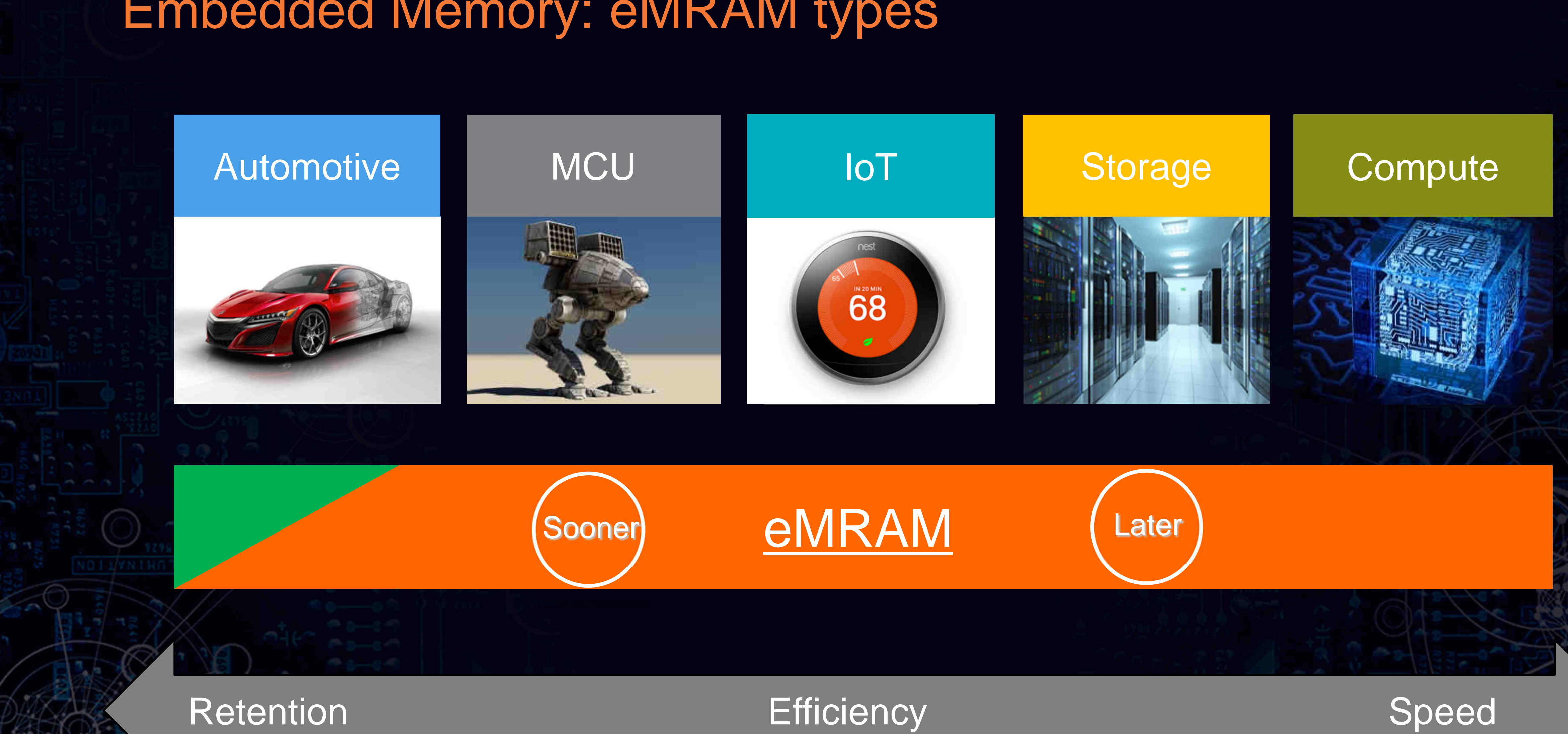

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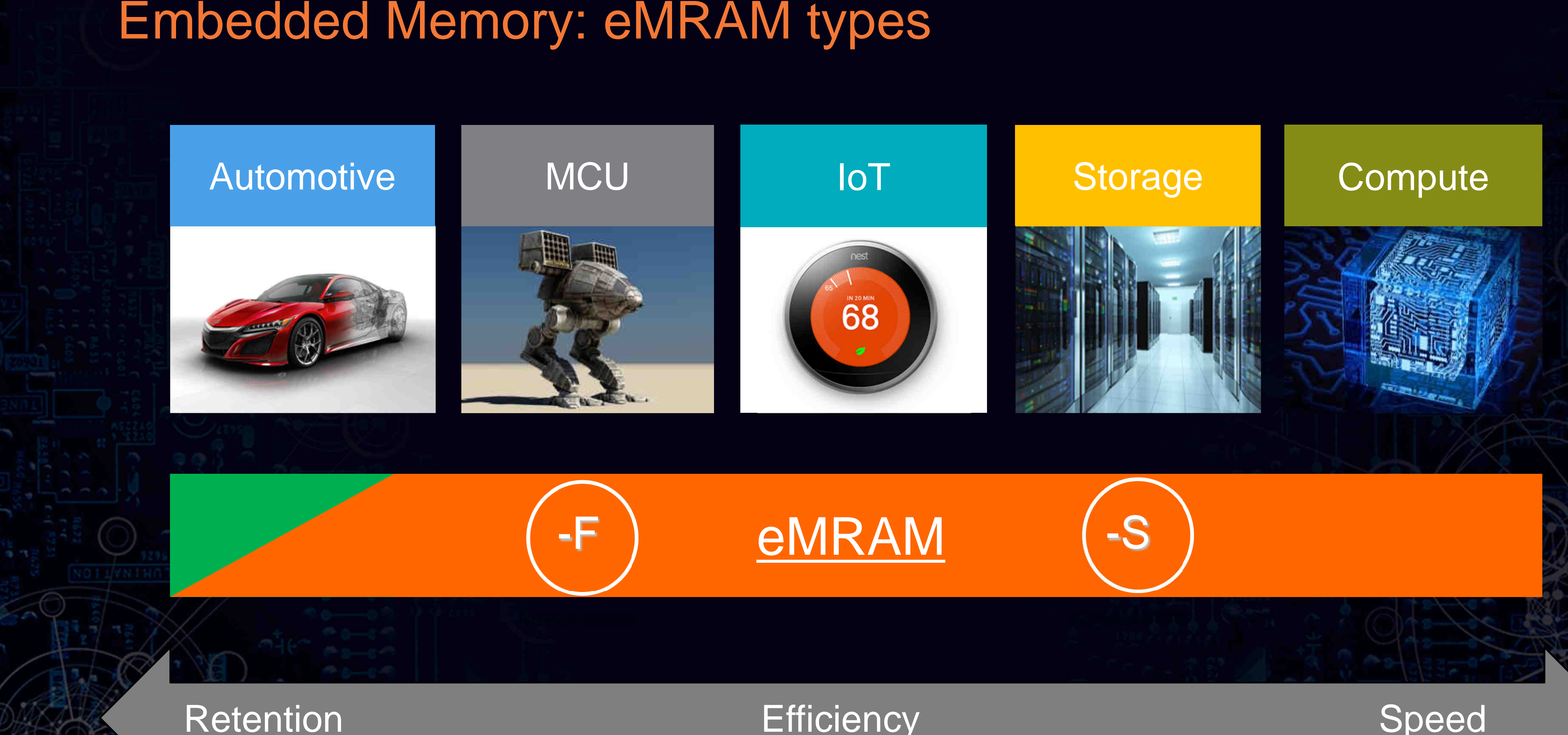

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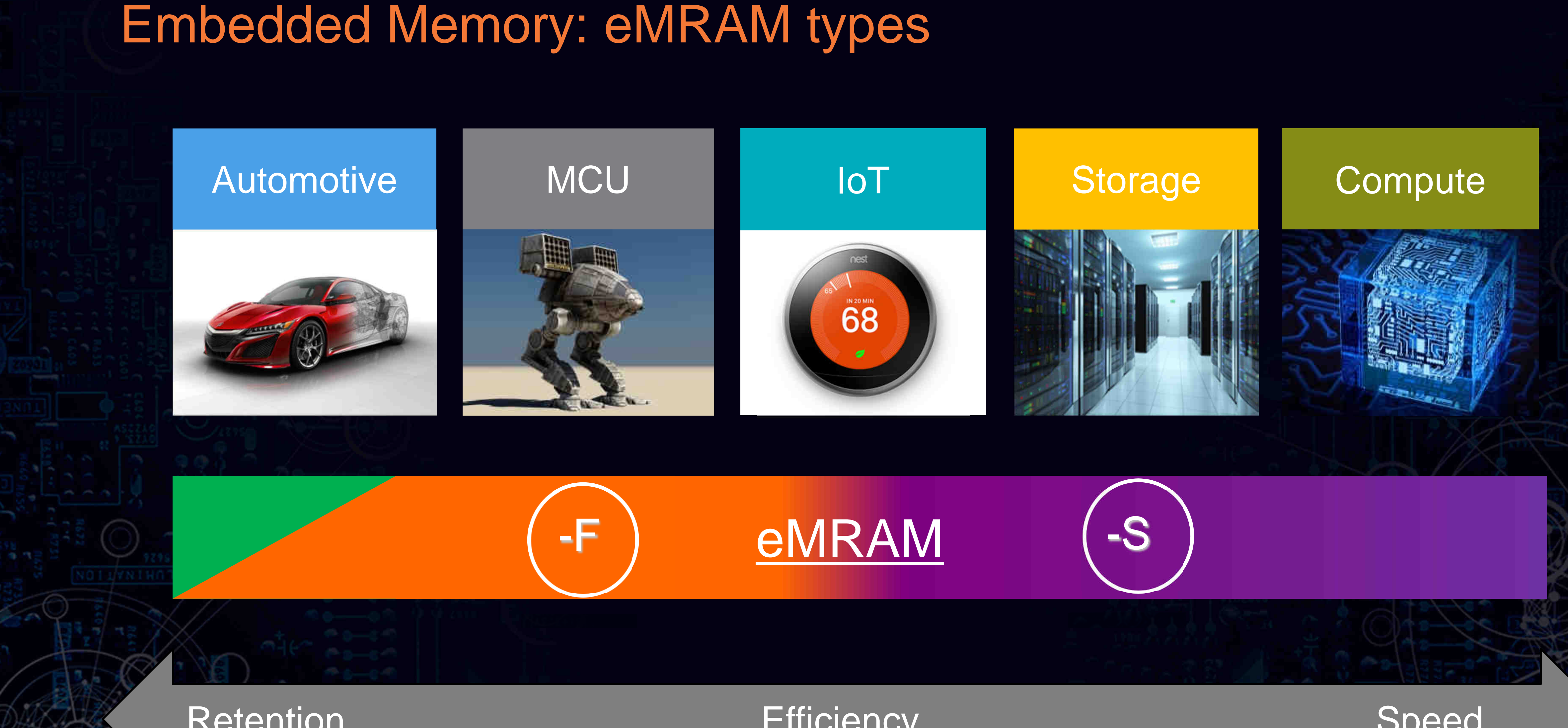

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	eFlash	eMRAM-F (macro#1)	eMRAM-F (macro#2)	eMRAM-S
Speed (Rd/Wr)	10ns / 20us	25ns /200ns	12.5ns /40ns	≈ 5ns / 10ns
Cell size	$40F^2$	$45F^2$	$70F^2$	$100\text{-}120F^2$
Endurance	10^5	$\approx 10^8$	$\approx 10^{10}$	$\approx 10^{14}$
Data Retention	>20 years	10 years	10 years	1 month
Solder reflow (260C/5min)	Yes	Yes	Yes	No
Op Temp (Tj)	155C Auto grade 1	125C Industrial/ Auto grade 2	125C Industrial/ Auto grade 2	105C Enterprise

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How much Endurance is enough for eMRAM-S?

Systematic Validation of 2x nm Diameter Perpendicular MTJ Arrays and MgO Barrier for Sub-10 nm Embedded STT-MRAM with Practically Unlimited Endurance

J.J. Kan[1,a], C. Park[1], C. Ching[2], J. Ahn[2], L. Xue[2], R. Wang[2], A. Kontos[2], S. Liang[2], M. Bangar[2], H.Chen[2], S. Hassan[2], S. Kim[1], M. Pakala[2,b], and S. H. Kang[1]

[1]Qualcomm Technologies, Inc., San Diego, California 92121, USA. E-mail: [a]jkan@qti.qualcomm.com
[2]Applied Materials, Inc., Sunnyvale, California 94085, USA. E-mail: [b]mahendra_pakala@amat.com

For typical cache use cases, an average time exists between successive writes to the same cache block. From reported workload simulations, very write-intensive applications (> 50% write vs. read) have a median write interval of ~ 10 ms (20 % of bits have $\Delta t \geq 40$ ms) [4]. This implies that a write endurance of 10^{11} cycles would be sufficient for 30 years of uniform write operations. Alternatively, one could assume a 32 MB STT-MRAM (64-bit I/O, 5 ns write cycle time) subjected to a constant write traffic of 1.6 GBps. With uniform writing, a lifetime of 63 years would be expected for an endurance of only 10^{11} cycles, substantially less than the 10^{15} predicted for our worst 1ppm.

Source: IEDM 2016; J.J. Kan, et al; Qualcomm

“Write endurance of 10^{11} cycles would be sufficient for 30 years of uniform write operations”

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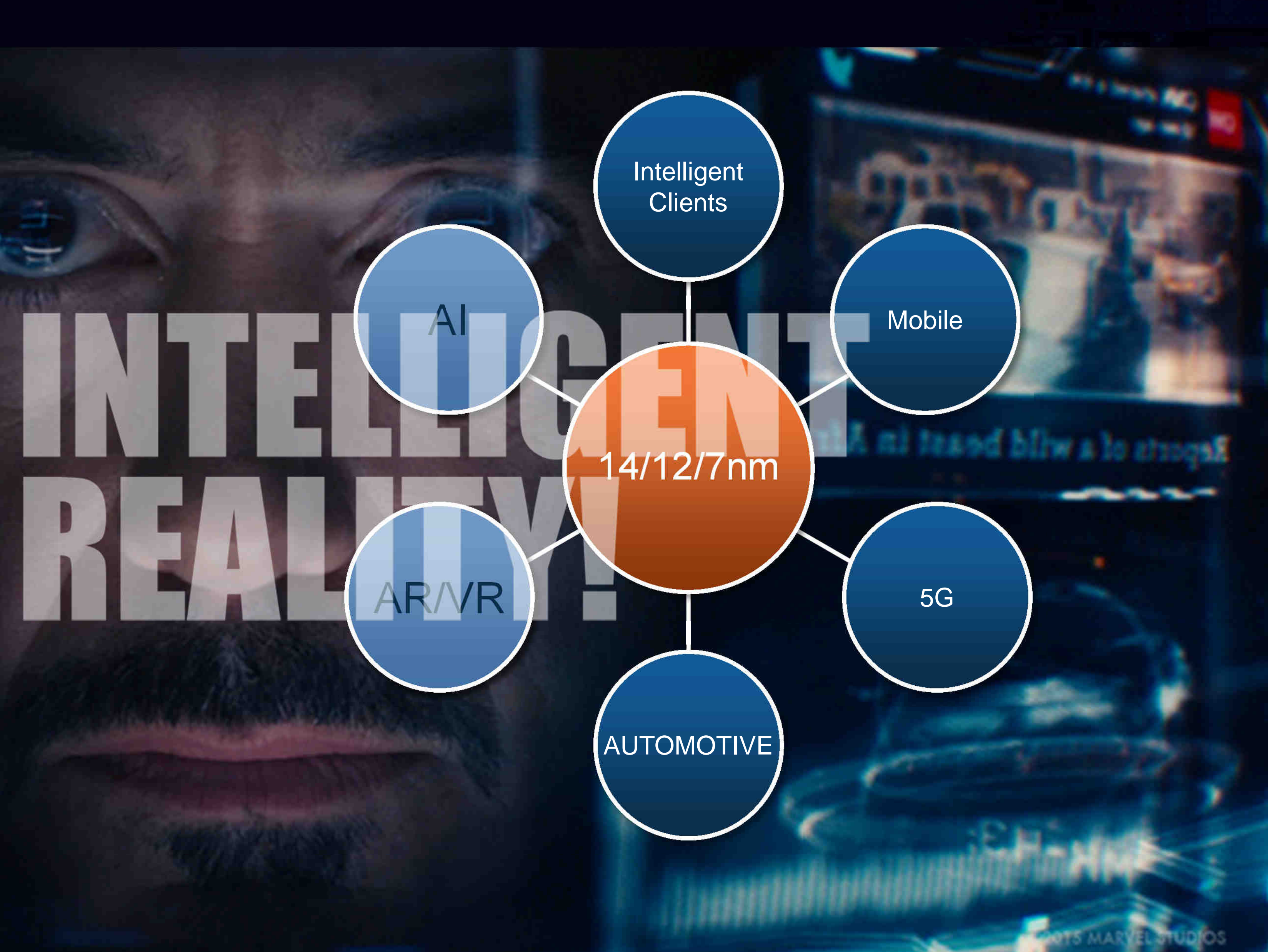
Future eMRAM

Gb densities of NV memory
- Enables real-time analysis of big data

Powers intelligent clients
- AR/VR, AI, Autonomous Vehicles

NV-logic transformation
- Integrate non-volatility directly into logic elements



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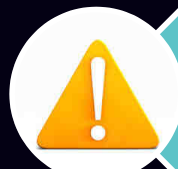
Markets & Requirements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GLOBALFOUNDRIES Roadmap & eMRAM

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Building Global Scale for FDX™

Dresden, Germany Fab 1

- Expanding 22FDX® FD-SOI capacity by 40% by 2020
- Developing 12FDX™ FD-SOI technology with tape-outs 2H 2018

Chengdu, China Fab 11

- New 300mm fab in partnership with Chengdu Municipal Government
- Existing 180 / 130nm technologies, production starting 2H 2018, then 22nm in 2H19

- Multi-fab sourcing for assurance of supply
- Multiple substrate vendors for robust supply chain
- Local commitment to China industry growth

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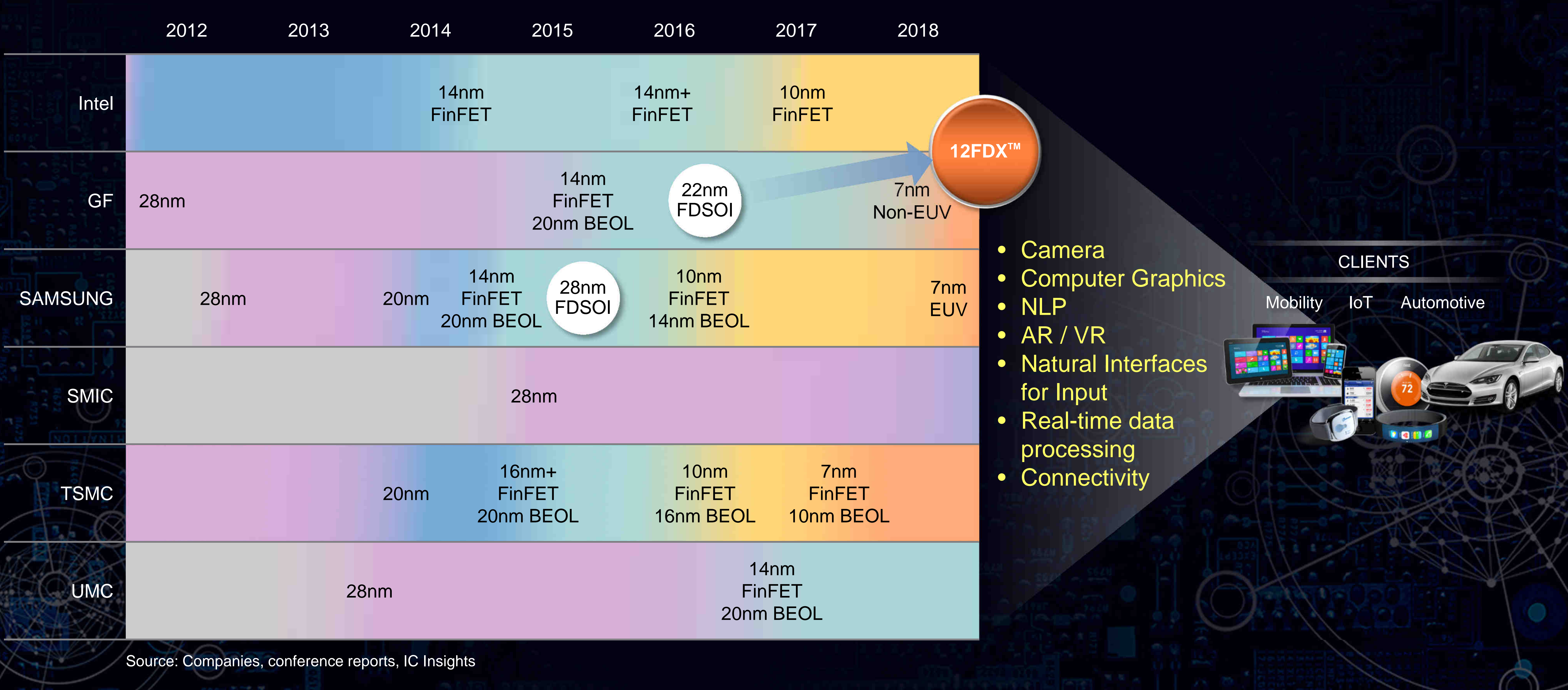
FD-SOI Will Become Standard for the Volume Tier



Source: Companies, conference reports, IC Insights

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GLOBALFOUNDRIES CMOS Roadmap

Markets: Servers, high performance computing and graphics, high-end smartphone, core networking

Premium Tier

Features: High-performance, balanced-cost

High Performance Computing

7nm FinFET

14nm FinFET

eMRAM-S

28nm

Wireless, Battery-Powered Computing

12FDX™

22FDX®

40/55nm

eMRAM-F

Markets: Low & mid-end smartphones, wireless, IoT, autonomous vehicles, mobile camera

Volume Tier

Features: Low-power, cost-effective-performance, RF, embedded memory

the Right Technology for the Right Application™

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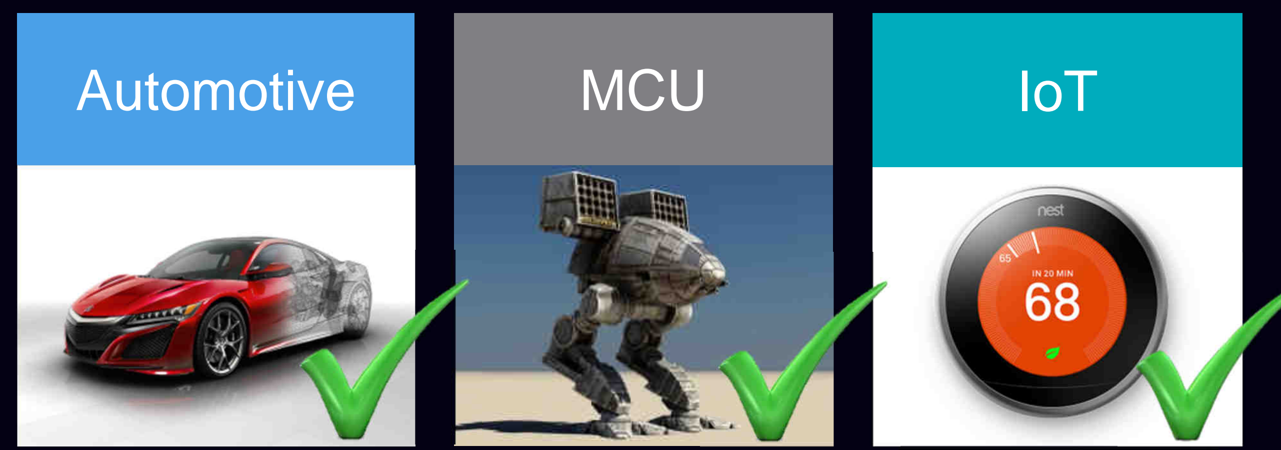
GF eMRAM: High Reliability, Broad Markets



GLOBALFOUNDRIES and Everspin continue to drive embedded MRAM (eMRAM) forward into the 22nm process node!

For the first time, we are unveiling eMRAM that can retain data through solder reflow at 260C and 10+ years at 125C, plus read/write with outstanding endurance at 125C.

This is a major breakthrough from GLOBALFOUNDRIES and Everspin that enables eMRAM to be used for general purpose MCU's and Automotive SOCs.

Please contact me if you want more information! dave.eggleston@globalfoundries.com

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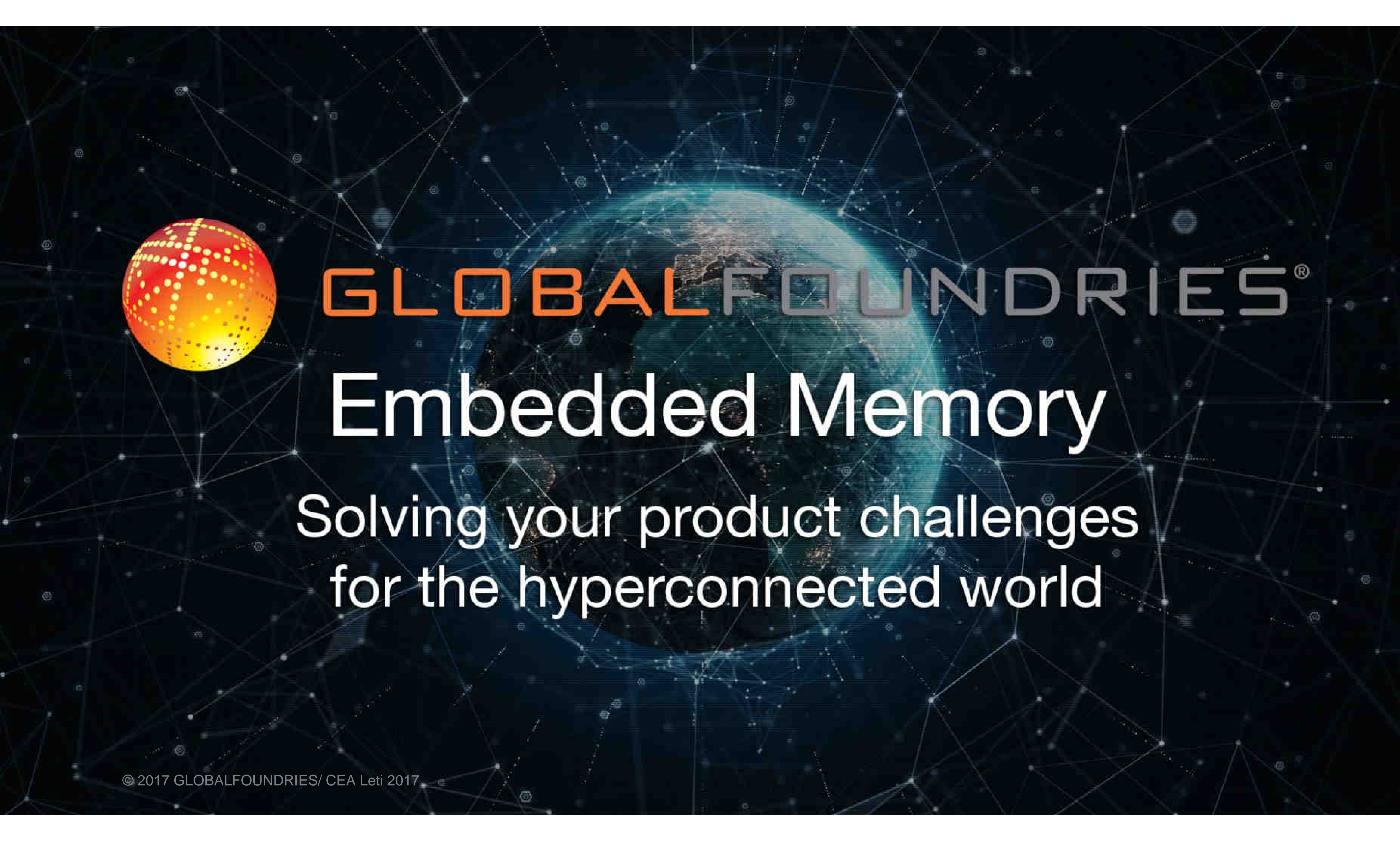
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