3D sequential integration: technology and application status

Perrine Batude, Claire Fenouillet-Beranger, Laurent Brunet, Vincent Mazzocchi, Cao-Minh Vincent Lu, Fabien Deprat, Jessy Micout, Bernard Previtali, Paul Besombes, Nils Rambal, François Andrieu, Olivier Billoint, Mélanie Brocard, Sébastien Thuries, Guillaume Berhault, Alexandre Ayres, Fabienne Ponthenier, Cristiano Lopes Dos Santos, Gérald Cibrario, Fabien Clermidy, Daniel Gitlin, Olivier Faynot and Maud Vinet

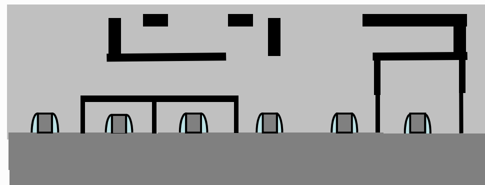
Outline

3D sequential characteristics

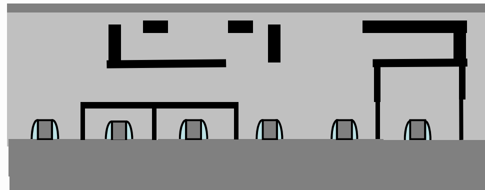
3D sequential opportunities

Process integration

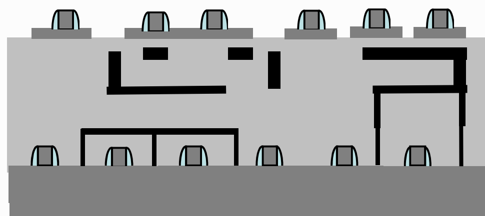
3D sequential integration



Bottom MOSFET process
with or wo interconnects



Top active creation:
Future MOSFET channel



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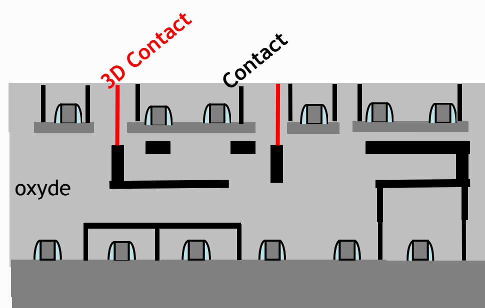
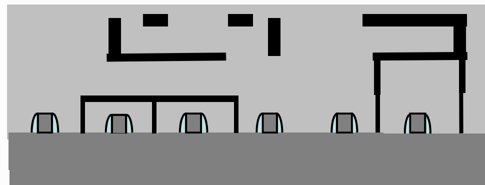


3D contact formation

Also named
... 3D monolithic
... 3D VLSI

3D sequential integration



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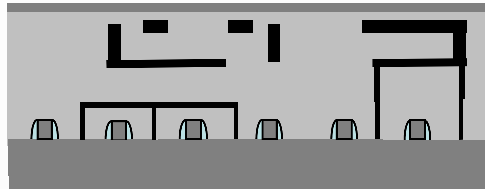

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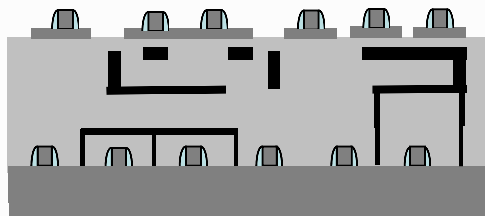
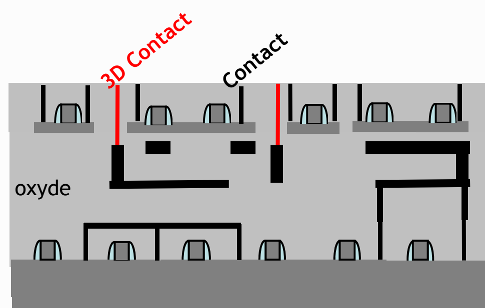


Top MOSFET process

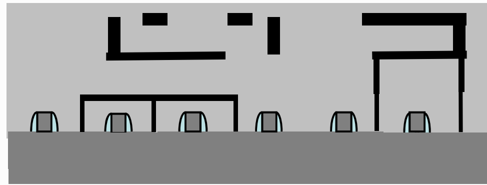
THERMAL BUDGET CONSTRAINTS



3D contact formation

... CoolCube™

3D sequential integration



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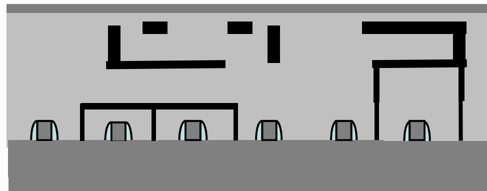
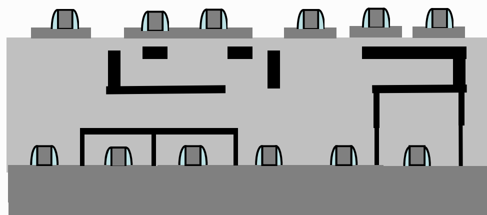
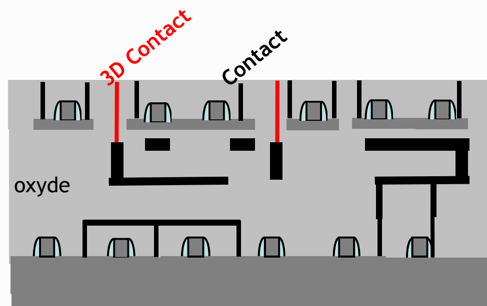


Top active creation
thin (10-100nm)



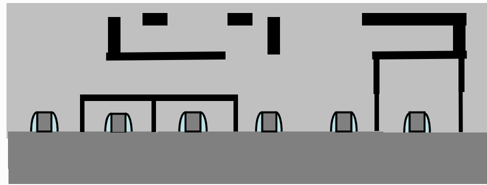
Top level pattern by litho
Top MOSFET process

Alignment TOP/ BOT
e.g: 28nm node: 3σ<5nm



3D contact formation:
Standard W plug in oxide

3D sequential integration



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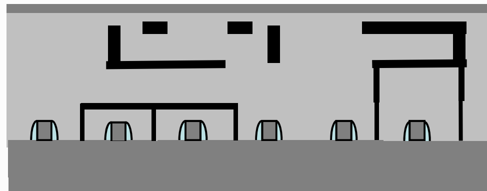

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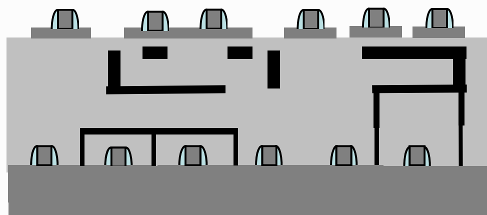

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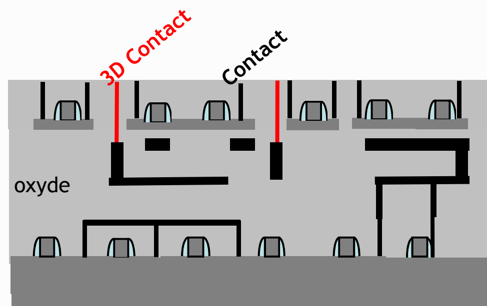
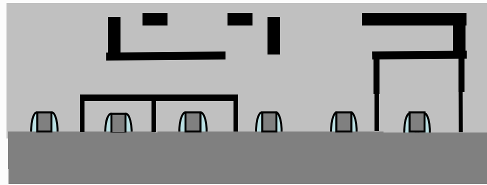


3D contact formation:
Standard W plug in oxide

3D Contact scales with
the device technology
e.g: 28nm node: ~40nm

3D sequential integration



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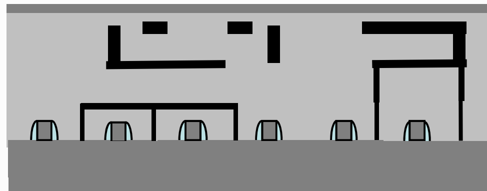
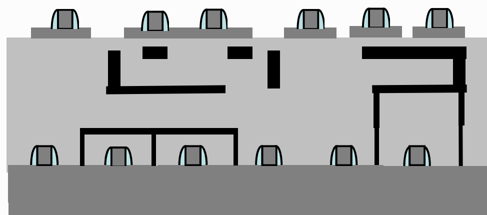


Top active creation
thin (10-100nm)

Small 3D via AR
Small Parasitic C



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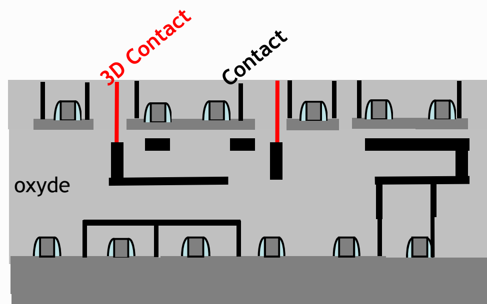
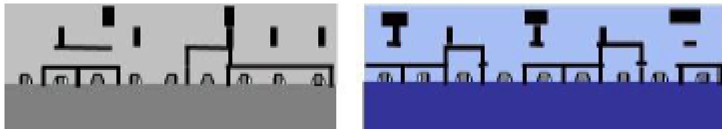


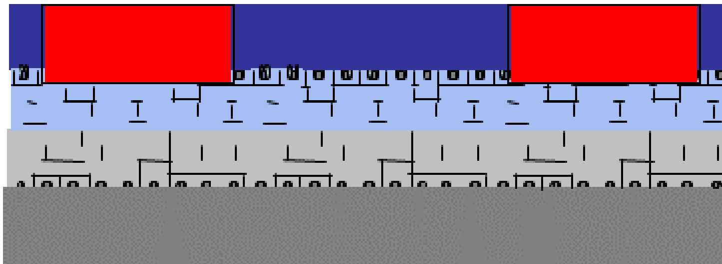
3D contact formation:
Standard W plug in oxide

Sequential ≠ Packaging integration

Packaging integration

(e.g.: TSV, copper to copper bonding..)

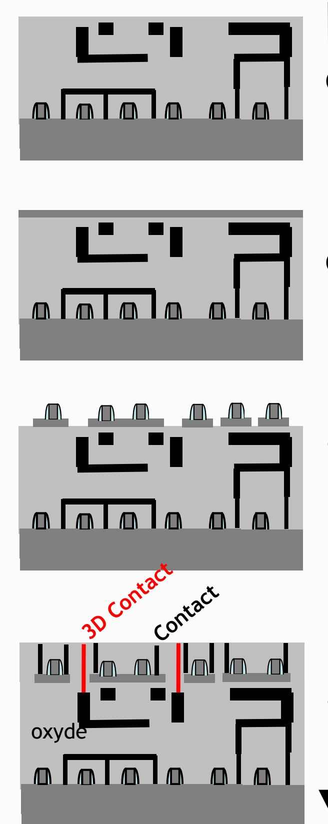




Alignment made during bonding

3σ min = 250nm

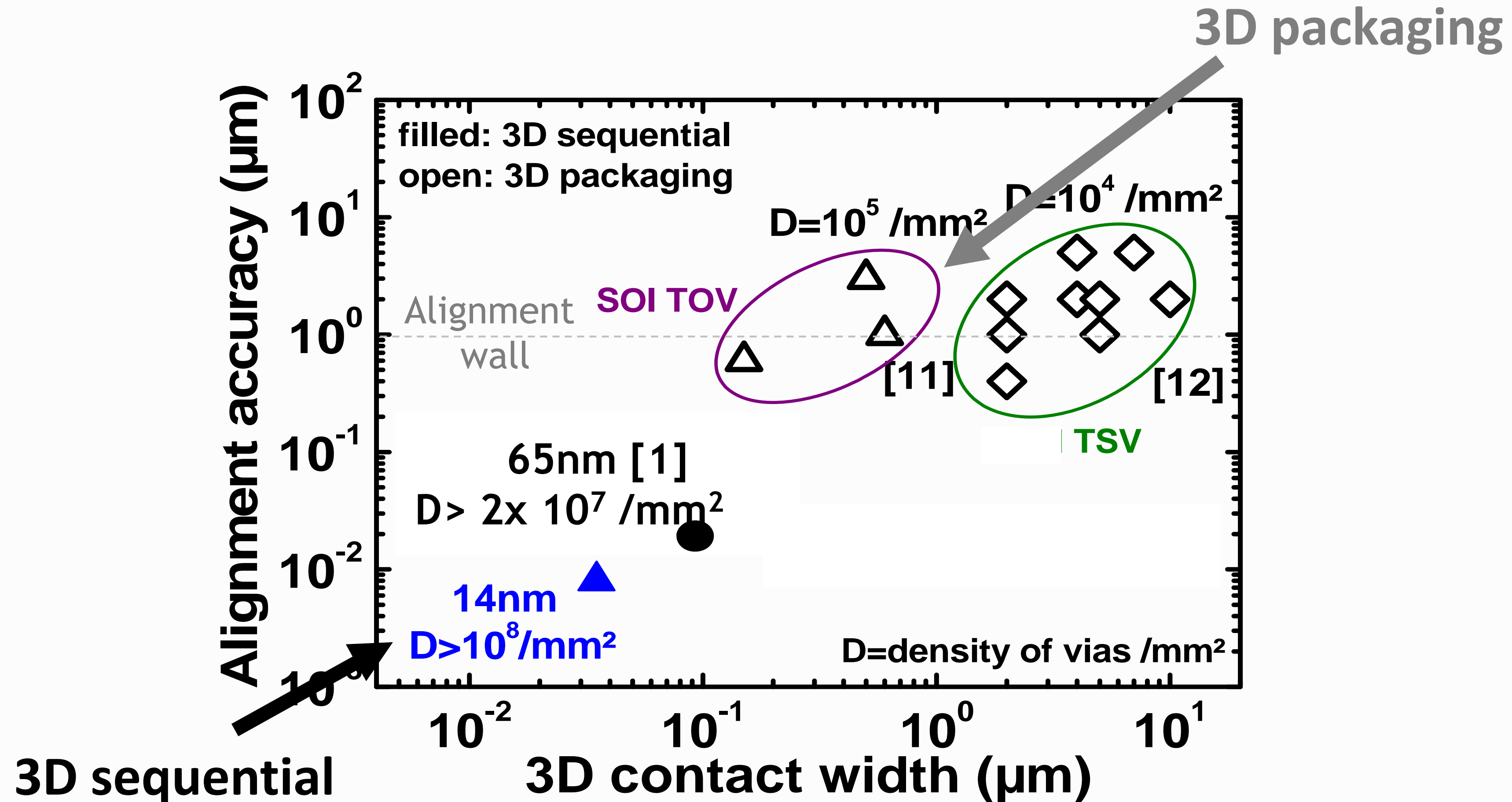
Sequential integration



Alignment by lithography

3σ = 5nm (28nm stepper)

3D contact density

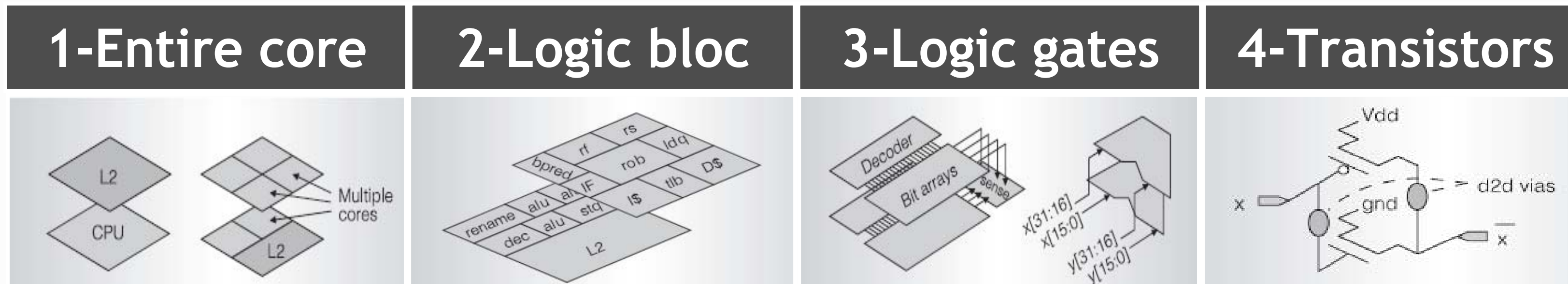


2×10^7 via/mm² demonstrated [1]

Reachable 3D via pitch @ 14 nm node =80nm

[1]: L. Brunet et al., VLSI 2016, [11] P.Garrou et al.,Handbook o f 3D integration, vol.12 (Wiley ed.), [12] B. Banijamali et al., ECTC 2011,

3D partitionning levels



Outline

3D sequential characteristics

3D sequential opportunities

Process integration

Outline

3D sequential characteristics

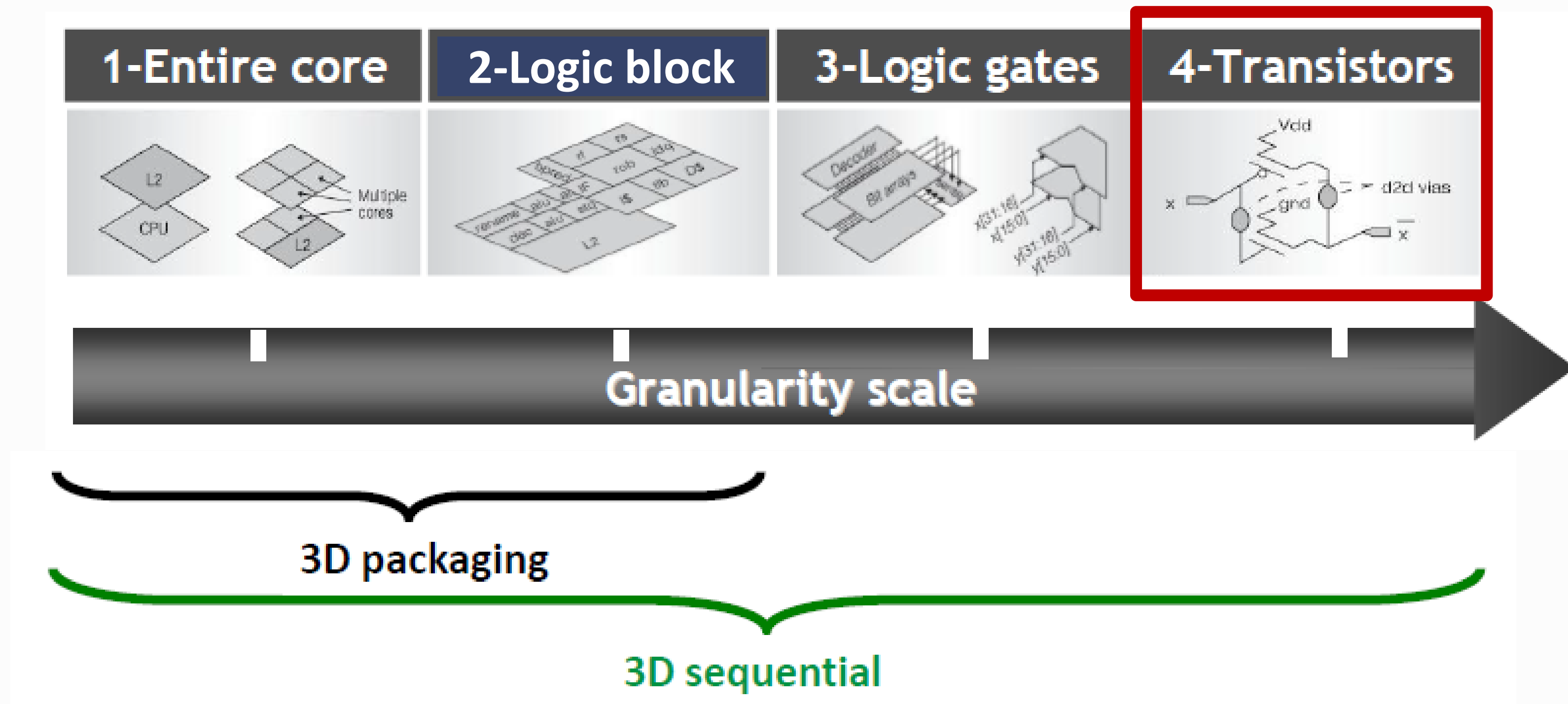
3D sequential opportunities

A Digital Computing (More Moore)

B Sensor interface (More than Moore)

Process integration

Using sequential 3D at the smallest granularity

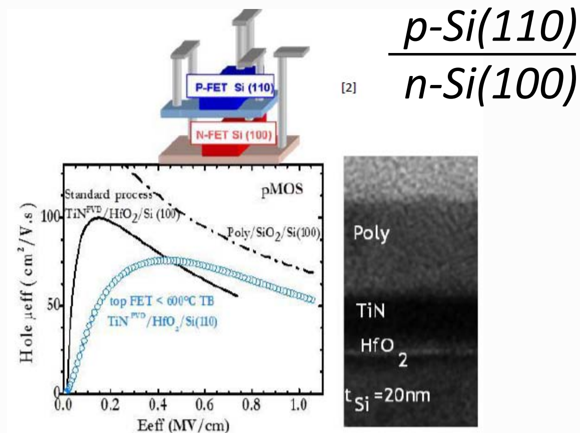


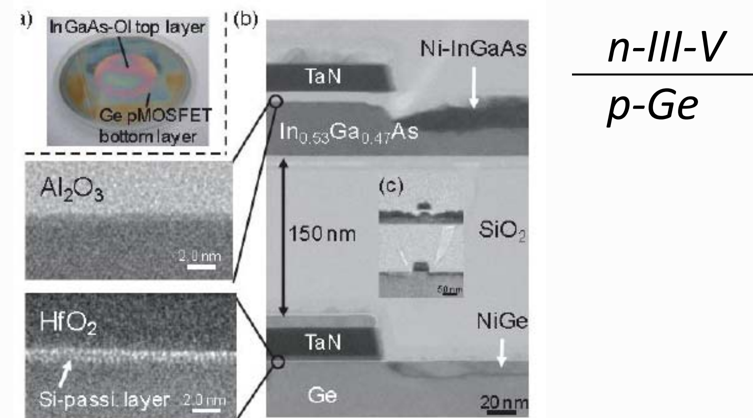
3D sequential offers the N & PFET stacking opportunity

N/P stack: the integration engineer's graal

If for each FET polarity, one were to pick the best possible:

- Channel material
- Gate stack
- Stressors
- Contact metallurgy
- Surface orientation
- Device Architecture



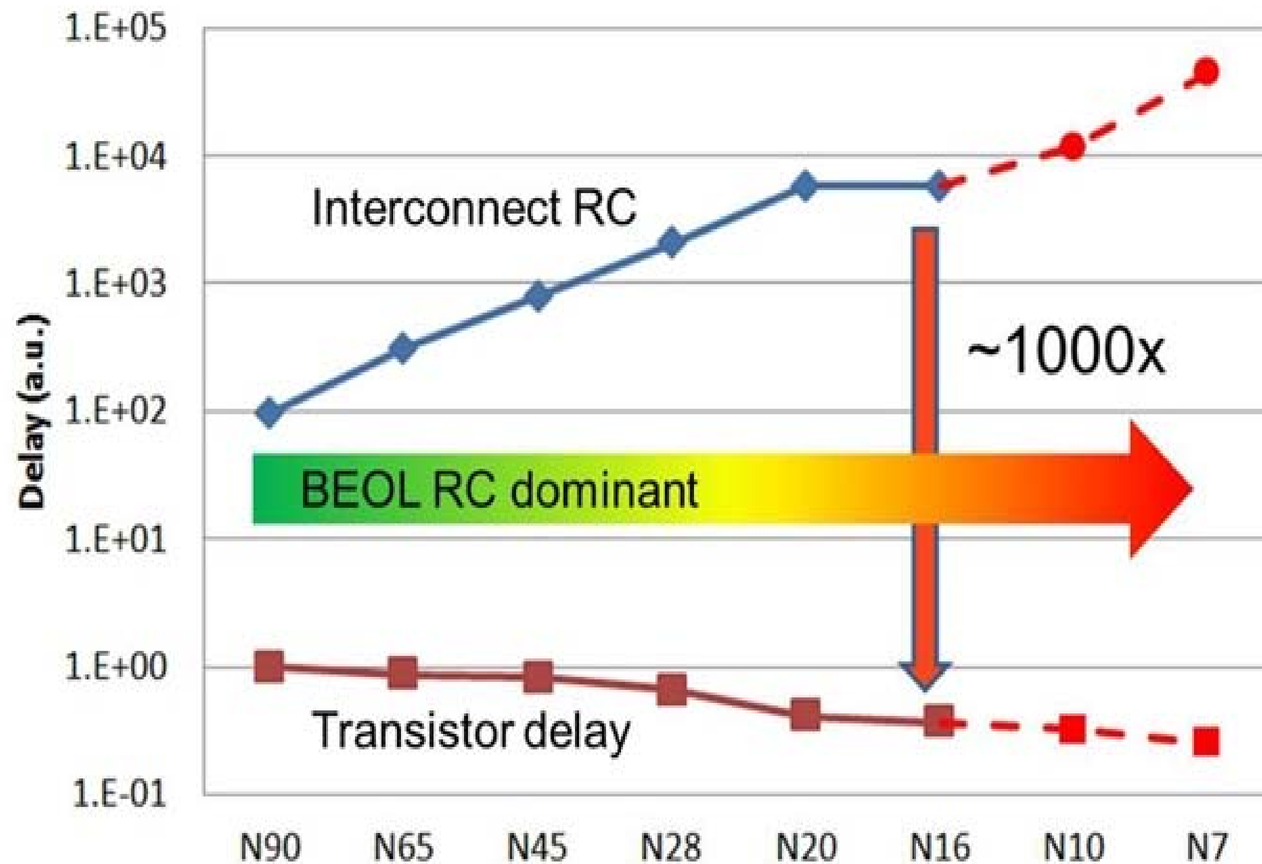


…then 3D sequential spares numerous litho steps and process selectivity challenges vs. co-planar

‡ P. Batude *et al.*, IEDM 2009 (Leti)

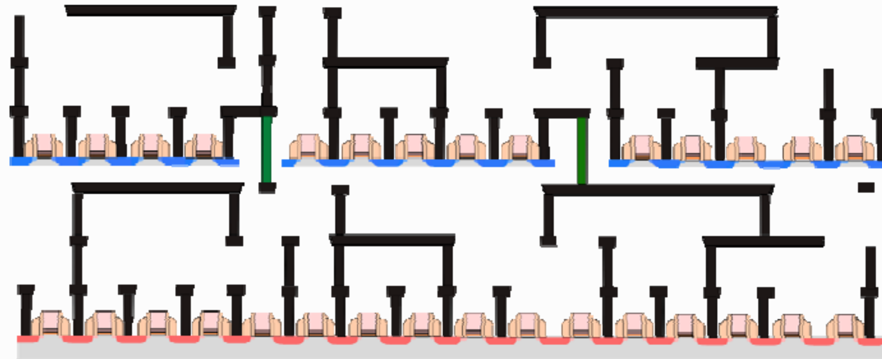
** T. Irisawa *et al.*, VLSI 2013 (AIST)

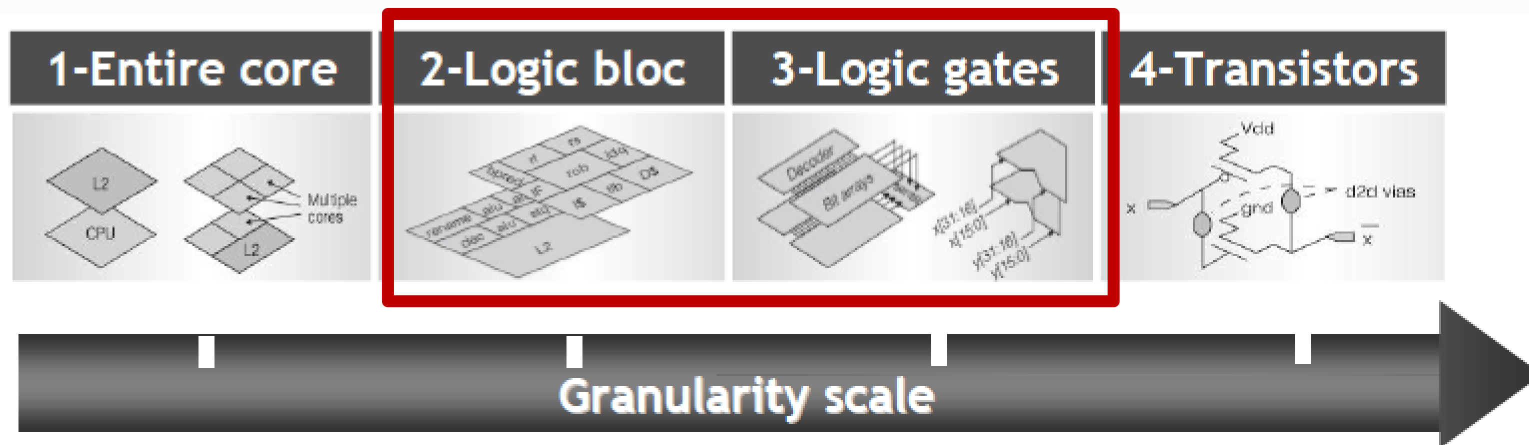
Interconnect delay supression: the designers' graal



Extracted from Geoffrey Yeap, Qualcomm's VP of technology IEDM 2013

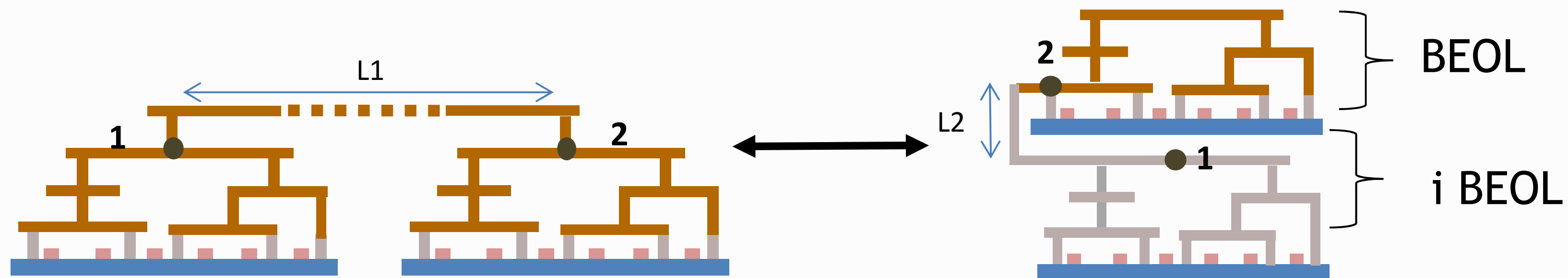
Gain in interconnection delay →CMOS/ CMOS stacking





IC gain performance by wirelength reduction
No modification of the MOS technology

Gain in interconnection delay → CMOS/ CMOS stacking



- Depends on the technology node
- Depends on the application
- Hard to tell without dedicated P&R tools [1,2]

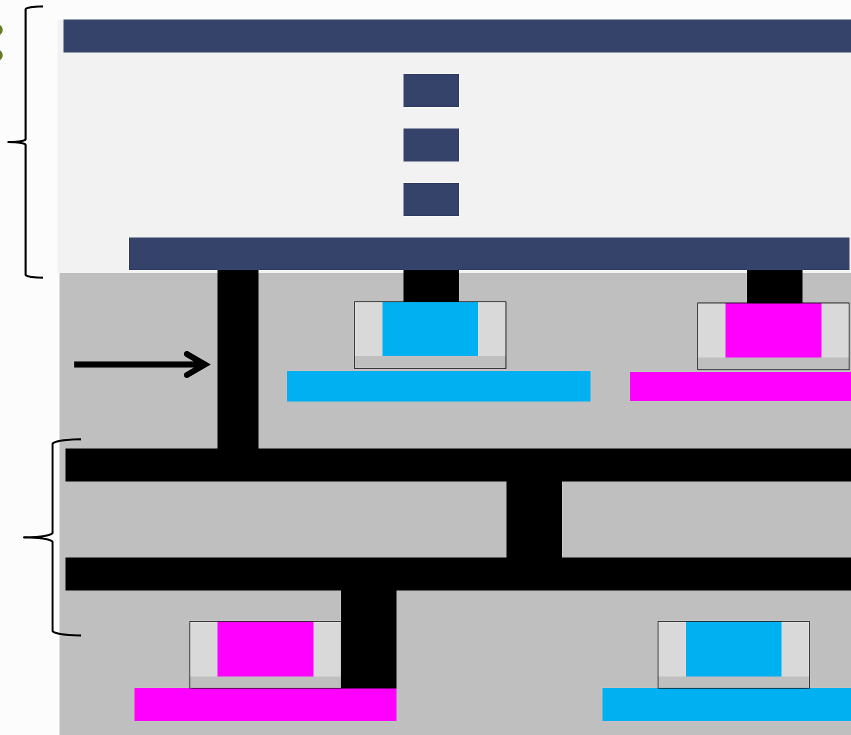
[1] K. Arabi et al., ISPD 2015 [2] O. Billoint et al., ISPD 2015

Full custom design: FPGA application

$\frac{\text{14 nm FDSOI}}{\text{14 nm FDSOI}}$ versus 14nm planar FDSOI

CoolCube DKIT:

- Top BEOL (Cu & low-k) M1 to Mx
- 3D Contact (Pitch 80nm)
- Int. BEOL (W & SiO_2) M1i to M3i



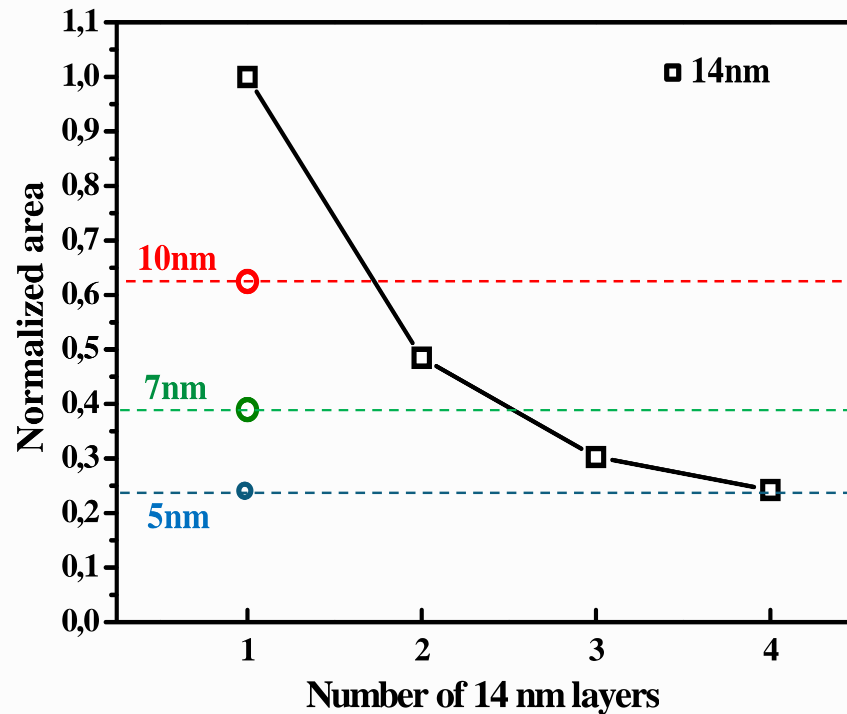
Partitioning:

- Top level: Logic
- Bottom level: SRAM memory

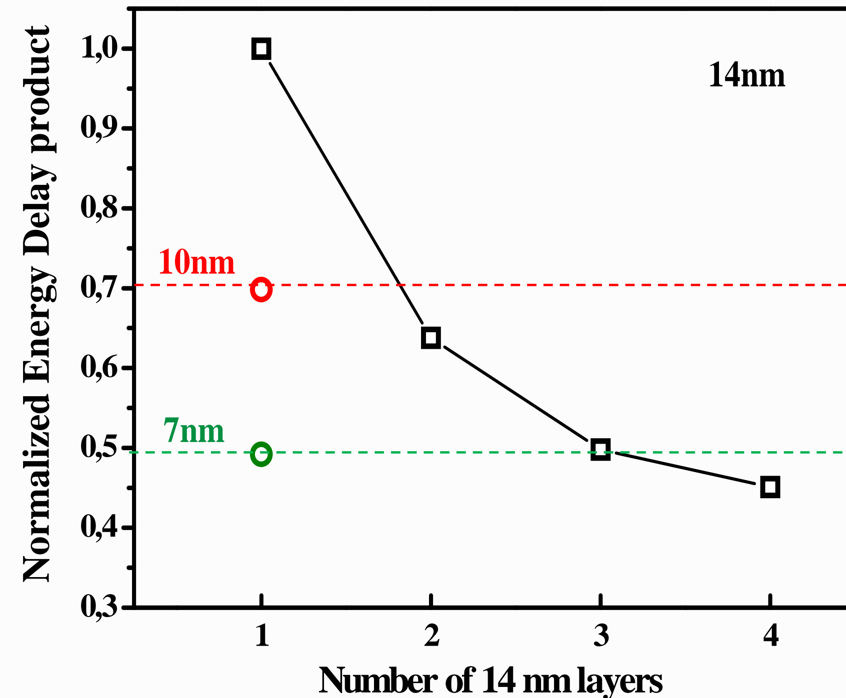
Full custom design: FPGA application

Analysis using VPR5 flow

Area



Energy Delay Product

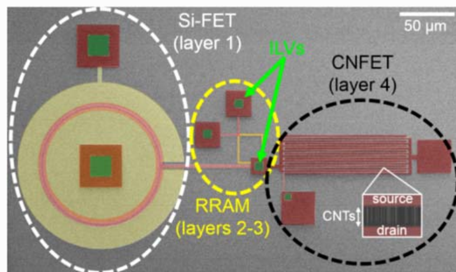


$\frac{\text{14 nm}}{\text{14 nm}}$ **better than 10 nm**

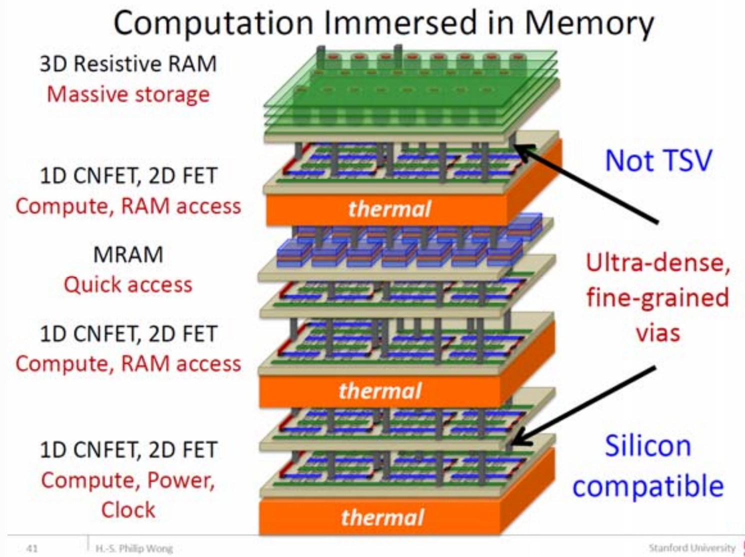
[1]: O. Turkyilmaz et al., DATE 2014 [2]: ITRS 2013, “System driver summary
[3]: ITRS 2013, “ORTC”

The new graal: Circuit power efficiency

How: Distributed memory in between the stacked layers



Stacking 4 layers with RRAM in between MOSFETS [1]



N3XT Computing system [2]

X 1000 gain in consumption expected with computing in memory - Need fine grain partitionning (Seq)

[1] Shulaker et al., IEDM 2014 , [2] Aly et al., Rebooting computing, 2015

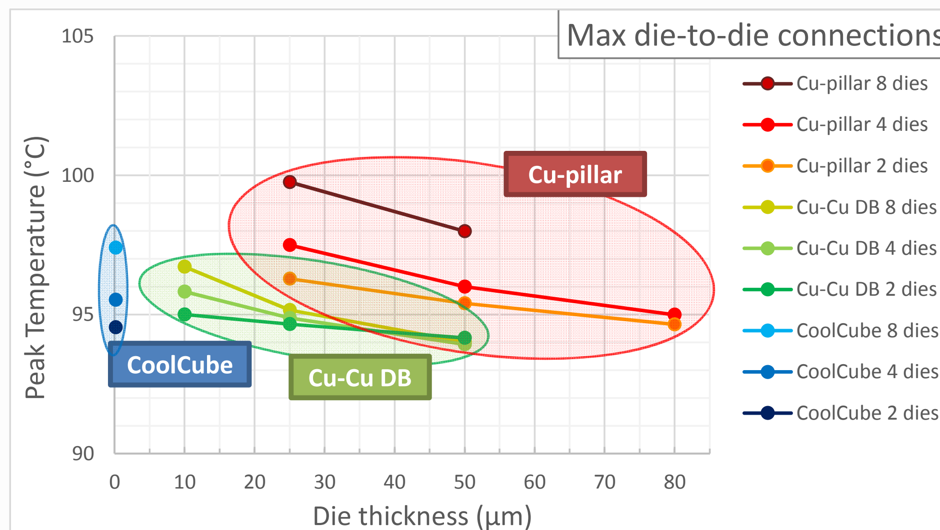
Thermal considerations: 3D seq vs 3D pack

The substrate thickness is very small in 3D sequential

→ smaller lateral heat conduction→ Hot spot

Small interdie thickness (60nm)

→ Die to die thermal coupling (vertical coupling) and temperature smoothing via the substrate



3D sequential thermal behaviour equivalent to TSV based integration process

[1] C. Dos Santos, 3DIC 2017

Outline

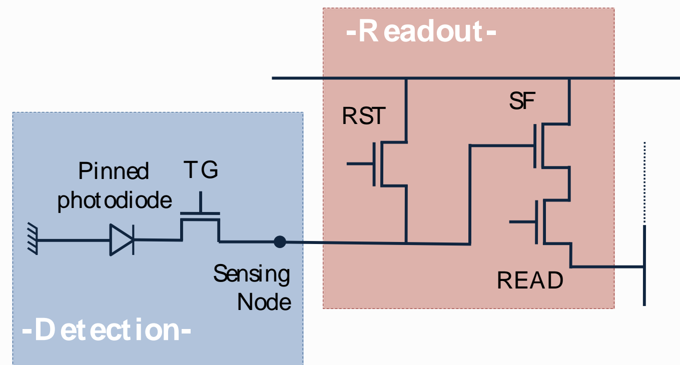
3D VLSI CoolCube characteristics

3D VLSI CoolCube opportunities

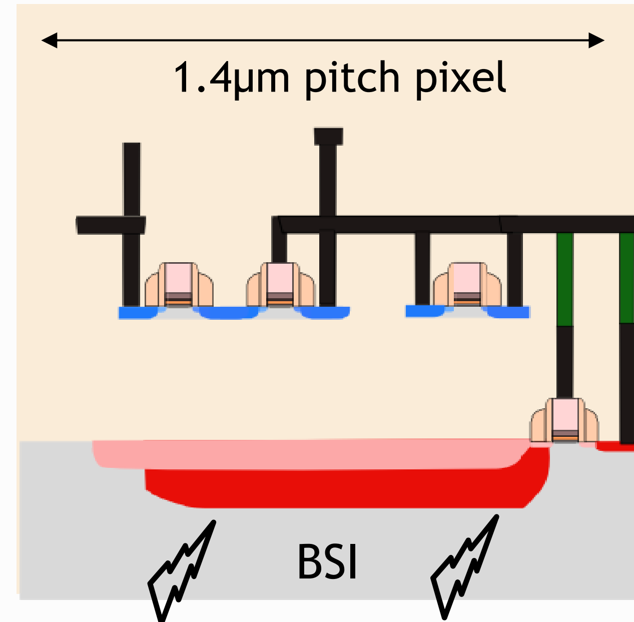
- A Digital Computing (More Moore)
- B Sensor interface (More than Moore)

Process integration

Enabling the pixel 3D partitionning



[1]



Multiple benefits

- BSI integration → high quantum efficiency
- Photodiode area +44% for 1.4µm pitch pixel

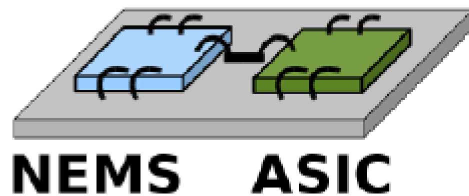
Sequential 3D can address these dimensions

NEMS/CMOS CO-integration enabler

Challenge: detecting NEMS resonance

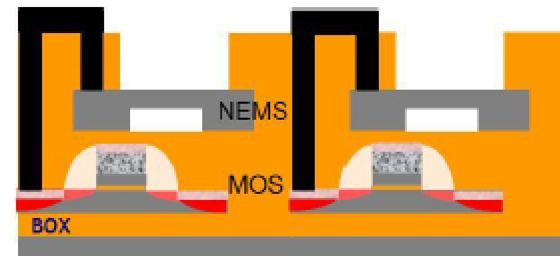
Stand alone NEMS + off-chip CMOS

No density (pads number limitation)
Very strong signal attenuation (LP filter)



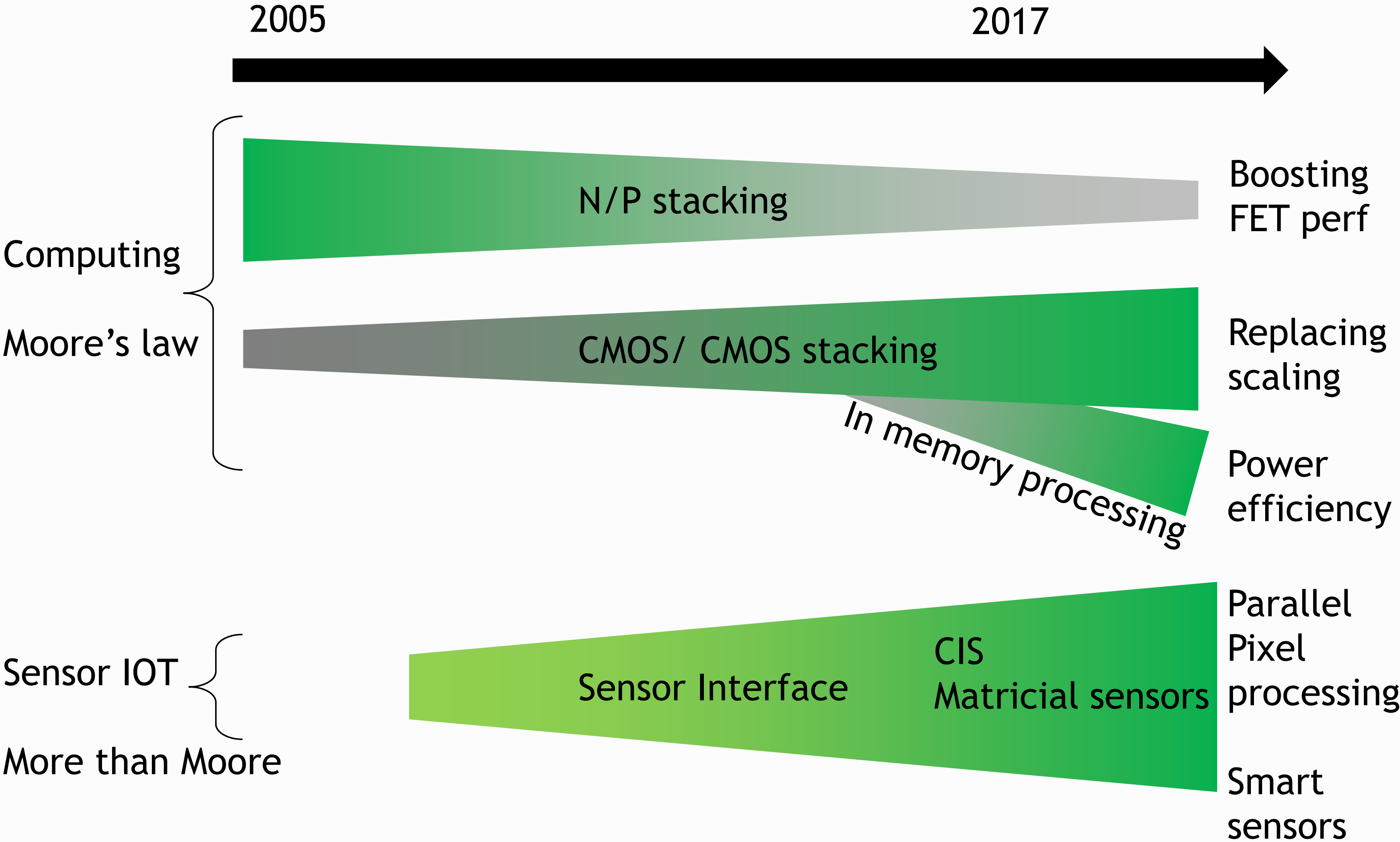
3D sequential NEMS + CMOS

No density limitation
no signal attenuation



Sequential 3D can solve detection limitation
Very small parasitics

Summary: Sequential 3D application trends



Outline

3D VLSI characteristics

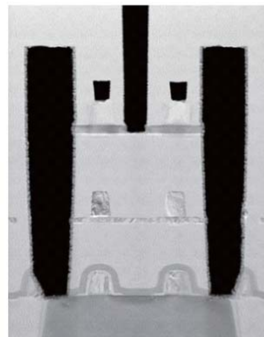
3D VLSI opportunities

Process integration

3D seq demonstrations & main actors

"Conventional MOSFETs *et al.*," (Si, Ge and III-V) i.e. target 100% perf team

[1] SRAM cell.
Seed window.
(SAMSUNG 2007).

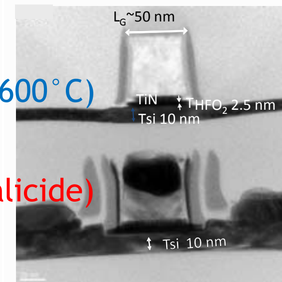


HT Si

HT Si

HT (no salicide)

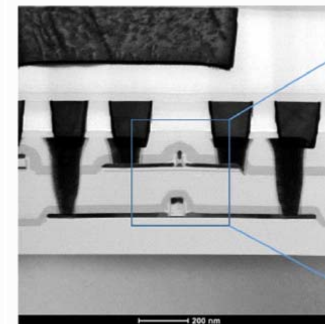
[2] SRAM cell.
Molecularbonding
(CEA/LETI 2010).



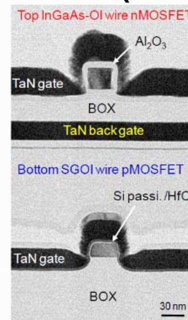
LT Si (600°C)

HT (salicide)

[3] 300mm. Inverters
Molecularbonding
(CEA/LETI 2016).



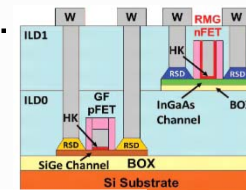
[6] CMOS inverters
InGaAs/SGOI (AIST 2014).

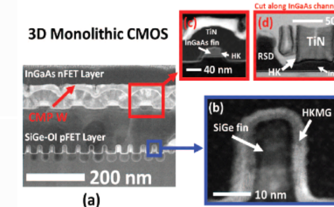


LT III V

Ge

[7] III-V on Ge.
(IBM 2015).





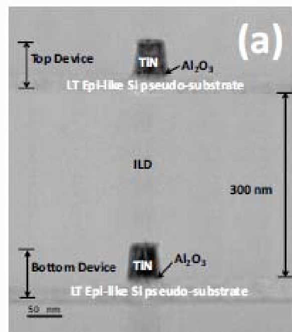
LT III V

Ge

3D seq demonstrations & main actors

"Innovative MOSFETs *et al.*," (TFT & CNT)
i.e. Low cost & low thermal budget team

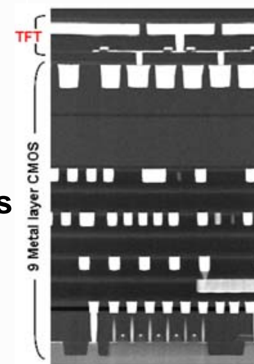
[5] SRAM cell. Laser crystallizedepi-like Si. (NDL 2015).



LT Si TFT (400°C)

HT (salicide)

with TFT SRAM over 90nm 9 layer Cu CMOS. Amorphous Si. (Toshiba 2010).



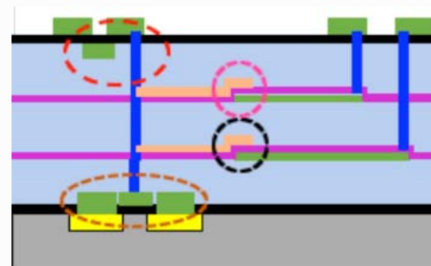
[9]

LT Si TFT (400°C)

i BEOL

HT (salicide)

Logic and Memory: CNT FETs, RRAM, Si -FETs (Stanford 2014).



LT CNT FET (180°C)

RRAM

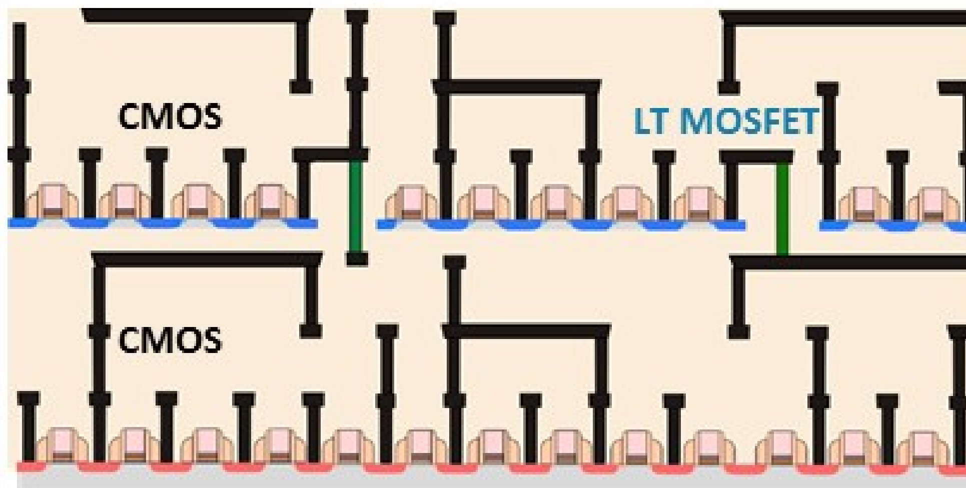
RRAM

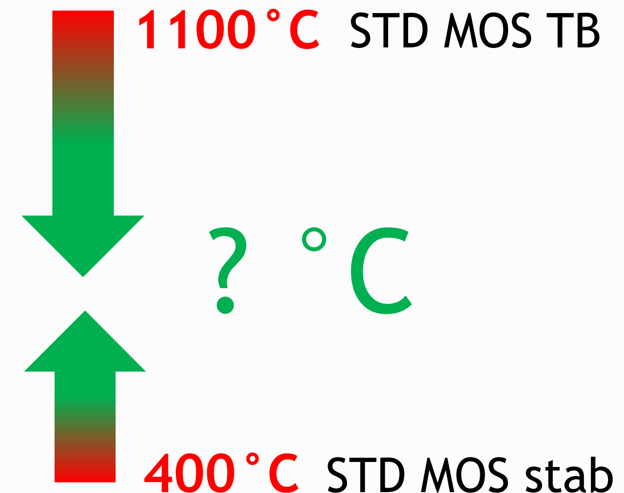
HT si

CoolCube™ process flow

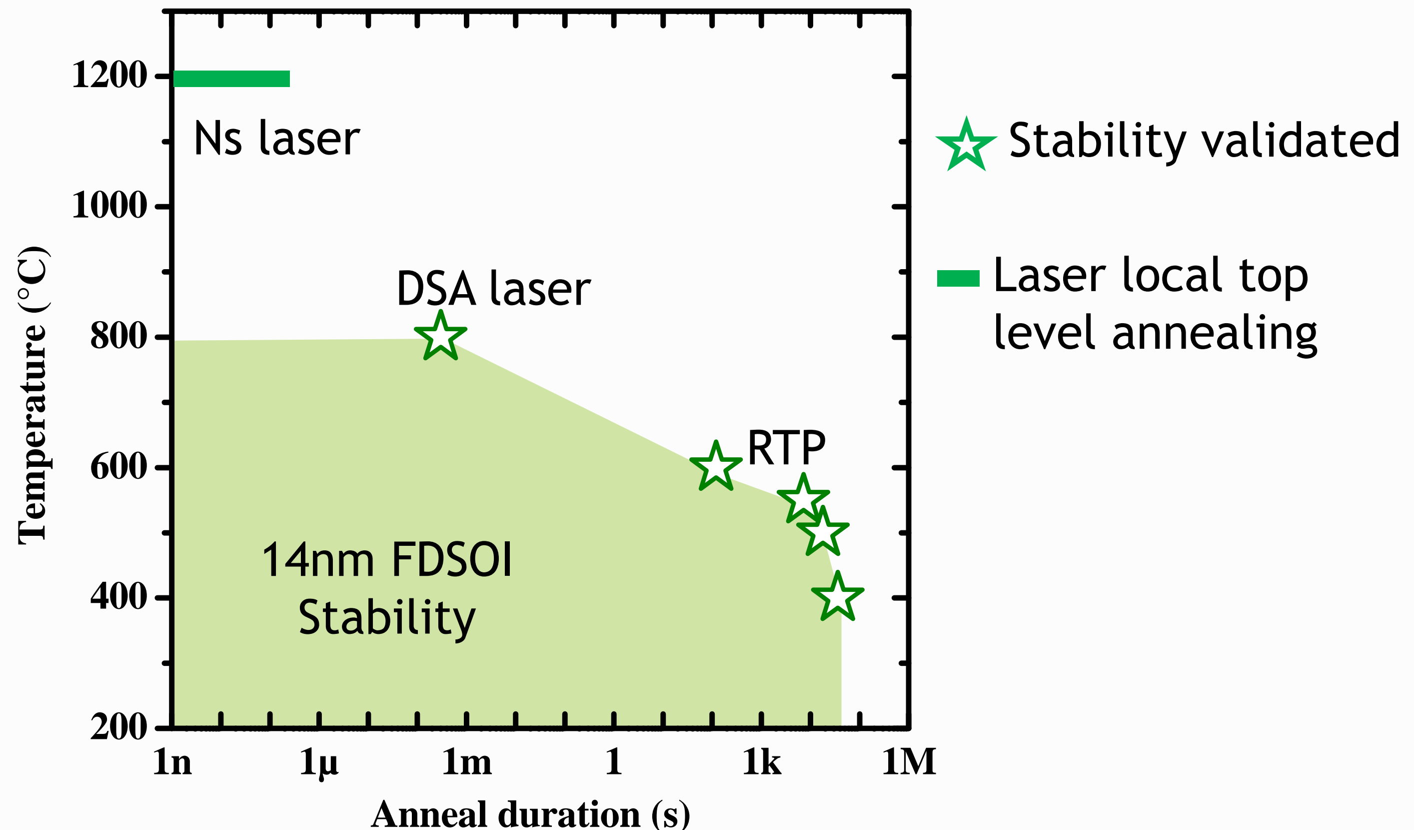
A - Bottom tier:
what maximum thermal budget to keep perf at 100%?

B- Top tier:
How achieving LT Top FET with 100% perf?





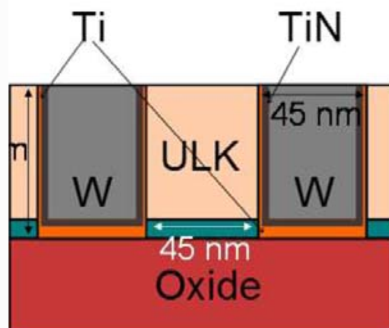
Bottom MOSFET stability



Bottom MOSFET thermal budget process window
Will be summarized as «500°C 5h»

[1]: P. Batude et al., VLSI 2015

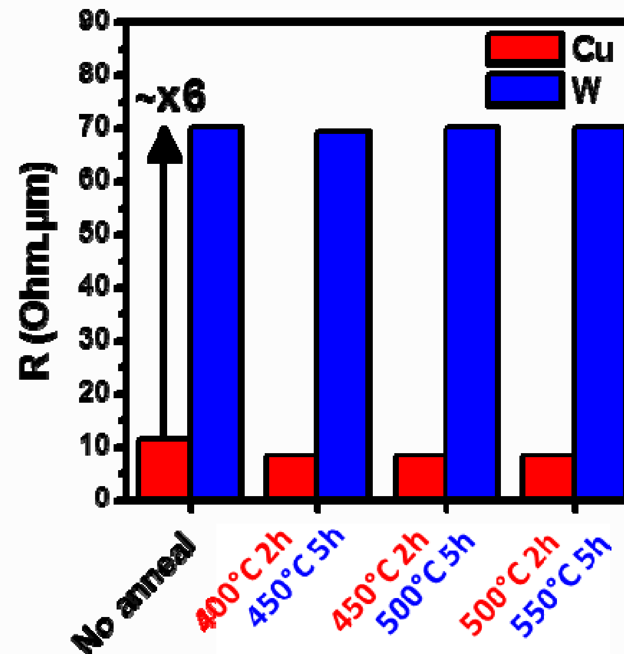
Interconnections stability



R & C stability [1]

Up to 500°C 2h for Cu/ULK

Up to 550°C 5h for W/ULK



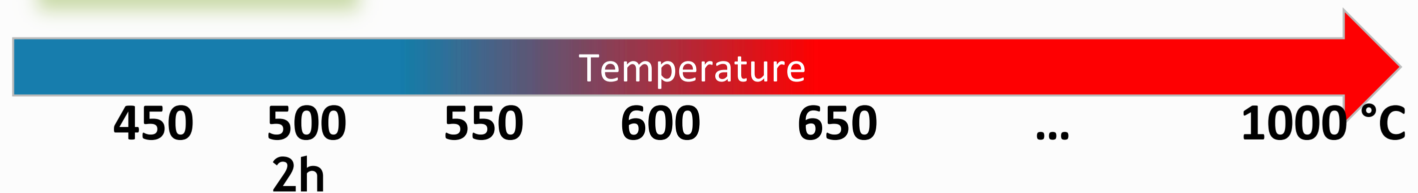
Voltage	Electric field	Reference	450 °C	500 °C	550 °C
V	$(MV/cm)^{0.5}$	Liftetime (Year)			
1.115	0.498	10^{16}	10^{13}	10^{11}	10^{9}
1.98	0.669	10^{13}	10^{11}	10^{9}	10^{8}
2.5	0.745	10^{12}	10^{10}	10^{8}	10^{7}

Reliability validated for W/ ULK at 550°C, 2h [2]

[1] C. Fenouillet-Beranger et al., *SSDM 2015,* [2]: V. Lu et al., VLSI 2017

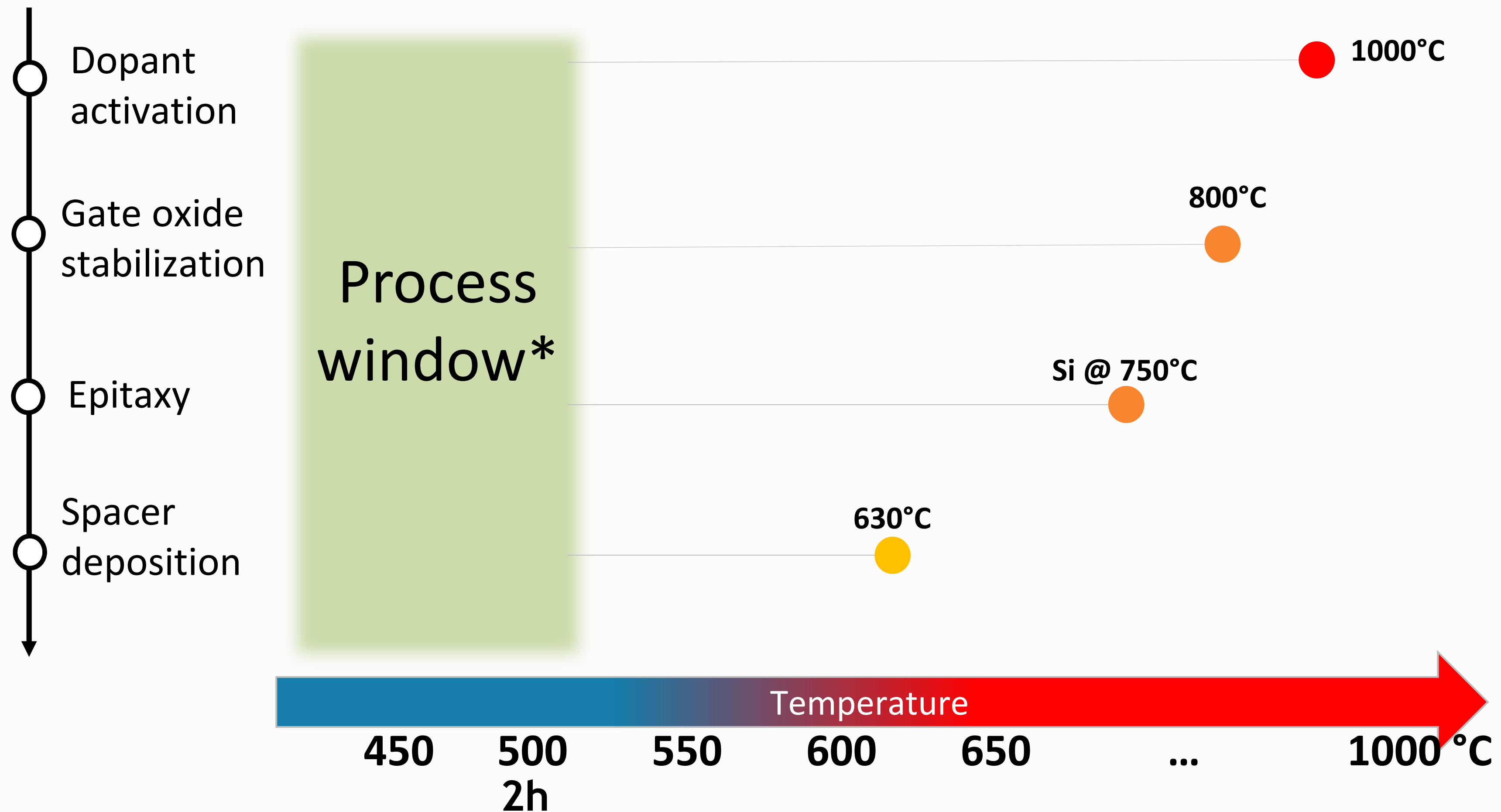
Thermal budget summary

Process window*



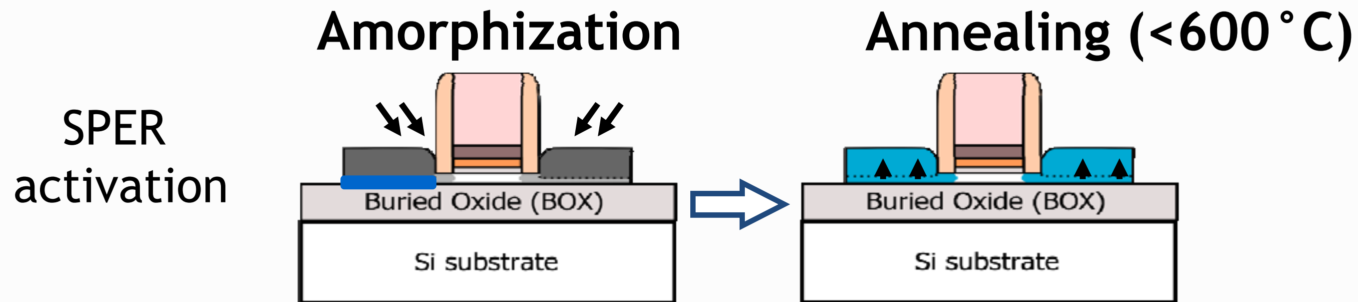
Rmk: * For 14 nm FDSOI and ULK interconnections

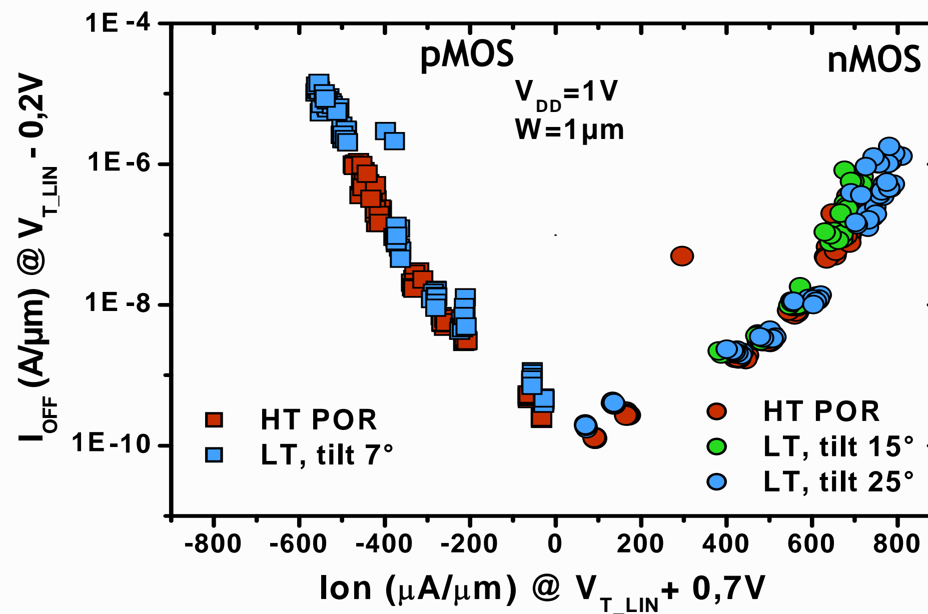
Thermal budget summary



Rmk: * For 14 nm FDSOI and ULK interconnections

Low temperature junctions



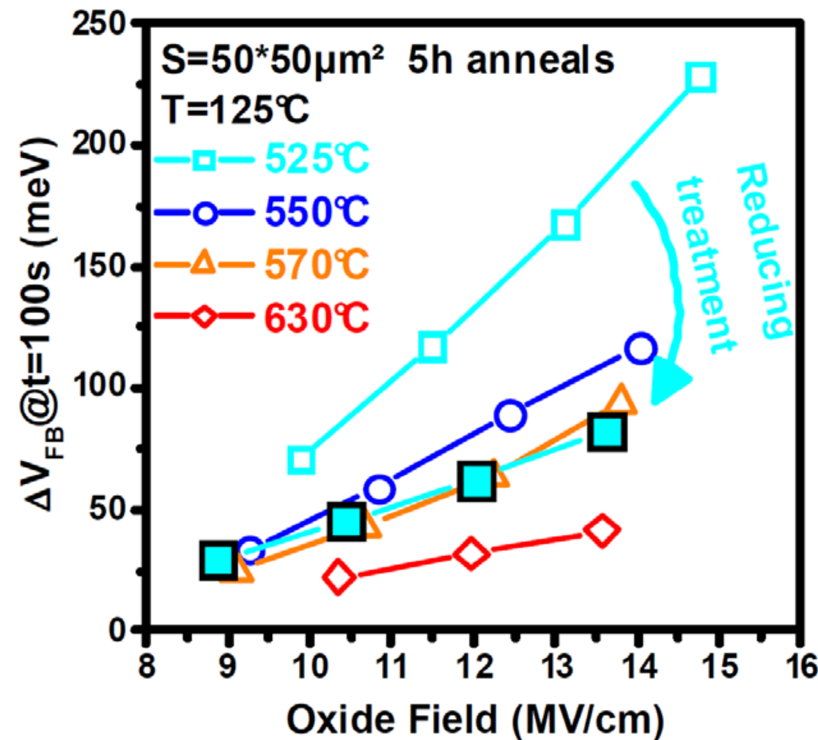


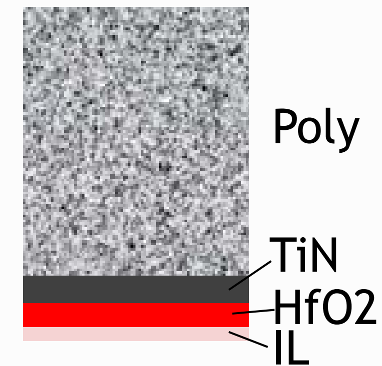
28nm FDSOI low thermal budget junction

Same I_{ON}-I_{OFF} trade off as HT POR

Low temperature gate stack

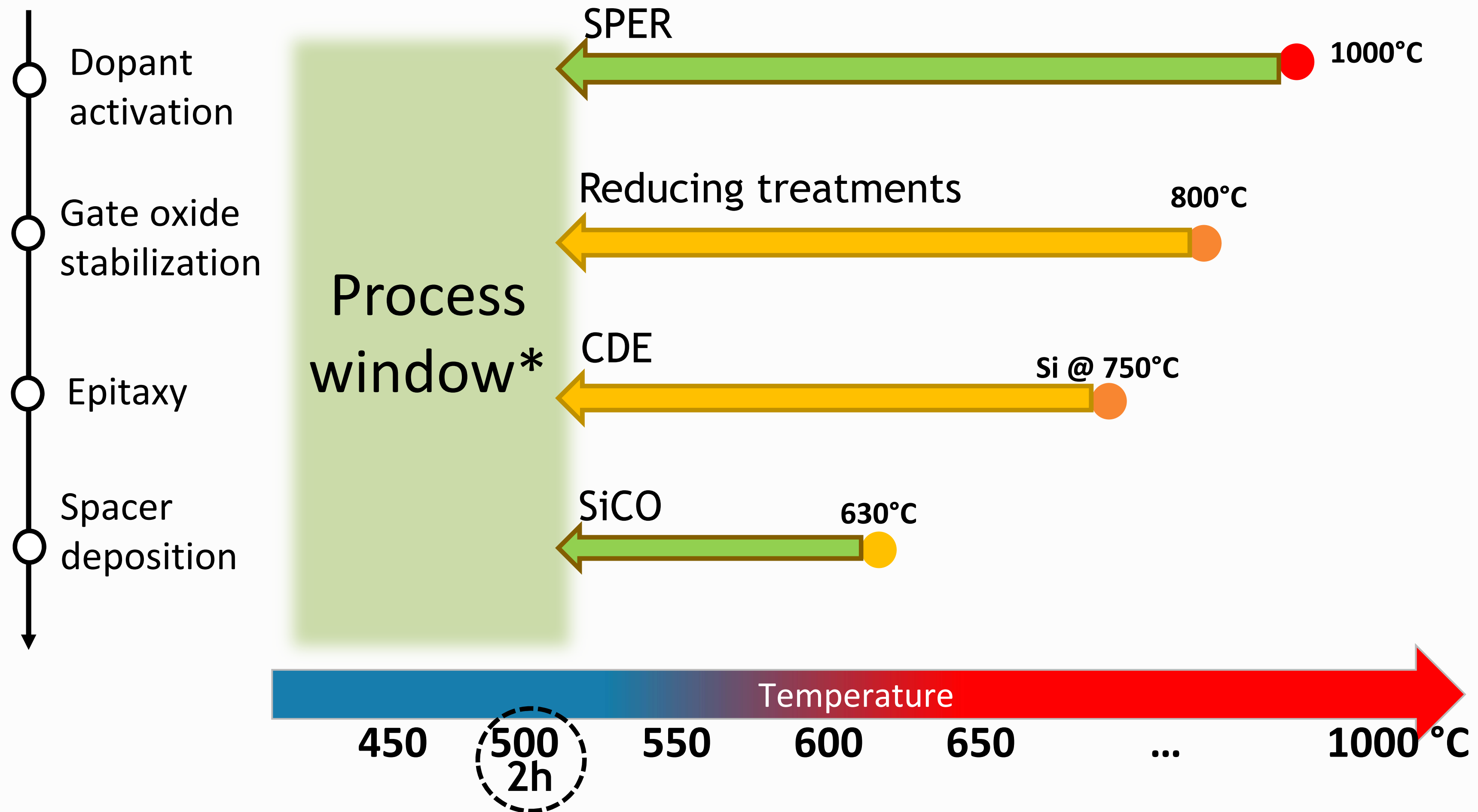
Degradation of NBTI with low thermal budget





Options exists to improve the NBTI reliability within 525°C TB

Thermal budget summary



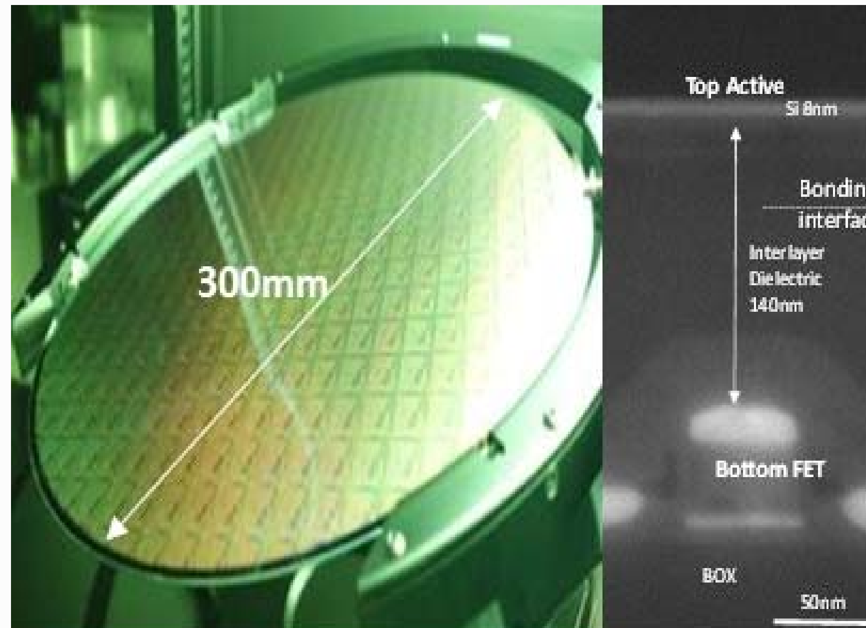
All the bricks TB are reaching the bottom stability

Rmk: lowering TB is a general need: Ge and III-V devices

Rmk: * For 14 nm FDSOI and ULK interconnections

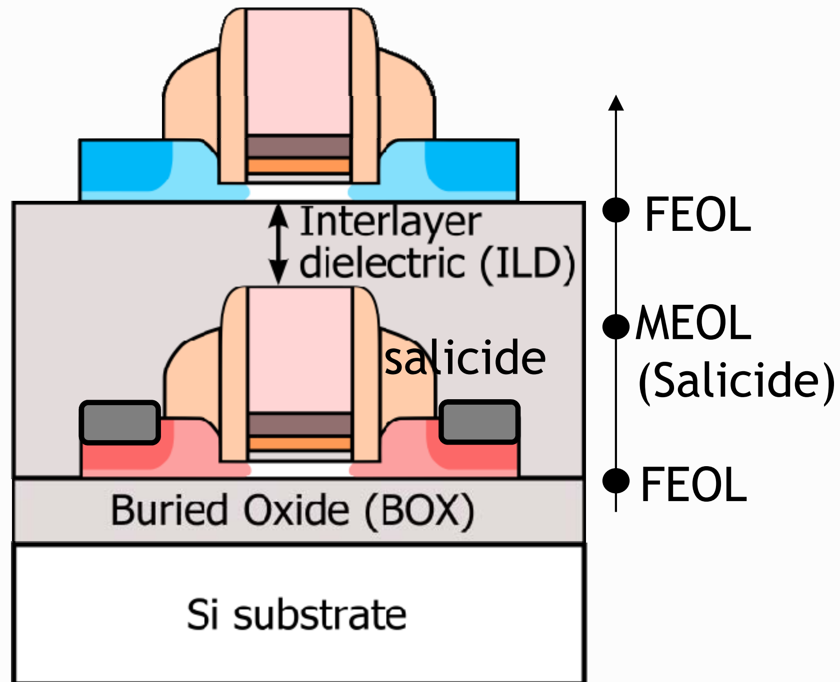
Manufacturability: Top channel creation

Si Thin film transfer by SOI bonding



SOI transfers above MOSFETs demonstrated in 300mm
Low thermal budget<400°C
Perfect cristalline quality and thickness control

Manufacturability: contamination

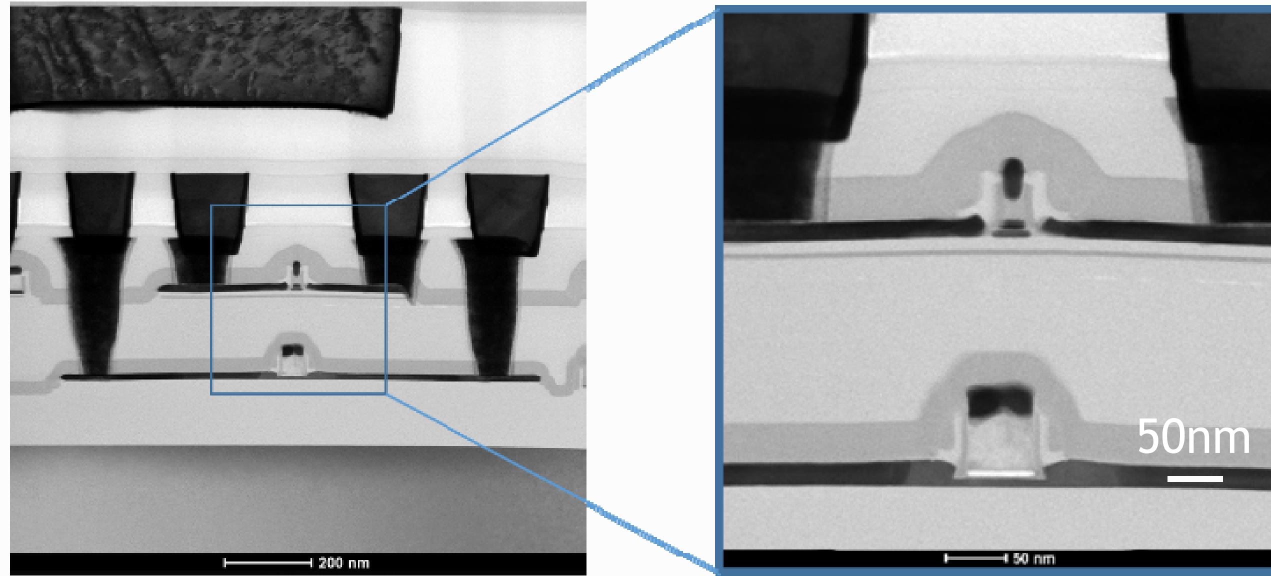


	Ni (at/cm²)
cleaning before bonding	< 9,4E8
bonding annealing	< 9,4E8
High-k deposition	2.9E+09
gate stack etch	8,3E9
epitaxy	6.40E+09
dopant activation annealing	2,8E9

bevel edge VPD-DC-ICPMS

Manufacturing compatible contamination

300mm fab demonstration



- ✓ **Nanometric lithography alignment at wafer scale**
- ✓ **3D contact size=100nm**
- ✓ **10nm thin top active layer**

Conclusions

The 3D contact characteritics offers a large set of applications with timing depending on the technology complexity.

For computing, first assessments are promising and place and route tools are needed to fully quantify the performance.

3D sequential is demonstrated in a 300mm industrial environment

Bottom tier (MOSFET and interconnection) max TB =500°C 2h

All the bricks for top FET can be within this 500°C TB limitation

Thank you to all Cool Cube™ co-authors

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Thank YOU for your attention