

3D Memory Patent Landscape Analysis

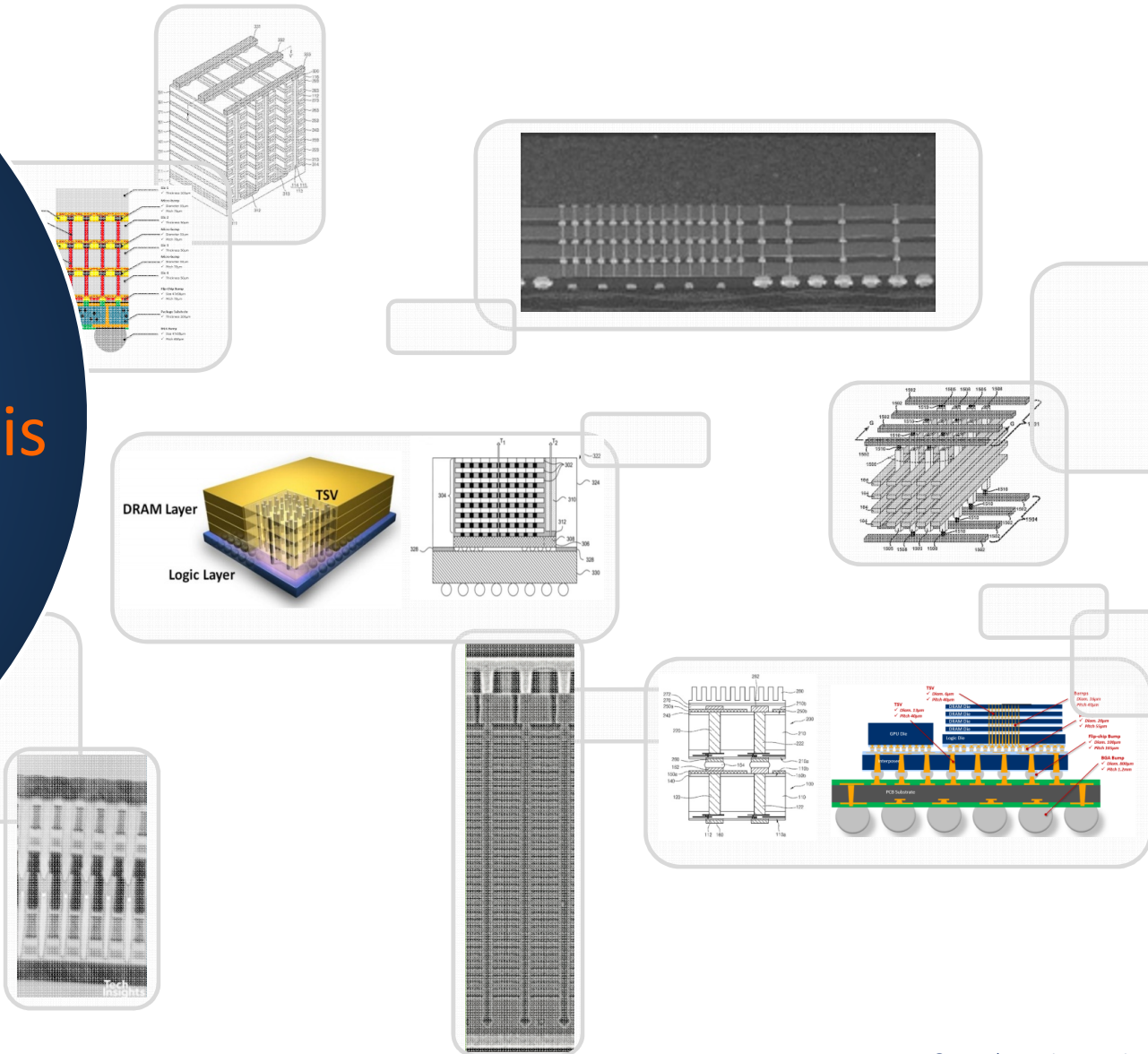
D43D Workshop

June 2017

Audrey Bastard

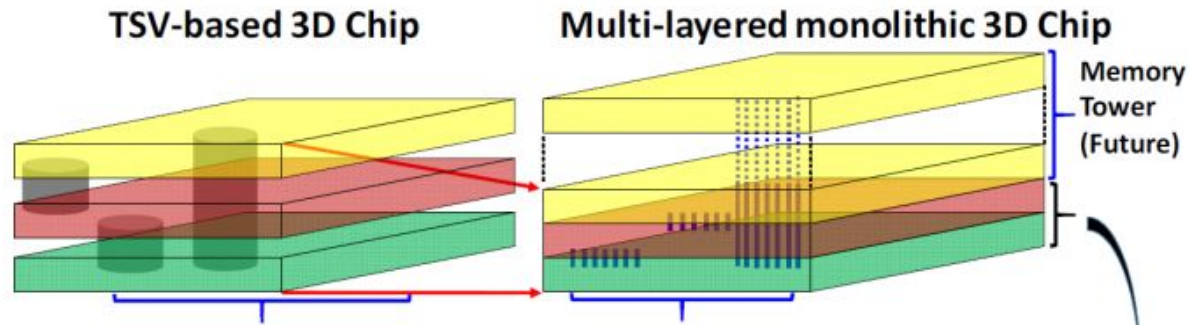
Technology & Patent Analyst

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INTRODUCTION

3D Memory



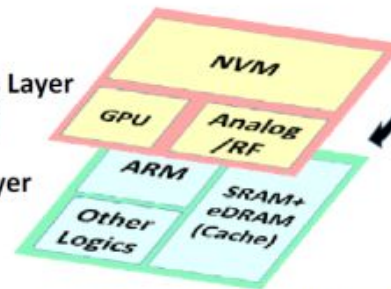
Through Silicon Via(TSV)

Normal Via(Higher bandwidth)

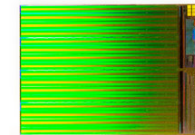
	Through Silicon Via (TSV)	Monolithic 3D integration
Diameter	2-4 μm	<200 nm
Height	20-50 μm	<300 nm
Alignment accuracy	$\sim 1 \mu\text{m}$	$\sim 20 \text{ nm}$
Reference	ITRS 2012~2015	This work

Heterogeneous Layer (Layer 2)

Pure Logic Layer (Layer 1)



3D Monolithic (2013)

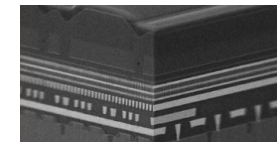


3D NAND Die

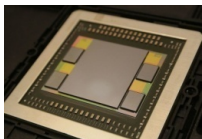
Micron Website



3D Cross-Point array ReRAM

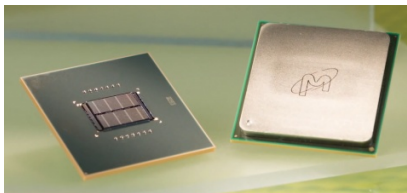


Western Digital, FMS 2016



High Bandwidth Memory

<http://www.pcgameshardware.de>



Hybrid Memory Cube

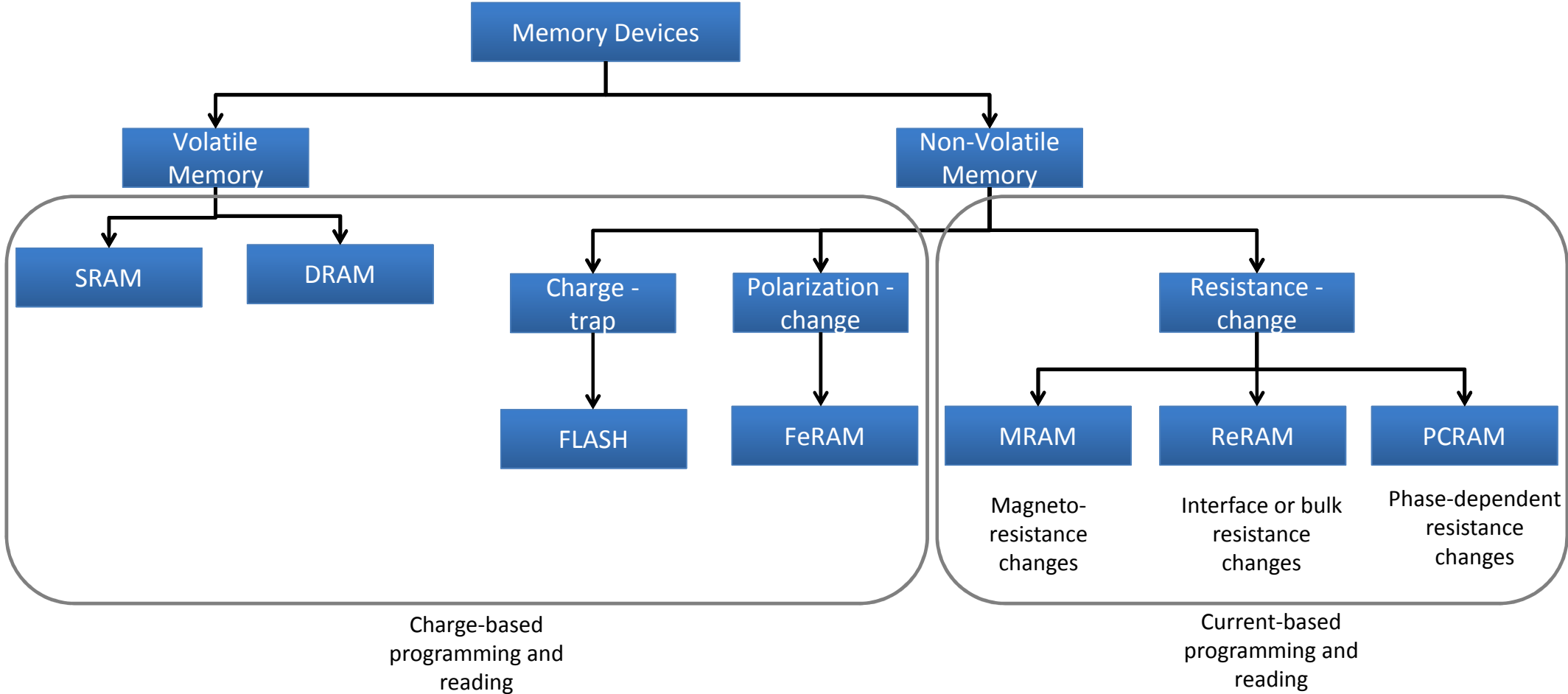
<https://www.golem.de>

1st part of this presentation

2nd part of this presentation

INTRODUCTION

Memory Types



INTRODUCTION

Methodology for patent search, selection and analysis

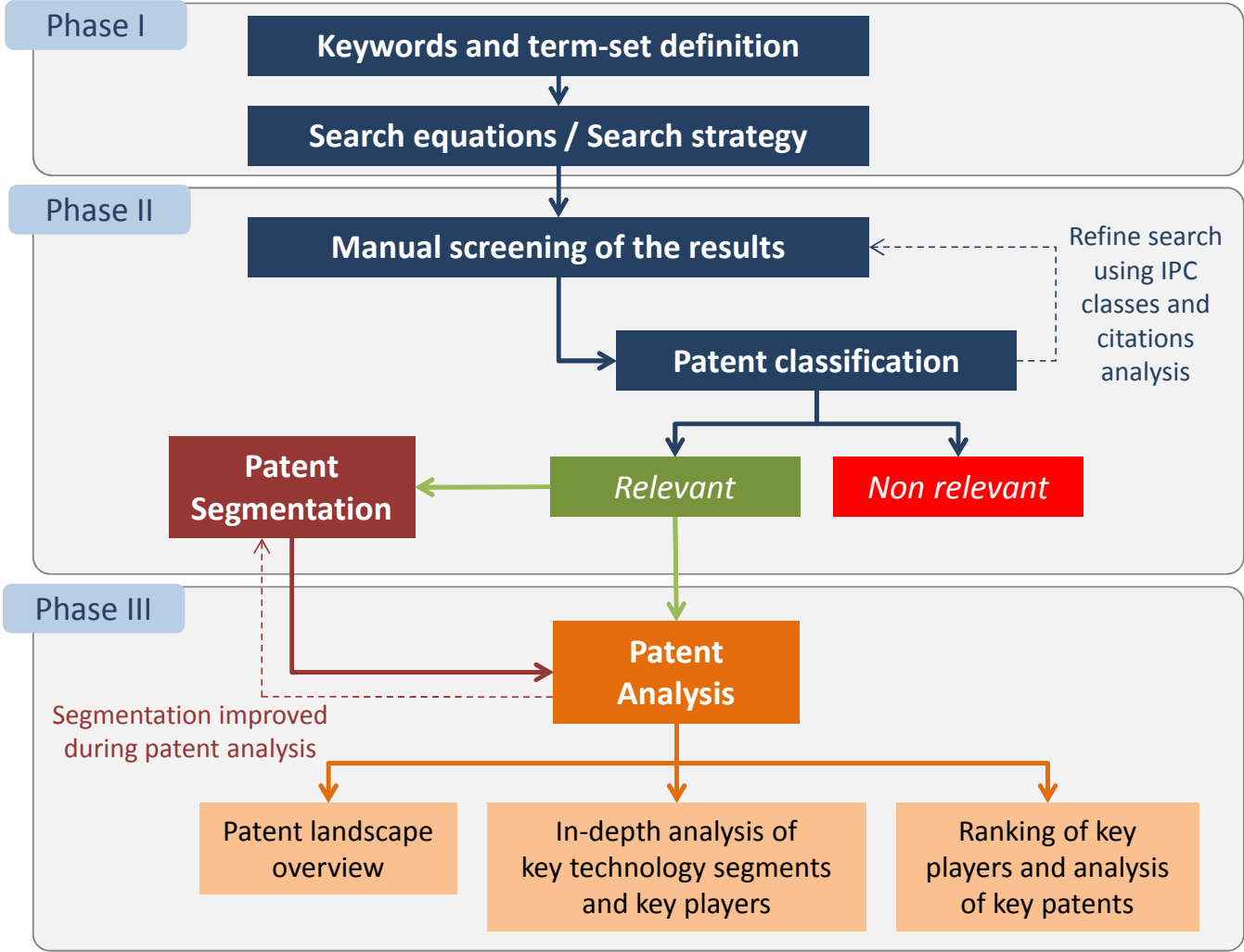


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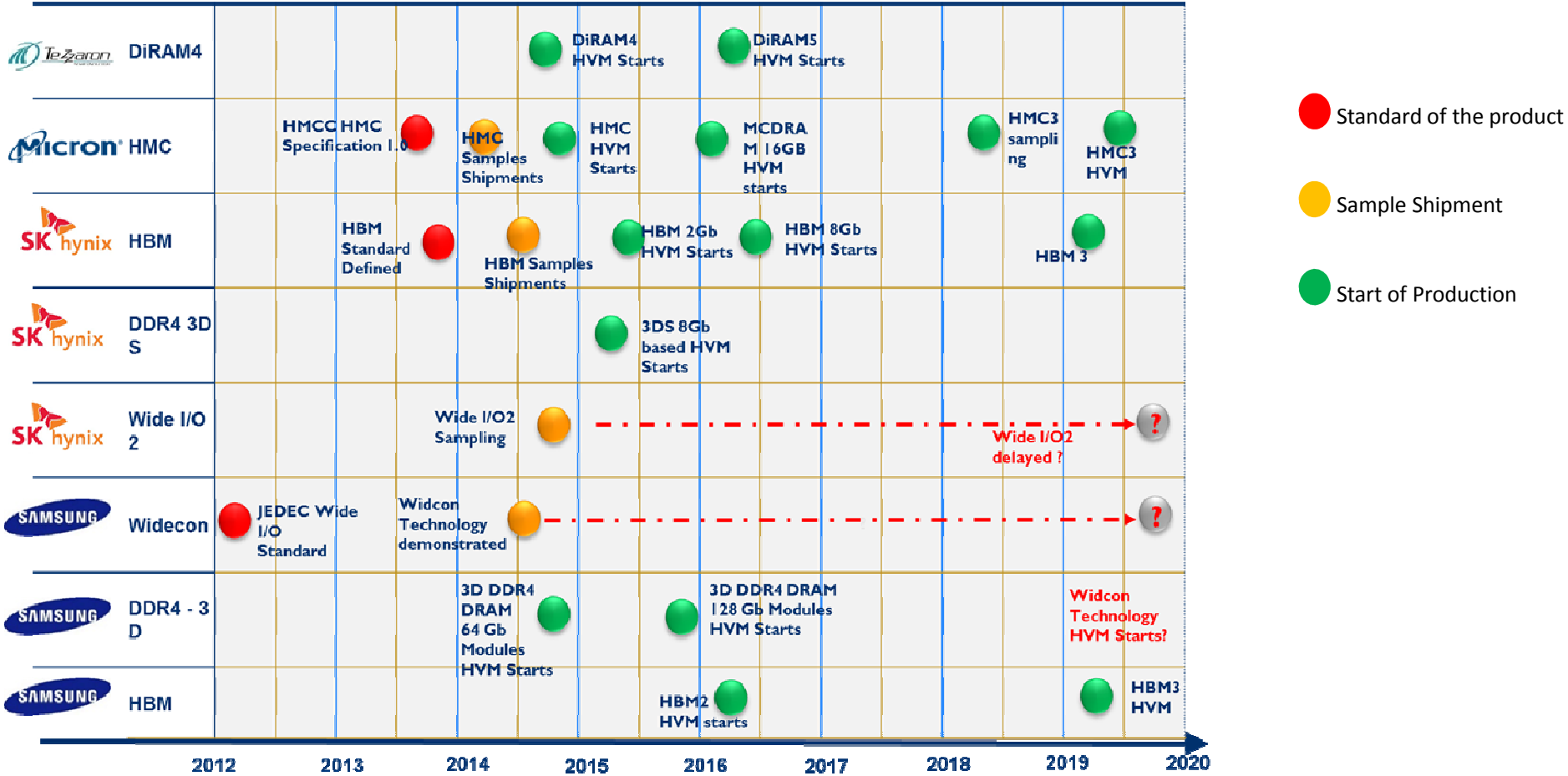
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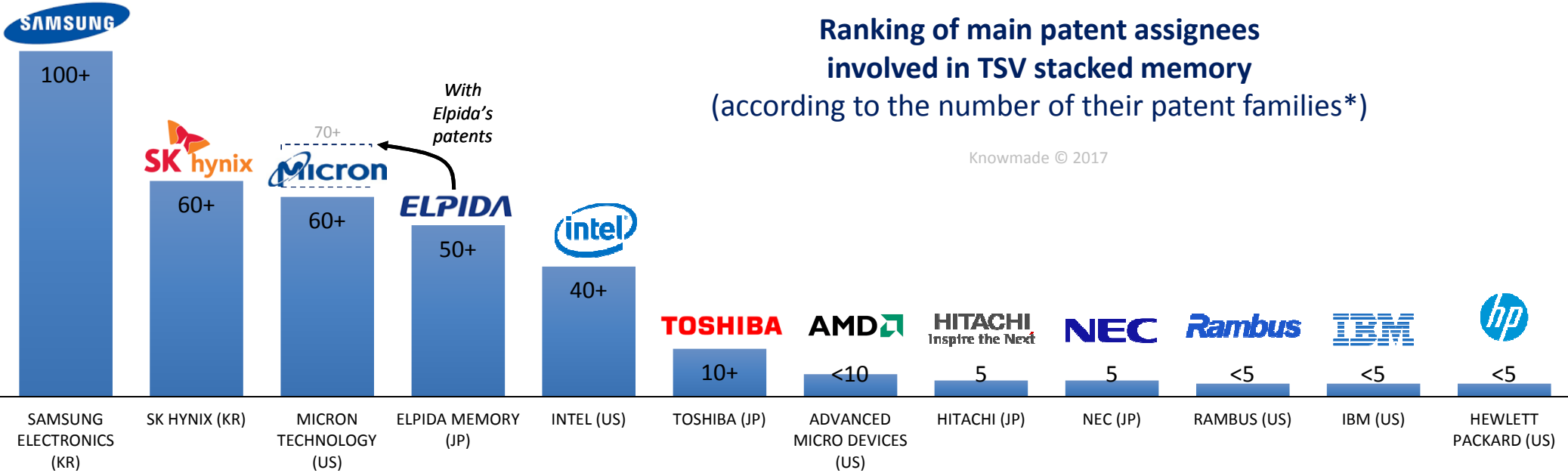
INTRODUCTION

TSV Stacked Memory Roadmap



IP OVERVIEW

Main patent assignees in TSV stacked memory



- Mainly industrial players from USA, Japan and Korea
- Micron/Elpida and Samsung own more than 40% of patents together
- Most of Elpida's patents were acquired by PS4 Luxco in 2013
- R&D Labs have only few patents (Carnegie Mellon University, University of California, ITRI, ETRI, Hiroshima University)
- Tezzaron holds 6 patent families on 3-dimensional IC design (not focus on stacked memory)

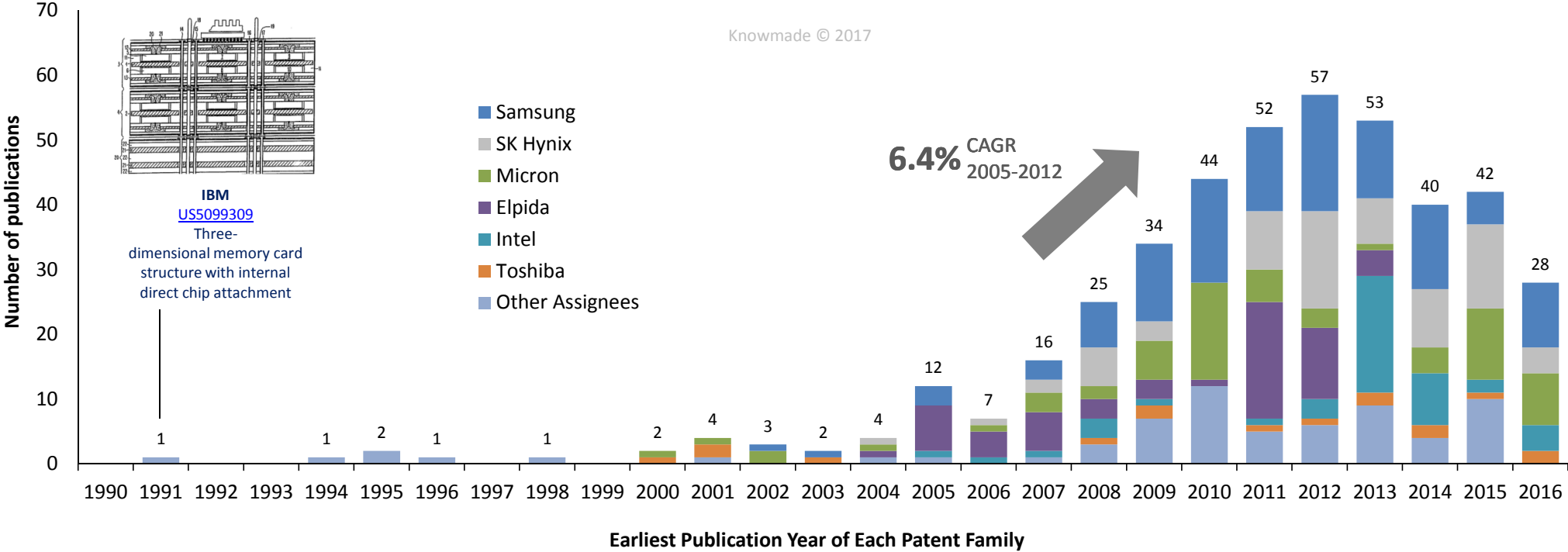
* A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor. A first application is made in one country – the priority country – and is then extended to other countries.

PATENT LANDSCAPE OVERVIEW

Time evolution of patent publications in TSV stacked memory

Patenting activity in TSV stacked memory

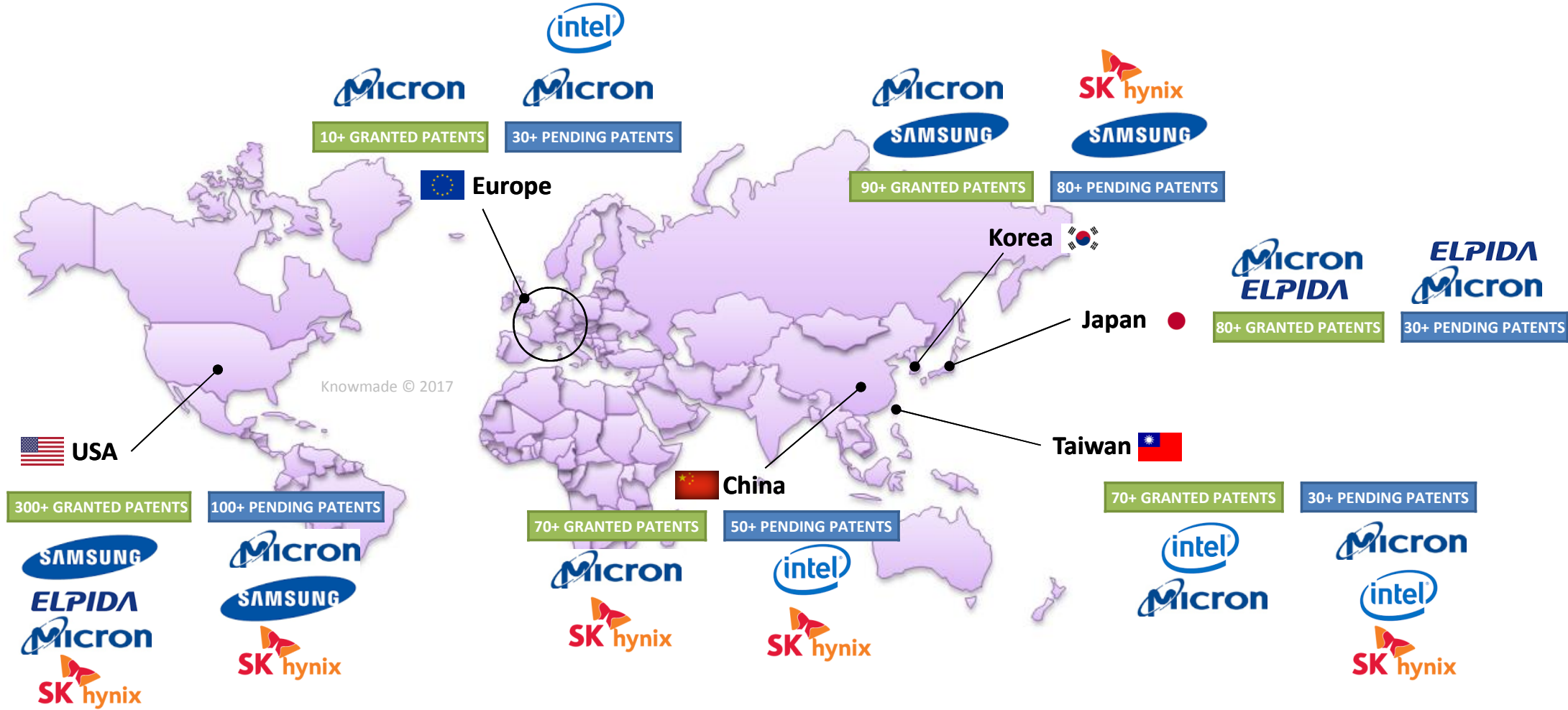
1,500+ patents grouped in 400+ patent families*



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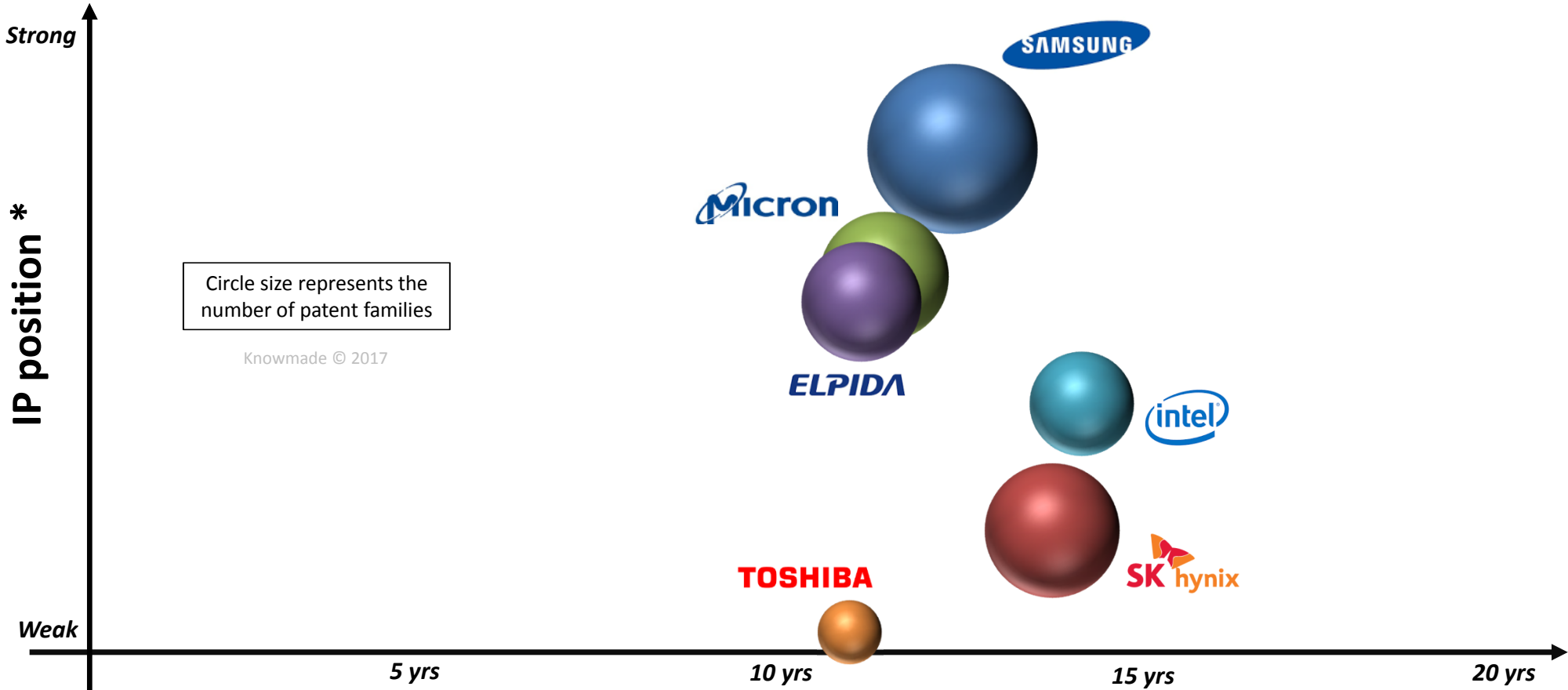
PATENT LANDSCAPE OVERVIEW

Geographic map of patenting activity of main IP players involved in TSV stacked memory



IP POSITION OF MAIN PATENT ASSIGNEES

IP position vs. remaining lifetime of enforceable patents

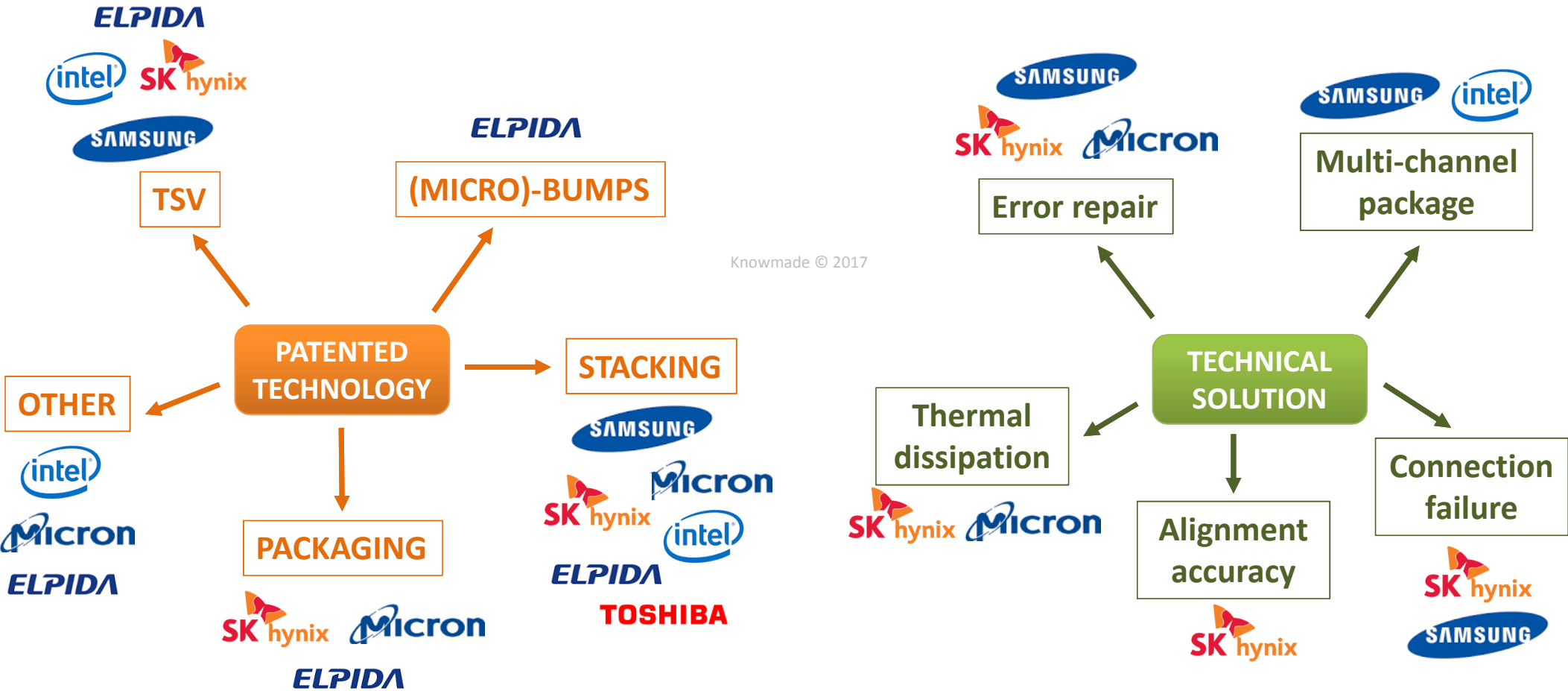


*Indicators: number of granted patents, number of pending patent applications, geographical coverage, IP strategy, IP leadership, IP strength, IP blocking potential

Remaining lifetime of granted patents

PATENT SEGMENTATION

Technologies patented by key IP players in TSV stacked memory

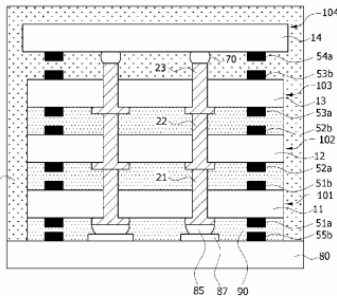


TECHNOLOGY OVERVIEW

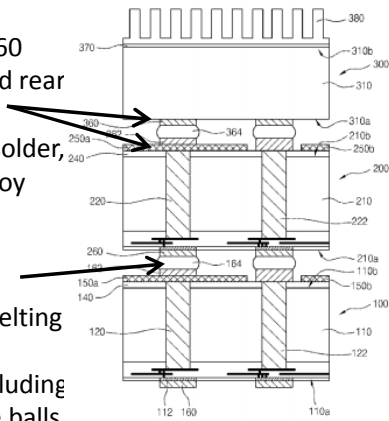
Technologies patented by key IP player in TSV stacked memory

Patented technologies used in SK Hynix HBM's package The 4 DRAM dies are connected together with TSV & micro-bumps

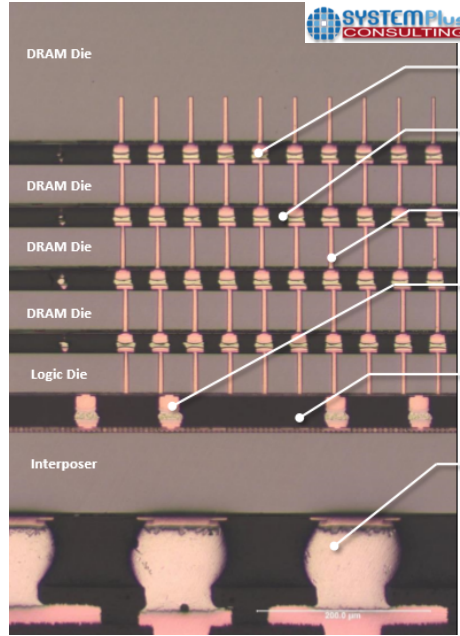
[US8592952](#) (2013)
Reduce misalignment between chips
→ magnetic force applied between the align patterns



[US9390997](#) (2015)
Connection electrodes 160 and 162 (front bumps and rear bumps)
→ formed of any one of solder, nickel, copper, tin and alloy thereof

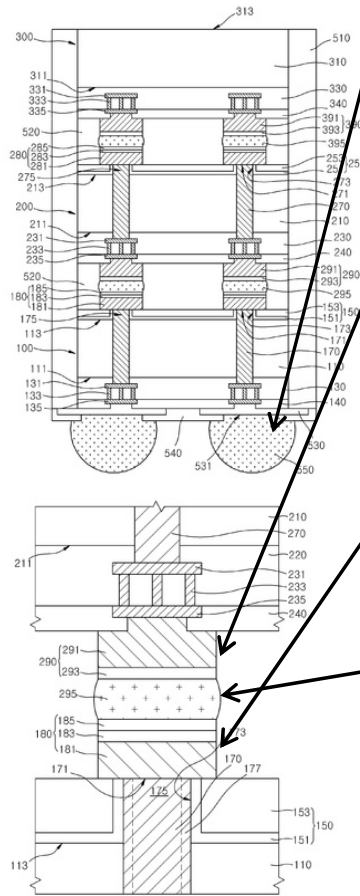


Connection member 164
→ solder having a low melting point or an anisotropic conductive film (ACF) including resin and fine conductive balls



HBM Package Cross Section, SEM View, System Plus Consulting

- Micro-bump**
 - ✓ Diameter 16µm
 - ✓ Pitch 40µm
- Underfill**
 - ✓ Thickness 19µm
- TSV**
 - ✓ Diameter 6µm
 - ✓ Depth 46.5µm
 - ✓ Pitch 40µm
- Micro-bump**
 - ✓ Diameter 20µm
 - ✓ Pitch 55µm
- Underfill**
 - ✓ Thickness 33µm
- Flip-Chip Bump**
 - ✓ Size 100µm
 - ✓ Pitch 200µm



- [US9257413](#) (2015)
Outer connection terminals 550
→ plurality of solder balls 2D arrayed.
→ area of a surface on which the outer connection terminals are arrayed can be maximized (even though a width of the lower semiconductor chip is reduced)
- Intermediate front side bumps 290
→ front side bump body 291 (Cu) contacting the chip contact portion 235
→ wetting layer 293 (Ni) stacked on the front side bump body 291.
- Lower backside bumps 180
→ Include also oxidation resistant layer 185(Au)
- Conductive adhesives 295 (solder layers)
→ disposed on the respective wetting layers 293
→ combined with the lower backside bumps

CONCLUSION

Patent Landscape analysis TSV Stacked Memory






Top-5 patent assignees					
IP position	Very Strong	Strong	Low	Very Low	Medium
Main countries of patent filings	USA Korea	Worldwide	USA	USA Japan	USA Taiwan
Main patented technology	Control of the stack, Wafer to wafer technique	Memory technology improvement, Interconnection stacking	Stacking Issues: dissipation, adhesion,...	Stacking Issues	Method for accessing memory, Thinner package substrates
Main technical issues in patents	Connection Failure Multi-Channel Package Error Repair	Thermal Dissipation Error Repair	Alignment Accuracy Error Repair Thermal Dissipation Connection Failure	Alignment Accuracy Connection Failure	Multi-Channel Package Alignment Accuracy
Products	3D DDR4 DRAM production in 2014, HBM2 4Gb and 8Gb in 2016	Production of 16Gb HMC Gen2 in 2014 with Intel	Production of HBM1 2Gb in 2014, Production of 3DS DDR4 8Gb and Wide I/O2 in 2015, Production of HBM2 4Gb and 8Gb in 2016 HBM3 in 2020	In 2017/2018, 1To package of 16 NAND dies TSV stacked 2To package will be proposed in 2019	Production of 16Gb HMC Gen2 in 2014 with Micron
Patent litigations	Nov-2014 ELM 3D as plaintiff for patent infringement against Samsung Final Decision in Q2 2017	Nov-2014 ELM 3D as plaintiff for patent infringement against Micron Final Decision in Q2 2017	Nov-2014 ELM 3D as plaintiff for patent infringement against SK Hynix Final Decision in Q2 2017	No	No

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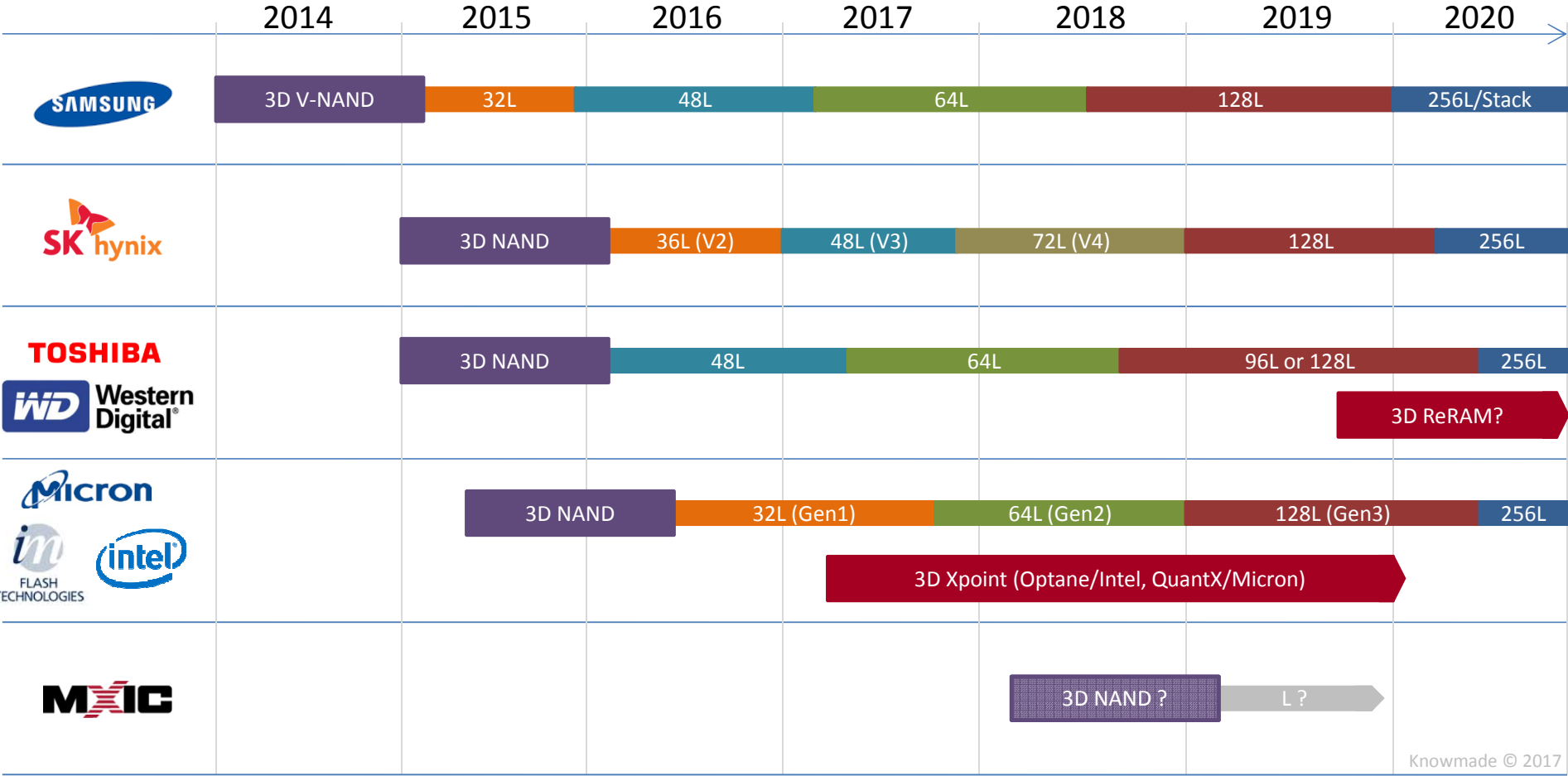
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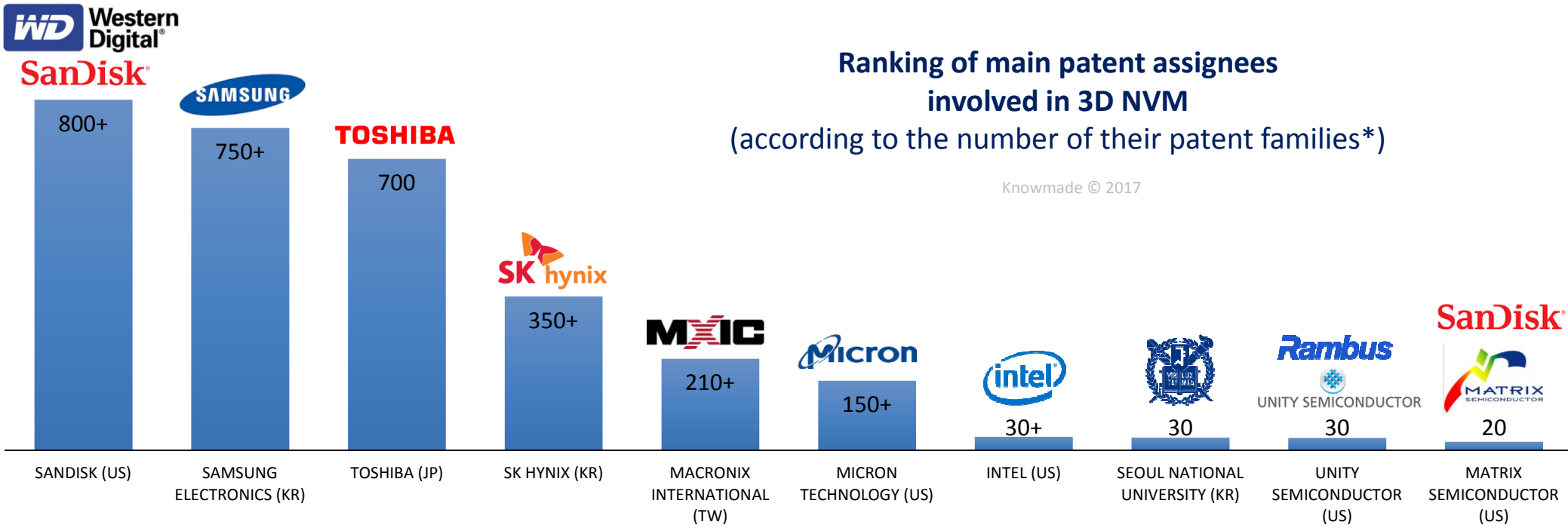
3D NVM Roadmap



Knowmade © 2017

IP OVERVIEW

Main patent assignees in 3D NVM

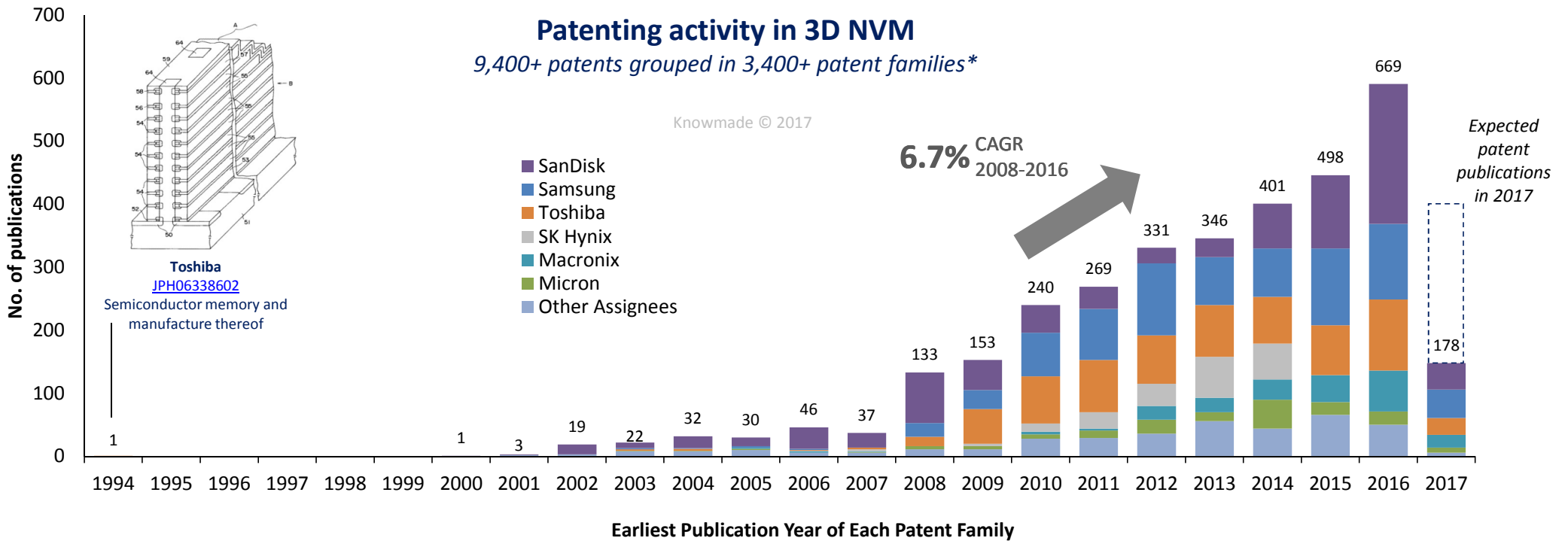


- Mainly industrial players from USA, Korea, Japan and Taiwan
- Top 3: SanDisk/Western Digital, Samsung and Toshiba own more than 65% of patents together
- Western Digital acquired SanDisk in 2016
- R&D Labs have only few patents (Seoul National University)
- Rambus acquired Unity Semiconductor in 2012
- SanDisk acquired Matrix Semiconductor in 2005

* A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor. A first application is made in one country – the priority country – and is then extended to other countries.

IP OVERVIEW

Time evolution of patent publications in 3D NVM

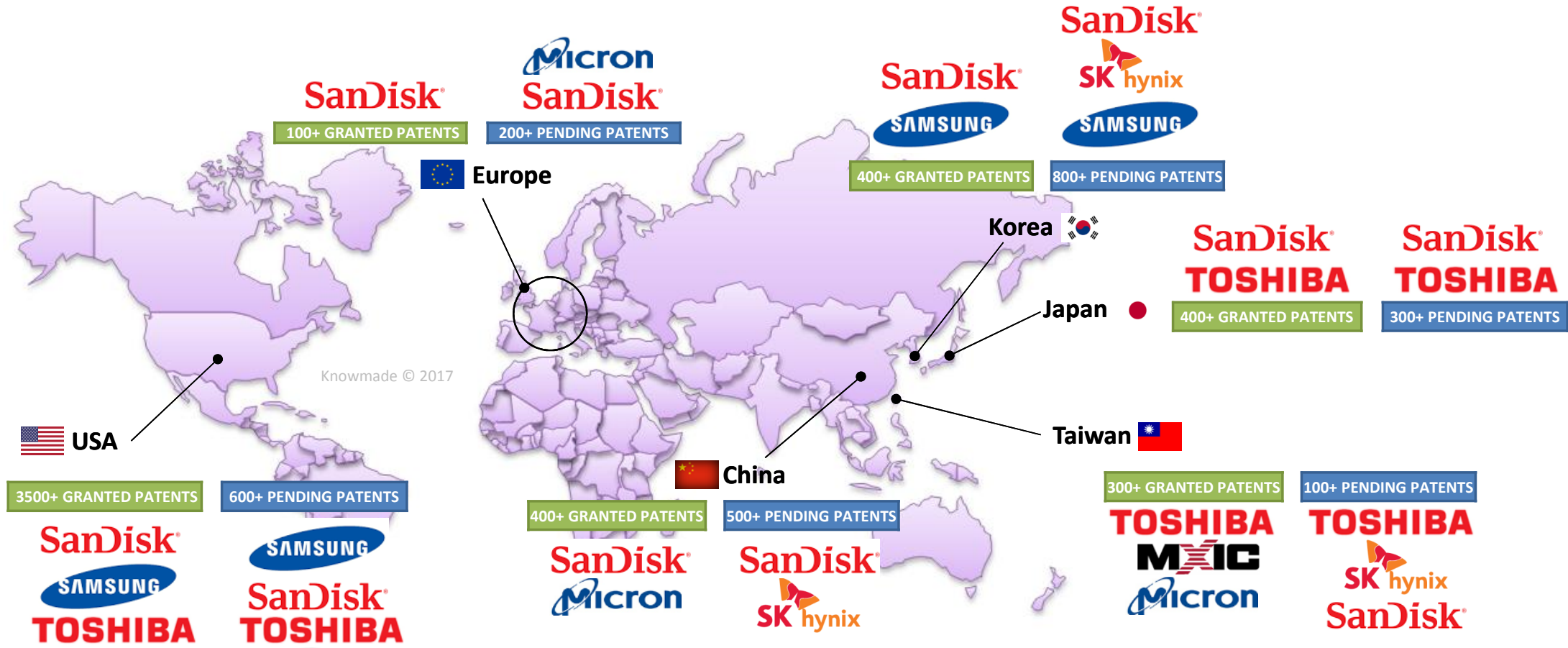


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Note: The patent search was done in June 2017, thus the data corresponding to the year 2017 are not complete. At the time of the patent search, 178 patent families had been published in 2017.

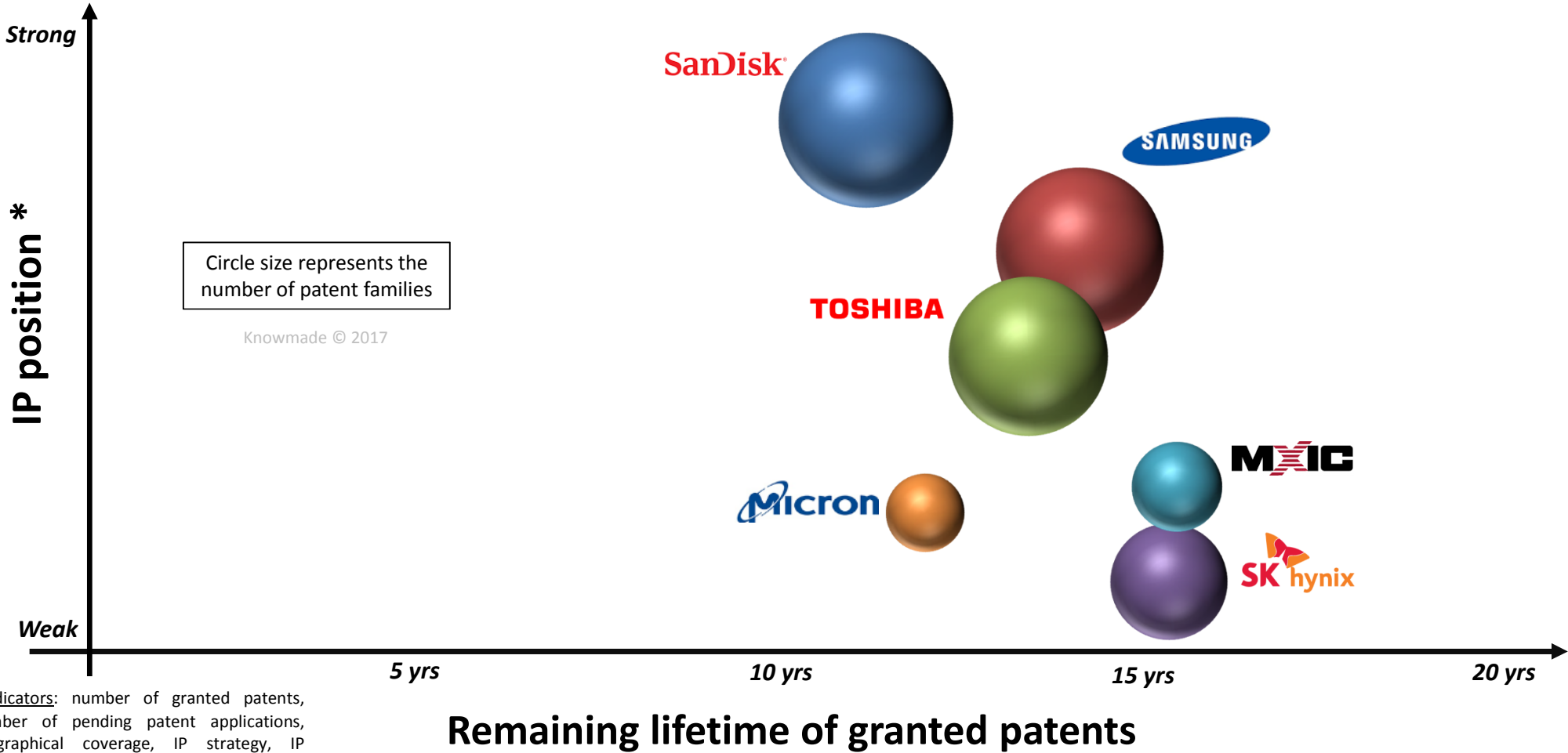
IP OVERVIEW

Geographic map of patenting activity of main IP players involved in 3D NVM



IP POSITION OF MAIN PATENT ASSIGNEES

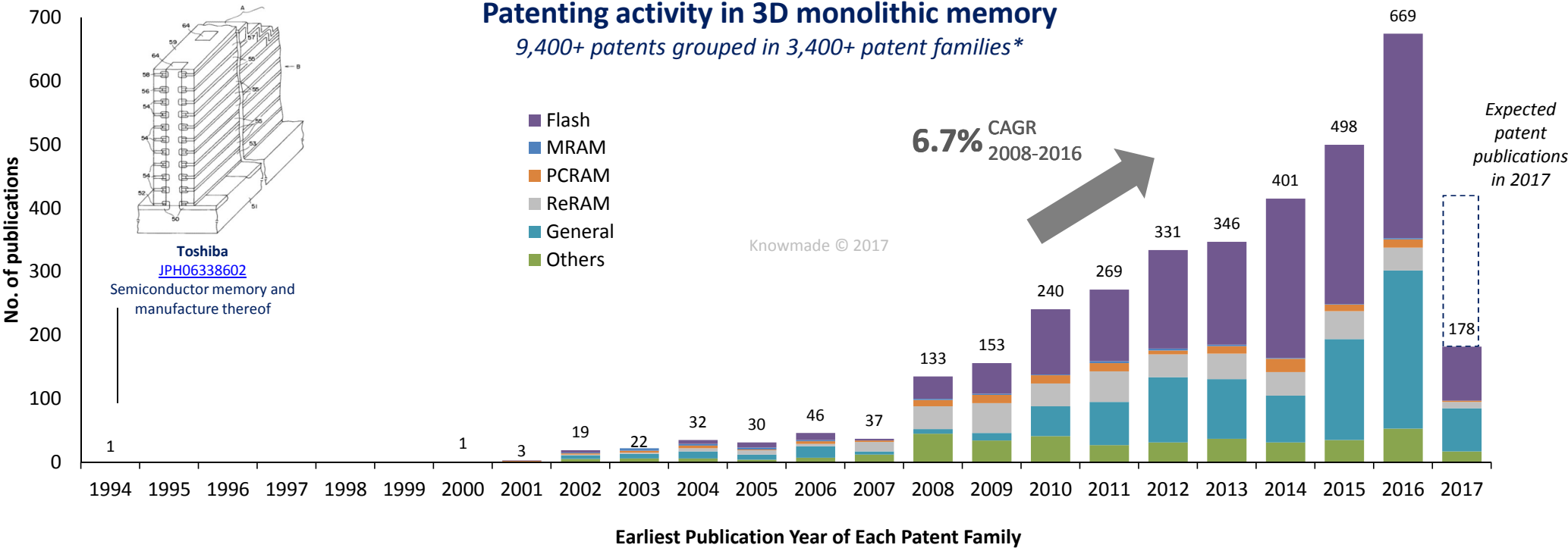
IP position vs. remaining lifetime of enforceable patents



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PATENT SEGMENTATION

Memory types timeline of publication in 3D NVM

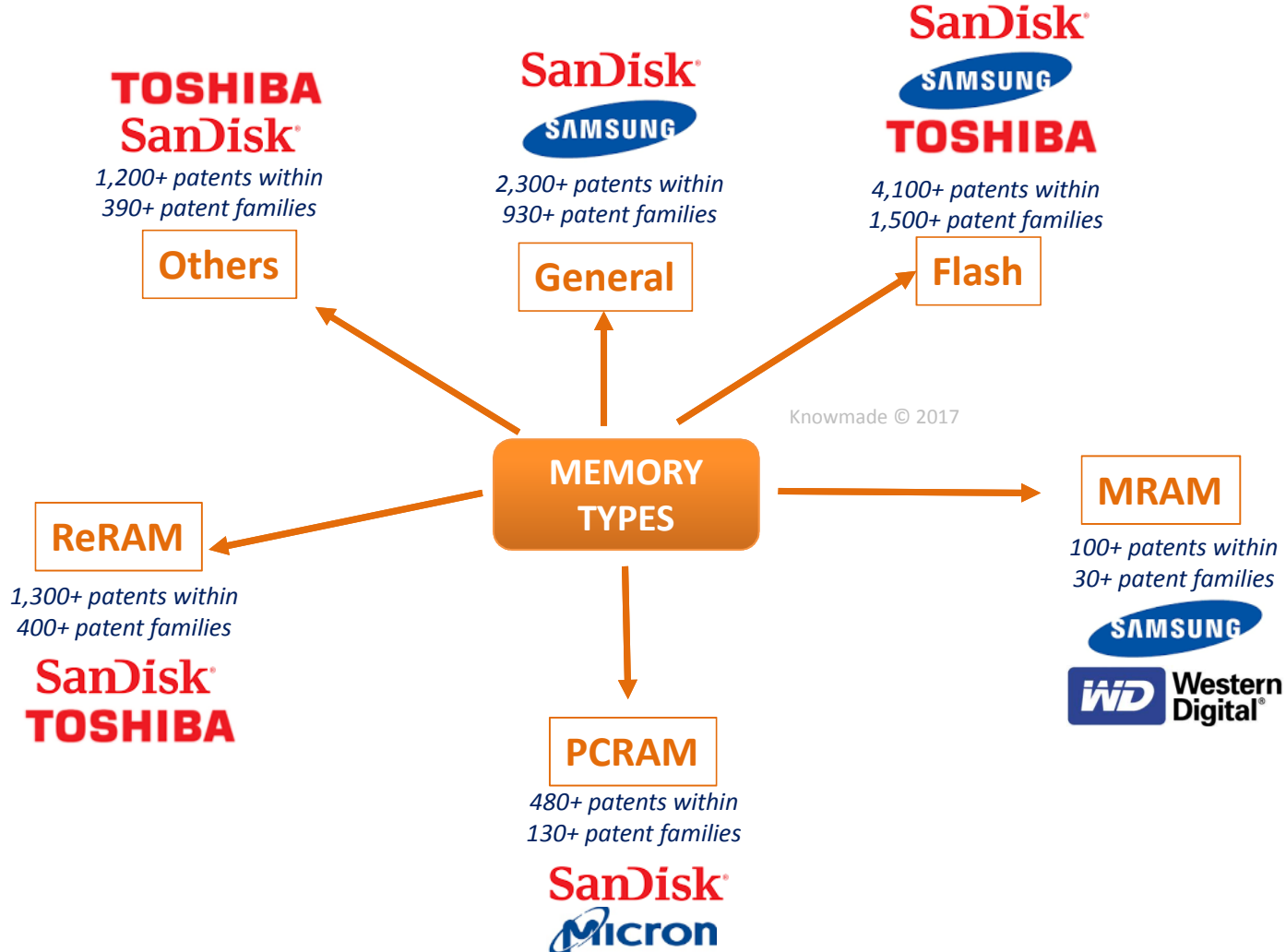


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PATENT SEGMENTATION

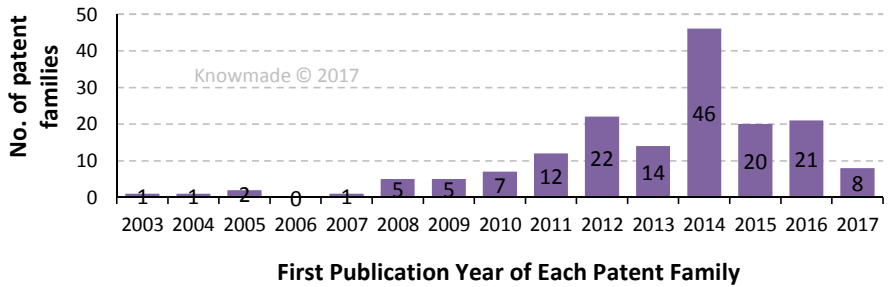
Memory types by key IP players in 3D NVM



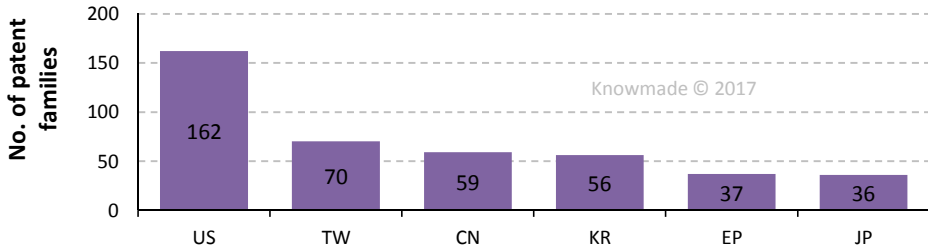
TECHNOLOGY OVERVIEW

Micron Technology IP Portfolio in 3D NVM

722 patents within 165 patent families on 3D NVM

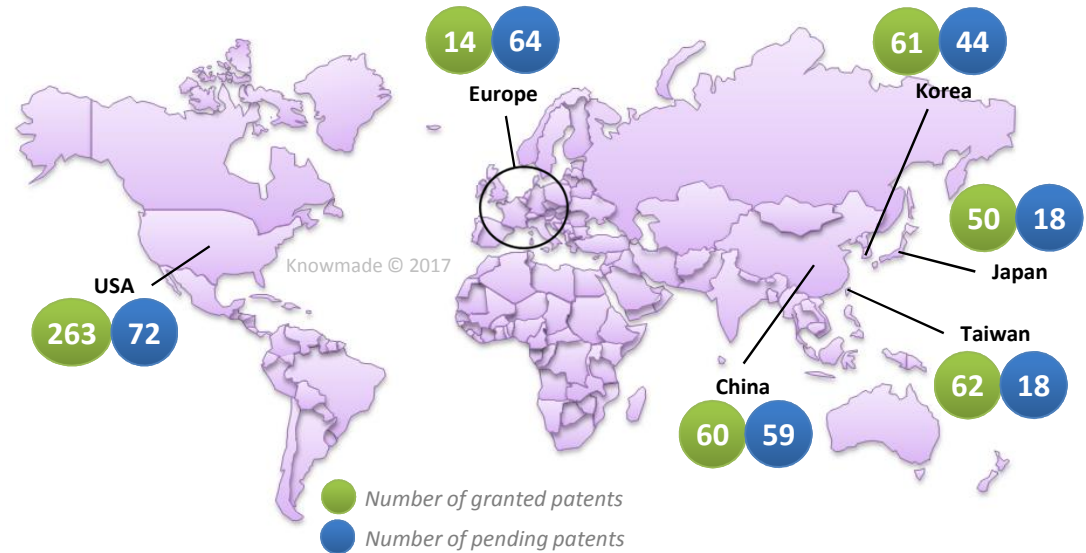


Countries of Patent Filings for Patents Related to 3D NVM



- In 2012-2013, Micron was actively working on improving 3D memory architectures as evidenced by the numerous patents published in 2014.
- Half of Micron's patent publications are related to Flash Memories
- Micron doesn't have a worldwide IP strategy in 3D NVM. Indeed, Micron has a very strong IP presence in USA and neglect Europe and Asian countries

Alive IP for 3D NVM



Segmentation for Patents Related to 3D NVM

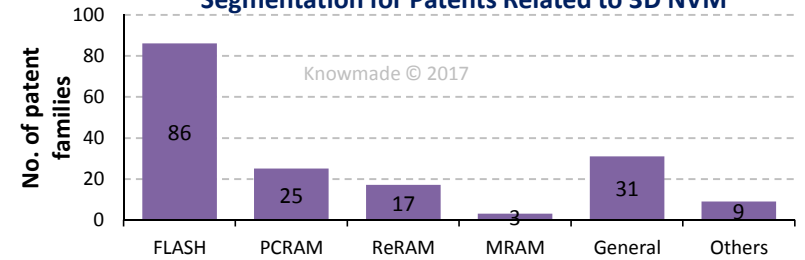


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CONCLUSION

- First patents related to 3D memory technologies (TSV Stacked or 3D NVM) were published in the 1990s, but patenting activity really started in the 2000s with a strong increase since 2007-2008 and first marketed products appeared in 2014.
- The patent landscape of 3D memories (TSV Stacked or 3D NVM) is led by the microelectronics giants, offering few space for new entrants and heralding inevitable patent battles.

Top patent assignees IP position	SanDisk Western Digital		SAMSUNG		TOSHIBA		SK hynix		MXIC		Micron intel	
	TSV Stacked	3D NVM	TSV Stacked	3D NVM	TSV Stacked	3D NVM	TSV Stacked	3D NVM	TSV Stacked	3D NVM	TSV Stacked	3D NVM
IP position	/	Very Strong	Very Strong	Strong	Very Low	Medium	Low	Very Low	/	Low	Strong	Low
Last and future Products	/	3D NAND 64L/512Gb (end 2017) 3D ReRAM In 2019	HBM2 4Gb and 8Gb in 2016 HBM3 in 2020	3D V-NAND Gen4 64L/512Gb (June 2017) “Z-NAND” prototype	2017/2018 : 1To package of 16 NAND dies TSV stacked, 2To package in 2019	3D NAND 64L/512Gb (end 2017) 3D ReRAM In 2019	Production of HBM2 4Gb and 8Gb in 2016 HBM3 in 2020	3D NAND Gen4 72L/256Gb (Q2 2017) 3D NAND 72L/512Gb (end 2017)	/	3D-NAND product introduction in 2018	MCDRAM production in 2016 HMC3 in 2020	3D NAND Gen2 64L/512Gb (2017) 3D Xpoint Optane Intel/QuantX Micron (2017)

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