leti
cea tech

ANNUAL
RESEARCH REPORT
2015

SILICON TECHNOLOGIES AND COMPONENTS

Leti, technology research institute

TECHNOLOGY RESEARCH INSTITUTE

LETI AT A GLANCE

Founded in **1967**

Based in **France** (Grenoble)
with offices in **USA** (Silicon Valley)
and **Japan** (Tokyo)

350
industrial partners

1,900
researchers

Committed to innovation, Leti's teams create **differentiating solutions in miniaturization and energy-efficient technologies** for its industrial partners.

Leti is a technology research institute at CEA Tech and a recognized global leader focused on miniaturization technologies enabling energy-efficient and secure IoT. Leti delivers solid expertise throughout the entire IoT chain, from sensors to data processing and computing solutions. Leti pioneered FDSOI low power platform for IoT, M&NEMS technology for low cost multisensors solutions, CoolCube™ integration for highly connected and cost effective devices.

Leti's mission is to pioneer new technologies, enabling innovative solutions to ensure Leti's industrial partners competitiveness while creating a better future. It tackles most current global issues such as the future of industry, clean and safe energies, health and wellness, sustainable transport, information and communication technologies, space exploration and safety & security.

For 50 years, the institute has built long-term relationships with its partners: global industrial companies, SMEs and startups. It tailors innovative and differentiating solutions that strengthen their competitiveness and contribute to creating new jobs. Leti and its partners work together through bilateral projects, joint laboratories and collaborative research programs. Leti actively contributes to the creation of startups through its startup program.

Leti has signed partnerships with major research technology organizations and academic institutions. It is a member of the Carnot Institutes network*.

**Carnot Institutes network: French network of 34 institutes serving innovation in industry.*

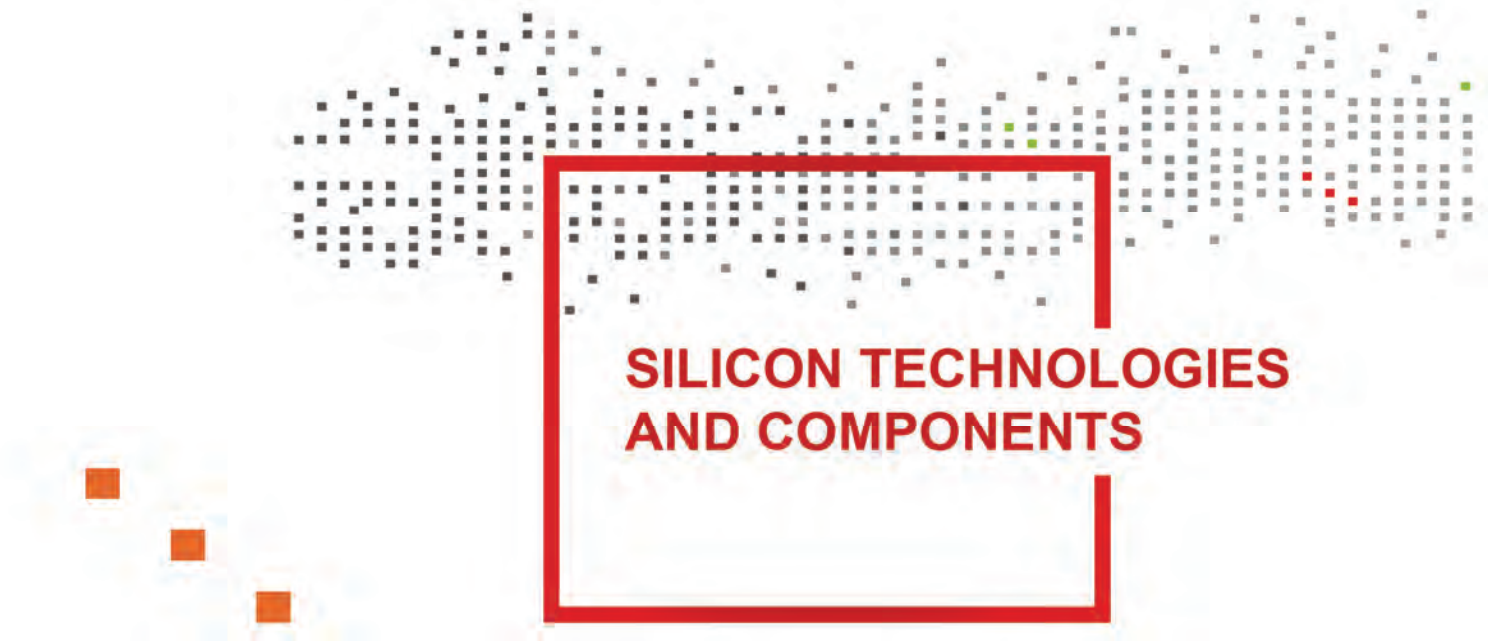
2,670
patents in portfolio

60
startups created

€315
million budget

700
publications each year

ISO 9001
certified since 2000

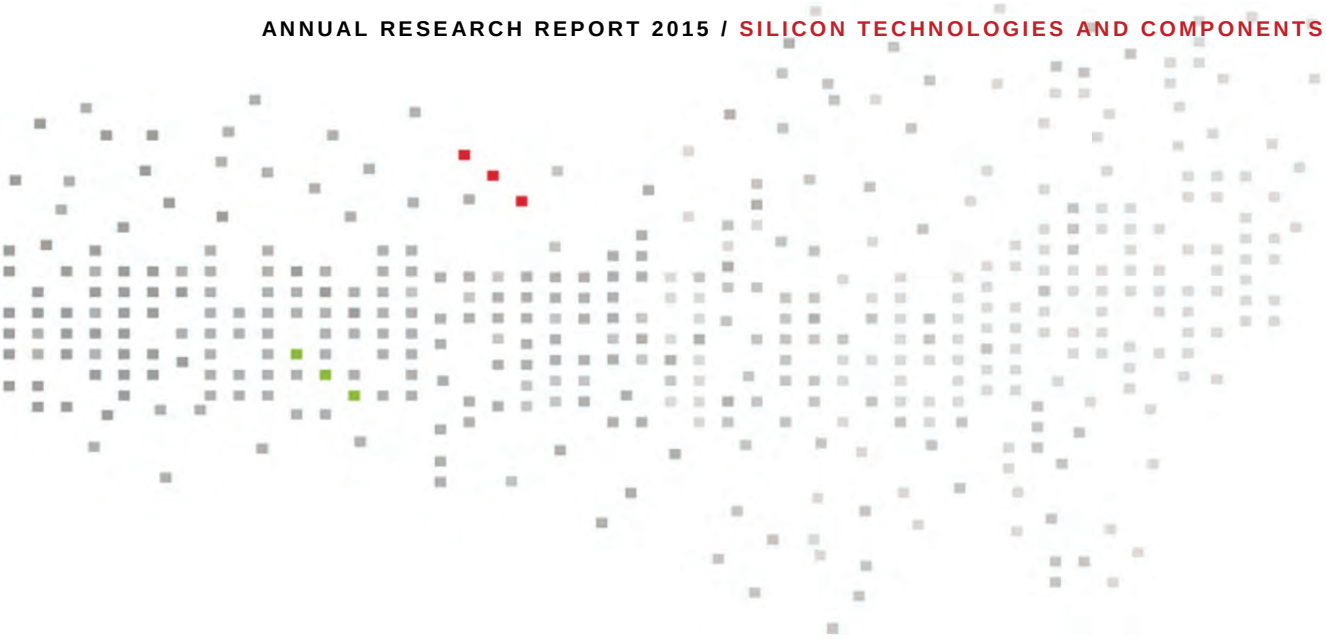


Within CEA Tech and Leti, silicon technologies and components research activities are shared between two divisions gathering together around 600 researchers:

The Silicon Technologies Division carries out innovative process engineering solution and research, operates 24/7 year round, 7,500m2 of state-of-the-art cleanroom space divided into three different technology platforms.

The Silicon Components Division carries out research on nanoelectronics and heterogeneous integration on silicon and is focusing on two mains areas: on-going shrinking of CMOS devices to extend Moore's Law for faster, less-expensive computing power, and the integration of new capabilities into CMOS, such as sensors, power devices, imaging technology, and new types of memory, to enable new applications.

This booklet contains 47 one-page research summaries covering advances in the focus areas of our Silicon Devices and Technologies Divisions, highlighting new results obtained during the year 2015.



Contents

Edito

Thomas ERNST
Chief Scientist

Dear Reader

We are proud to release our seventh Silicon Components and Technologies Annual Scientific Research Report, for the year 2015. This booklet contains 47 one-page research summaries covering advances in the focus areas of our Silicon Components and Technologies Divisions, highlighting new results during the year.

The year 2015 illustrates the strong diversification of nanotechnologies at Leti and in particular in our Si technologies departments for emerging applications such as the Internet of Things (IOT), automotive, energy and health monitoring.

In 2015, the Silicon Divisions produced 426 publications, including 109 in peer-reviewed journals, achieving impact factors as high as 31.

Our sensor research activities were established more than 25 years ago with a first startup creation in 1997. Since then, we have transferred several technologies to our startups or to established companies worldwide. The combination of new materials and architectures, and our vision ranging from emerging materials to systems enable us to propose competitive solutions for emerging applications. Our research on future IoT sensing systems includes embedded RF functionalities, dedicated packaging (especially for harsh environments), energy harvesters and micro-batteries.

We are also anticipating new paradigms in data treatments. Moore's Law will reach its end around 5 nm. However there is a strong need in the emerging "big data" society to make our systems more energy efficient by one order of magnitude or even more. Such breakthroughs should combine both hardware and software innovations. This trend is illustrated in this report by neuromorphic computing. Such research includes new materials (for resistive RAM), and 3D integrations. In our approach, those technological breakthroughs remain compatible with existing technologies. Thin films technologies such as FDSOI, nanowires and 2D materials are also a key element for future ultralow-power technologies.

New materials stimulate our innovation for growing domains, such as automotive, energy, data transfer… We also outline this year our results on GaN transistors on Si for power devices, GeSn laser, first 300 mm InGaAs-on-insulator substrates and innovative processes for 2D materials growth. Our divisions develop advance processes to pattern those materials at the nanoscale including DSA, nanoimprint and advanced maskless lithography.

We are very proud of our valuable collaborations with nearly all of French universities, CNRS laboratories and research institutes involved in nanotechnologies for electronics.

Our visibility and international recognition are made possible by our international collaborations including teams at Jülich (Germany), Tokyo Institute of Technology (Japan), Stanford (USA), Caltech (USA), the University of California (USA), University of Cambridge (GB), École Polytechnique Fédérale de Lausanne (Switzerland), CNR (Italy), Sherbrooke University (Canada) and Albany-Nanotech (USA); and by our participation in major international conferences through technical program committees, boards of governors and evaluation committees.

We thank all our industrial partners for their continuing confidence in us. We are committed to ensuring the transfer of our research to industry. Strong industrial partnerships are the foundation of our culture of innovation.

Underlying all these efforts is the cooperation of all our researchers and management, as well as the Silicon Technologies and Components Divisions and Leti's scientific advisory boards.

I wish to thank my predecessor Simon Deleonibus, now retired, for his continuous efforts to introduce new topics and ideas and encouraging researchers to explore new fields.

I also wish to extend my appreciation to the 10 chapter editors and authors of the 2015 Scientific Report, who spared no effort to prepare this document.

Thomas Ernst

Chief Scientist

Edito

Jean-René LEQUEPEYS

Head of Silicon Components Division

Dear Reader

Semiconductor industry growth is slowing and outlooks are mixed for the next few years, largely because of the fragile global economic outlook. This creates uncertainties about:

- Technology roadmaps: a co-existence between FDSOI and FinFET ? Which R&D strategy for 450mm ? What will be the impact of non-volatile memory emerging technologies ? When will a new era of computing based on neuromorphic or quantum electronics arrive?
- Collaborative models or alliances: increase in number of large mergers, growth of the Chinese ecosystem, IDMs refocusing on their core business ...
- Development of future markets: advanced driver assistance systems, Internet of Things, Big Data, High Performance Computing and servers, e-health ...

In this evolving context, our division reaffirms its world-leading position in nanoelectronics research, and it delivered again in 2015 cutting-edge technology solutions to its industrial partners. The following is a partial list of our major breakthroughs of the past year.

CMOS

- Leti helped STMicroelectronics extend its offer in 28nm FDSOI with a variety of key technology blocks, such as memories and RF, targeting Internet of Things applications.
- Leti assigned a team of experts to GLOBALFOUNDRIES' Fab 1 in Dresden to support ramp up of the 22FDX™ technology platform. As an ecosystem partner, Leti is also providing GLOBALFOUNDRIES' customers circuit-design IP, including its back bias feature for FDSOI, which enables exceptional performance at very low voltages with low leakage.
- EV Group (EVG) joined the 3D integration consortium of IRT Nanoelec, which is headed by Leti. EVG joins Leti, ST and Mentor Graphics to develop advanced 3D wafer-to-wafer bonding technologies. SET also joined the consortium this year.
- Leti is continuing its path finding solutions to future nanoelectronics technologies and systems; noteworthy results were achieved in quantum computing and neuromorphic architectures.

Power Electronics and Energy

- Major improvements have been made on our HEMT Normally-Off power transistors. Last year, our 200mm GaN-on-silicon technology convinced several industrial partners to commit to long-term partnerships with us.
- Our start-up Exagan raised €5.7 million to produce high-efficiency GaN-on-Silicon power-switching devices on 200mm wafers. This Leti and Soitec spinout is focusing on becoming a leading European source of GaN devices for solar, automotive, telecoms and infrastructure uses.
- CEA Tech and Fraunhofer ISE signed a collaboration agreement to create a common “virtual lab”. We will combine forces in “industry-like” research to further develop high efficiency multi-junction solar cells, educate young scientists and develop prototypes of next-generation ultra-high-efficiency solar cells.

Microsystems

- We manufactured micro-accelerometers on 300mm wafers, a first for the MEMS industry. This development could lead to significantly lower MEMS manufacturing costs.
- We provided support to our startup WAVELENS which is developing optical MEMS solutions aimed at improving camera image quality by making the integration of optical functions such as autofocus, image stabilization and zoom, easier.
- We demonstrated a NEMS-CMOS co-integration based on our CoolCube™ technology. Scaling down dimensions also scales down the amplitude of the signals and susceptibility to parasitics, in particular for resonant NEMS sensing. CMOS co-integration is the only viable solution to this complex addressing issue. Moreover, a vertical integration, as offered by CoolCube™, can be a competitive advantage for footprint reductions of MEMS sensors.

All these results were obtained due to the sustained efforts of our team, and I would like to sincerely thank them all. This report provides you with an overview of their achievements.

Jean-René LEQUEPEYS

Head of Silicon Components Division

Edito

Fabrice GEIGER

Head of Silicon Technologies Division

Dear Reader

The mission of our division is to provide our internal and external customers with the best innovative engineering solutions, so they can perform world-leading research on next-generation technology nodes. To achieve this, we provide 7,500m² of advanced research facilities, 3,000m² of nano characterization platform and the best human competencies.

In 2015, we invested €32.4M investment in new manufacturing equipment. This figure includes €7.9M dedicated to upgrading our installed base. Examples of tools put into production last year include a 300mm Applied Endura platform for PCRAM, an Applied Verity tool for high-volume metrology of logic and memory devices and a new LAM KIO FX etcher tool for tiny conductor and for III-V materials etching for photonics and a stepper CANON FPA 5510iZ for our 3D integration line.

This internal investment is complemented by a strong policy of collaboration with tool manufacturers. The idea is to build win-win partnerships. Leti takes advantage of innovative tools or materials to develop next-generation technologies. In return, our partners gain insight into the requirements needed for future market positioning.

We renewed four common labs in 2015:

- With EV Group (EVG): a new program in nano-imprint lithography (NIL) called INSPIRE to demonstrate the benefits of the versatile, powerful nano-patterning technology.
- With Aveni (former Alchimer) a project to develop their innovative approach to metallization for semiconductor, MEMS, advanced packaging and flex applications. Aveni's processes-Electrografting and Chemicalgrafting-rely on molecular engineering to grow metallization films molecule by molecule.
- With SPTS to develop disruptive 300mm HAR Cu-filling technology using CVD Cu-seed process in our 3D integration line.
- With Mapper Lithography to develop the ecosystem around multi-beam lithography. We installed the MATRIX pre-production equipment and were able to qualify this new and disruptive maskless technology.

We also strengthened and extended strategic partnerships with major manufacturing equipment suppliers as Applied Materials, LAM research, Tokyo Electron (TEL), Screen Semiconductor Solutions and FEI.

The year also was rich in scientific results for our division with a record number of more than 290 scientific papers published. The international recognition we received (seven distinctions and awards obtained in 2015) underscores the excellence of our teams and their accumulated skills and expertise. We have also generated 41 patents.

Our teams are focusing on key challenges around advanced CMOS, 3D, photonics and advanced memories. We are also addressing key 200mm challenges around MEMS, power electronics, RF, magnetic materials and other fields. Examples of our achievements include:

- Demonstration of a ultra-high vacuum direct bonding activated by ion beam. Examples of applications are heterogeneous integration (e.g. multi-junction solar cells based on III-V semiconductors), layer transfer for advanced substrates or high-vacuum encapsulation (MEMS).
- Development of an industrial CMP process for direct hybrid bonding and its application to 3D advanced imagers with direct assembly of Back Side Illuminated (BSI) wafers on the display processor. Direct hybrid bonding is quite promising for 3D industry because it enables very high interconnection densities compare to standard thermos-compression packaging technologies.
- Development of a methodology that allows a rapid evaluation of GaN-on-Si epitaxial wafers and does not involve any sample preparation. It enables our team to drastically lower the hole defect density, thus increasing the blocking voltage limit. As a consequence GaN power devices up to 12mm² (corresponding to devices capable of passing 90A) can be produced with no impact on the leakage current.

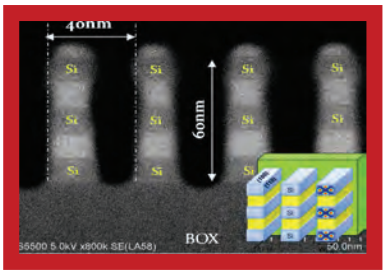
This scientific annual report includes additional details about all these key achievements, which were made possible by the work of our researchers and technicians. I would like to take this opportunity to thank all of them for their constant commitment.

Fabrice Geiger
Head of Silicon Technologies Division

Key figures

607 Permanent staff
220 Industrial residents
119 PhD students
22 Post-docs

200&300mm Platforms for CMOS and MEMS
7,500 m² Clean rooms
500 Process tools
Non-stop operation



121 Patents filed in 2015
426 Scientific papers produced

17 Common laboratories
7 Startups created since 2010

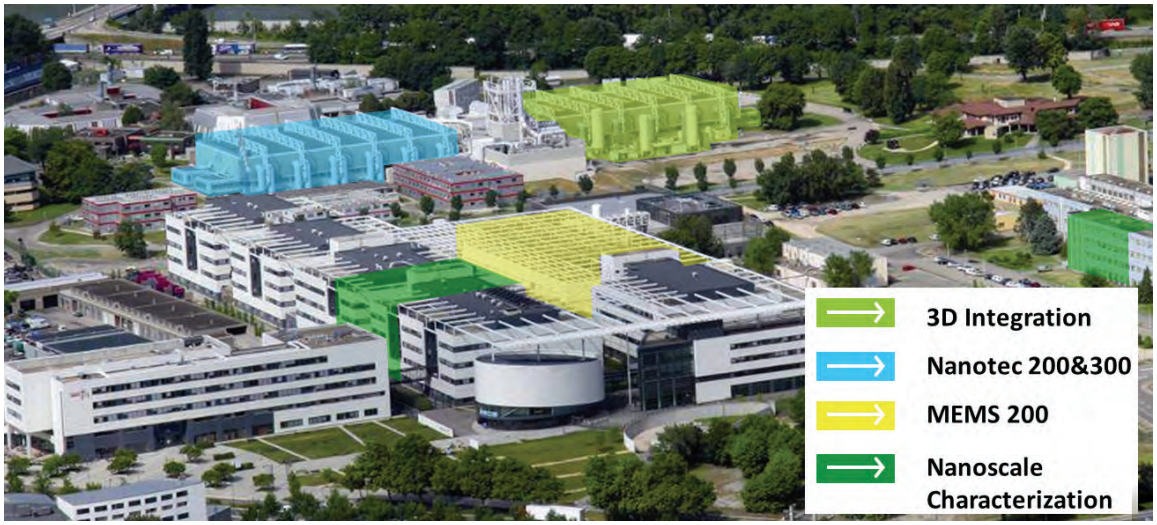
Technological Platforms

The silicon divisions operate 7,500m² of state-of-the-art cleanroom space divided into three platforms, gathering 500 process tools and a combined staff of more than 450; they run industry-like operations, 24 hours a day, 7 days a week, all year round.

- The Nanotech200&300 platform provides 200mm and 300mm CMOS wafer processing, which can be applied to both semiconductor and microsystem devices.
- The MEMS200 platform produces non-CMOS Micro-ElectroMechanical Systems (MEMS).

Both platforms are focused on the More than Moore initiative to develop new semiconductor capabilities. An innovative cleanroom shuttle system links the two platforms to add process flexibility and faster processing.

- The third platform 3D Integration aims to integrate various microelectronics objects together in order to juxtapose complementary functions, such as sensing, storing, processing, actuation, communication and energy scavenging. This provides advanced system solutions in three dimensions. This line is open to our customers for prototyping through the Open3D service.
- All research carried out in our cleanrooms benefits from the Nano-Characterization Platform, which is located on the MINATEC campus. This platform, unique in Europe, covers eight domains of competencies, including electron microscopy, X-ray diffraction, ion beam analysis, optics, magnetic resonance, scanning probe, surface analysis and sample preparation.



Organization

Silicon Technologies Division is organized according to six departments.

- Three Process Departments whose missions are to realize generic process steps for all projects and to develop innovative processes to provide state-of-the-art solutions to internal and external customers. Those departments are focused on patterning, deposition, and surface treatments. Their research activities in collaboration with key universities will support Leti's advanced position in the future.
- A Characterization Department whose mission is to perform off-line observations to characterize process steps, materials or components. This department also has a research activity to maintain its level of excellence.
- Two Support Departments: one is in charge of the planning, the interface with internal divisions or external customers as well as methods, training and clean-concepts. The other is responsible for facilities operations and engineering.

Silicon Components Division is organized around three departments with clear objectives and market focus.

- The MOS Department's mission is to simulate, model, develop, demonstrate and test new generations of circuits and modules for sub-20nm CMOS, digital and memory.
- The MEMS Department designs and develops innovative microsystem components (sensors, actuators and RF) and the associated toolbox (packaging, heterogeneous integration, reliability).
- The Power and Energy Department develops and demonstrates technology modules and components for power and energy (photovoltaic, power electronics, integrated storage).

Scientific Activity

Publications

- In 2015: 426 publications produced
- Ratio “A grade published items/ Publishing researchers”> 1.00 (including grade A conferences, journals and international extended patents)

Distinctions and Awards

- 8 distinctions and awards received in 2015
  - Young Scientist Award –E-MRS 2015, L. Bonnet
  - Young Scientist Award –E-MRS 2015, D. Ouhab
  - Best Video Clip Award –Bronze Medal -JSIAM 2015, L. Bonnet
  - Prix IEEE EDS Paul Rappaport 2015, V. Delaye, D. Lafond, J.-M. Hartmann
  - Young Scientist Award –M&M 2015, R. Estiville
  - Best Paper Award -IWJT 2015, E. Ghegin
  - Prix NanoArt2015, V. Gorbenko, T. Printemps
  - Best student paper SISC 2015, Julien Borrel
- 84 additionnal awards including the 2005 Grand Prix Académie des Technologies, 2008 IEEE Cledo Brunetti Award, 2011 French-German Prize for Economy, 2011 Silver Medal STMicroelectronics, 2012 SEE Grand Prix du Général Ferrié, 3 ERC grants, 49 Best Papers Awards

Expertise and Recognitions

- 97 Leti experts: 4 Research Directors, 7 International Experts
- 25 researchers with habilitation qualification “HDR” (to independently supervise doctoral candidates)
- 1 IEEE Fellow, 3 IEEE Seniors

Scientific Committees

- 3 journal editors: IEEE TED, European Physical Journal-Applied Physics, Science China-Information Sciences
- 7 researchers involved in ITRS (International Technology Roadmap for Semiconductors)
- 40 members of Technical Programs and Steering Committees at major conferences: IEDM, VLSI Technology Symposium, IRPS, ESSDERC, SSDM, ECTC, ECS…
- Awards committees: IEEE Cledo Brunetti Award, IEEE Paul Rappaport Award, SEE & IEEE Brillouin-Glavieux Award, European Research Council Panel
- Boards of Governors: IEEE ED Society, Nanosciences Foundation Board, IEEE CPMT, SFV IEEE ED Society Region 8 Vice-Chair

International Collaborations

Collaborations with more than 50 universities and institutes worldwide : Tokyo Institute of Technology (Japan), CALTECH (USA), University of Stanford (USA), University of Berkeley (USA), University of Cambridge (GB), University of Tokyo (Japan), EPFL (Switzerland), Albany-NT (USA), …

01

CORE & BEYOND CMOS

- 14nm FDSOI Technology for Energy Efficient CMOS
- Innovative Strain Techniques for CMOS Performance Boosting
- From Mismatch to Process Variations - A Unified CAD-Compatible Model of Statistically Correlated Variability
- Tungsten and Copper Interconnection Stability for 3D VLSI CoolCube™ Integration
- Nanowire MOSFET for 5nm Node and Beyond

14nm FDSOI Technology for Energy Efficient CMOS

Research topics: CMOS, SOI

O. Weber, J. Mazurier, P. Perreau, F. Andrieu

Partnership: STMicroelectronics
Sponsorship: NANO 2017, ENIAC-Places2Be

Context

As CMOS technology scales down, two paths are pursued by the industry to overcome the fundamental limits of traditional planar bulk transistors. One is the introduction of a Tri-Gate or FinFET transistor at the 22 and 16-14 nm nodes. These architectures provide impressive drive currents per footprint at low supply voltages because of the 3-D conduction channel and excellent electrostatic control. Conversely, they have high gate and parasitic capacitances, proportional to the 3-D effective W increase, which negatively impacts both the speed and active power consumption. Alternatively FDSOI provides an evolutionary path. First introduced at the 28nm node, FDSOI includes excellent mismatch properties, a simplified planar manufacturing process vs 3-D finFET technology and capitalization of existing design techniques. It also extends the possibility of back biasing and therefore offers unique "smart" solutions for dynamic power optimization. The technology reported here furthers the appeal of FDSOI to the 14nm node [1].

Process Technology

Table 1 highlights key 14nm FDSOI design rules and technology features. A 0.55x area scaling with respect to the 28nm FDSOI technology was achieved with the introduction of local interconnect and the adoption of fixed layout shapes (or "constructs"). Compared to the 28nm technology, new front-end process elements include a dual SOI/SiGeOI N/P channel, a dual workfunction gate-first HKMG integration scheme and a dual in-situ doped Si:CP/SiGeB N/P raised source-drain (Fig.1). Additionally, and for the first time, a SiBCN low-k material spacer was integrated in a gate-first flow for minimizing the gate-to-drain parasitic capacitance [1].

Key features	28FDSOI	14FDSOI
Min Contacted gate pitch CPP	114nm	90nm
M1 pitch	90nm	64nm
Std cell area	1X	0.55X
VT flavours	RVT / LVT	LVT / SLVT
Lgate in min CPP	24nm → 30nm	20nm → 34nm
Channel	SOI 7nm	Dual SOI/SiGeOI 6nm
Buried oxide	BOX 25nm	BOX 20nm
Gate	HKMG single metal	HKMG dual WF
Source-Drain	Single Si epi + I/I	Dual epi SiGeB/Si:CP

Table 1: Key 14FDSOI ground rules and technology features.

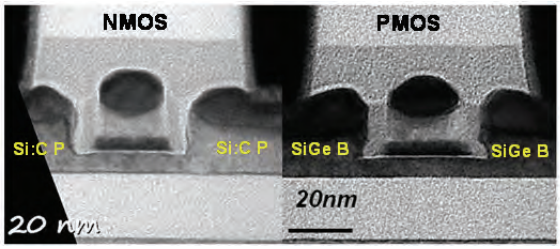


Figure 1: N&PMOS transistor TEM cross-sections in 14nm FDSOI.

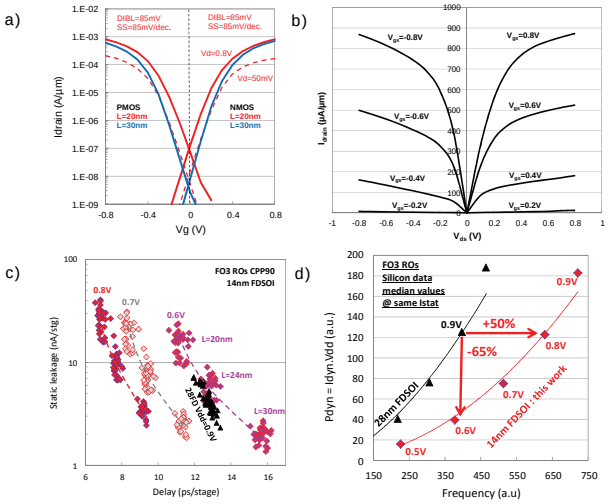


Figure 2: (a) $I_d(V_g)$ for N&PMOS transistors at L=20nm and 30nm, V_{dd}=0.8V, (b) $I_d(V_d)$ for N&PMOS transistors at L=20nm and Vdd=0.8V, (c) 14nm FDSOI Delay/Istat for FO3 ring oscillators vs 28nm FDSOI, (d) 14nm FDSOI Frequency/Pdyn vs 28nm FDSOI.

Performance & Power

I_d-V_g plots at V_{dd}=0.8V show DIBL of 85mV and a sub-threshold slope of 85mV/dec. for both NMOS and PMOS at L_{nom}=20nm (Fig.2a). I_{dsat}=880µA/µm at I_{off}=100nA/µm and V_{dd}=0.8V were achieved at L_{nom}=20nm/W_{nom}=0.17µm for both NMOS and PMOS (Fig.2b). As a result, 14nm FDSOI devices running at V_{dd}=0.6V are as fast as 28nm FDSOI devices running at V_{dd}=0.9V (Fig.2c). At the same operation frequency and at same static leakage, 14nm FDSOI provides 65% power saving over the 28FDSOI technology (Fig.2d) [1].

In addition, FDSOI offers a unique opportunity for energy efficient product design in its extended capability of back biasing. Fig.3a shows that devices running at V_{dd}~0.63V with a 2V forward back bias (FBB) are as fast as devices running at V_{dd}=0.8V with no back bias, reflecting a 40% dynamic power saving at same speed. Of course, because FBB is associated with V_t lowering, static leakage strongly increases at the same time, as shown in Fig.3b. But, with this flexibility offered by the large back bias capability, FDSOI appears as a powerful technology to find the right performance at the right power and at the right leakage for each application product.

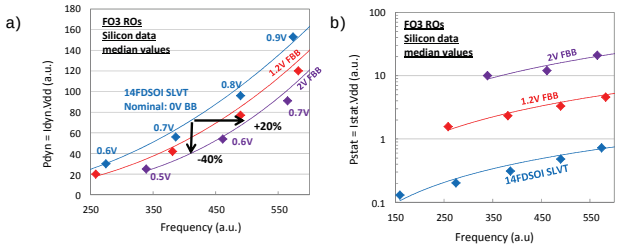


Figure 3: Freq/Pdyn (a) and Freq/Pstat (b) with forward back bias application.

Related Publications
[1] O. Weber *et al.*, "14nm FDSOI Upgraded Device Performance for Ultra-Low Voltage Operation", *VLSI Technology Symposium, 2015.*
[2] O. Weber *et al.,* (invited) "Static and Dynamic Power Management in 14nm FDSOI Technology", *ICICDT conference, 2015.*
[3] O. Weber *et al.,* (invited) "14nm FDSOI Technology for High-Speed and Energy-Efficient CMOS", *ECS transactions 2015 - issue 20.*

Innovative Strain Techniques for CMOS Performance Boosting

Research topics: Strain, Stress, CMOS, Si, SiGe, SOI, sSOI, BOX Creep, STRASS

C. Le Royer, S. Reboh, Y. Morand (STM), A. Bonnevialle (STM), D. Rouchon, P. Gergaud, C. Plantier, J.-M. Hartmann, O. Rozeau, S. Maitrejean, B. de Salvo

Partnership: STMicroelectronics
Sponsorship: IRT Nanoelec., ECSEL-WayToGoFAST

Context and Challenges

Innovative performance boosters (mainly strain boosters) are mandatory to improve Fully-Depleted SOI devices performance and power efficiency. Channel strain is an effective way to enhance electrons and holes mobility: compressive SiGe for pFETs and tensile Si for nFETs. The interest of using Smart Cut™ sSOI substrates (for nFETs), SiGe channels/Raised Sources and Drains (for pFETs) as strain boosters has successfully been demonstrated on FDSOI architecture.
Since 2013 we investigate new strain techniques [4] such as "STRASS" (Fig.1.i) [1,2] and "BOX creep" (Fig.1.ii) [3] in order to obtain tensile stress (for nFETs) and compressive stress (for pFETs).

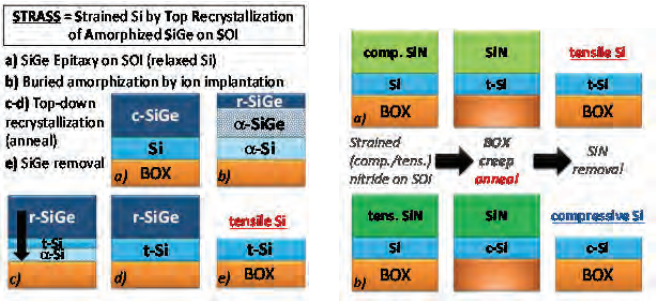


Figure 1: i) Schematics of the STRASS process to fabricate tensile Si on insulator. ii) Principle of the BOX creep technique applied to the fabrication of a) tensile Si and b) compressive Si, depending on the sacrificial SiN stress.

Main Results

STRASS for tensile Si [1]: We propose here another approach (Fig.1.i) to create sSOI structures starting from SOI ones by transfer of lattice parameter from a relaxed $Si_{0.7}Ge_{0.3}$ to the Si layer. The process is divided in four steps: i) a $Si_{0.7}Ge_{0.3}$ epitaxy of 40 nm on SOI with 9 nm thickness Si; ii) an amorphization by Si implantation at 25 keV with 2.5 x 10^{14} at/cm² (tilt 0°) of the Si layer and the lower portion of the SiGe layer; iii) a recrystallization by thermal annealing at 850 °C, 10 s under N2 atmosphere, and; iv) SiGe selective etching using HCl. The stress induced in the Si thin film is memorized turning the initial SOI into sSOI. According to Raman spectroscopy, the 9 nm Si layer exhibits a large tensile stress (+1.6 GPa), which is expected to lead to a +60% in electron mobility (at 1MV/cm electric field).

BOX creep for compressive Si (or SiGe) [3]: We demonstrate in 2015 the fabrication of localized tensily strained Si-On-Insulator (sSOI) using a method named BOX creep process. This technique is based on the creep of the Buried OXide (BOX) and consists in the stress transfer from a top sacrificial (compressive) SiN layer into the thin Silicon layer during a high temperature anneal (Fig.1.ii.a). Strain and stress were determined using Raman spectroscopy. Using a compressive SiN on SOI (14 nm Si / 145 nm BOX), we turned relaxed Si into tensile Si with +1.2 GPa stress.

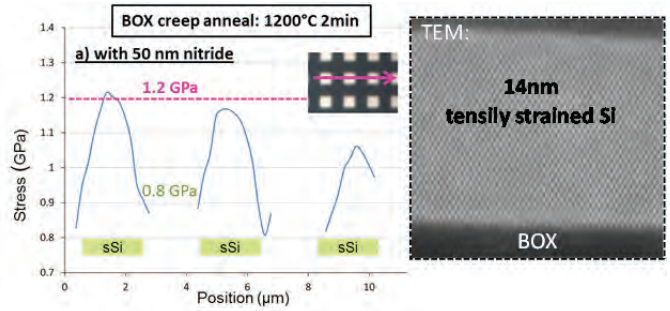


Figure 2 : Left) Stress profiles from scanning Raman extractions for 2x2µm² SOI structures after BOX creep process. Right) Corresponding cross-sectional HAADF STEM micrograph of the sSi film.

We have also investigated the crystalline quality and the top Si roughness of the fabricated sSOI MESAs. The cross sectional STEM micrograph (Fig.2.ii) of the Si layer after BOX creep process confirms the good crystallinity of silicon: no defects are observed in the field. All the AFM mapping measurements confirm the absence of impact of this technique on the Si roughness.

Perspectives

After the morphological studies which enabled to confirm the strain efficiency of these techniques, we are currently investigated the integration of STRASS and BOX creep modules in a state-of-the-art FDSOI CMOS route. The goal of these electrical demonstrations is to obtain significant boost in the electrical performance of the fabricated devices and circuits. Moreover we will be able to optimize process conditions and to tackle the potential design issues related to STRASS and BOX creep.

Related Publications
[1] A. Bonnevialle, S. Reboh L. Grenouillet, C. Le Royer, Y. Morand, S. Maitrejean, J.-M. Hartmann, A. Halimaoui, D. Rouchon, C. Plantier, M. Vinet, "Top Recrystallization of Partially Amorphized SiGe on SOI for sSOI Fabrication", *2015 MRS Spring Meeting & Exhibit*, April 6-10, 2015, San Francisco, California.
[2] S. Maitrejean, N. Loubet, E. Augendre, P. F. Morin, S. Reboh, N. Bernier, R. Wacquez, B. Lherron, A. Bonnevialle *et al.*, "A New Method to Induce Tensile Stress in Silicon on Insulator Substrate: From Material Analysis to Device Demonstration," *ECS Trans.*, vol. 66, no. 4, pp. 47-56, Mar. 2015.
[3] A. Bonnevialle, C. Le Royer, Y. Morand, S. Reboh, J.-M. Pédini, A. Roule, D. Marseilhan, P. Besson, D. Rouchon, N. Bernier, C. Tabone, C. Plantier, M. Vinet, "A New Method to Induce Local Tensile Strain in SOI Wafers: First Strain Results of the "BOX Creep" Technique", Proc. of *SSDM 2015*, Japan.
[4] A. Idrissi-El Oudrhiri, S. Martinie, J-C. Barbé, O. Rozeau, C. Le Royer, M-A. Jaud, J. Lacord, N. Bernier, Y. Morand, L. Grenouillet, P. Rivallin, *et al.*, "Mechanical Simulation of Stress Engineering Solutions in Highly Strained p-type FDSOI MOSFETs for 14-nm Node and beyond", *2015 SISPAD*, pp. 206-209.

From Mismatch to Process Variations
A Unified CAD-Compatible Model of Statistically Correlated Variability

Research topics: Mismatch, Across-Chip Variations, Process Variations, Variability Modeling, SPICE

T. Poiroux, P. Scheer (STM), A. Juge (STM), M. Vinet

Partnership : STMicroelectronics
Sponsorship: ENIAC-Places2Be

Context and Challenges

As downscaling of CMOS technologies is pursued, transistor variability remains a critical challenge for digital and analog applications. Therefore, proper compact modeling of the effect of process variations, from local to global scale, on nanoscaled transistors is crucial for computer-aided design (CAD). Today, CAD models of statistical variability are based on Pelgrom's approach, in which two separated components are described: local mismatch sources, featuring extremely small correlation lengths, and large scale process variations, with correlation lengths larger than die size. An extensive literature exists on causes of deviation from this approach. In particular, some variability sources, such as line-edge / line-width roughness (LER/LWR), require CAD-compatible models able to deal with correlation lengths comparable to device size and to distance between devices. By generalizing Pelgrom's approach to variability sources with arbitrary correlation length, we have developed a simple CAD model that unifies all cases, from local to large-scale variations, in a single formulation.

Main Results

Considering a given process parameter p as variability source, we assume that device characteristics are impacted by the average $\bar{p}$ of this process parameter over the device area (or over the transistor width if LER is considered), as done in Pelgrom's approach. Without doing any assumption about the process parameter autocovariance function, except that it is monotonically decreasing as the position shift is increased, process parameter power spectral density (PSD) (or, equivalently, autocovariance function) can be decomposed as a sum of centered normal functions. Each of these normal components of the PSD contributes independently (i.e. in an uncorrelated way) to the mismatch induced by process parameter variations. Then, for each normal component, an exact expression of the autocovariance function of the averaged process parameter $\bar{p}$ can be calculated as a function device dimensions (D_x, D_y), distance between device centers (P_x, P_y) and PSD component correlation length $(\Lambda_{xi}, \Lambda_{yi})$:

$$\Gamma_{\bar{p}-\langle p\rangle,i}(P_x,P_y)=\frac{\alpha_i\Lambda_{xi}\Lambda_{yi}}{4{D_x}^2{D_y}^2}\times\left(\theta\left(\frac{P_x+D_x}{\Lambda_{xi}}\right)-2\theta\left(\frac{P_x}{\Lambda_{xi}}\right)+\theta\left(\frac{P_x-D_x}{\Lambda_{xi}}\right)\right)\times\left(\theta\left(\frac{P_y+D_y}{\Lambda_{yi}}\right)-2\theta\left(\frac{P_y}{\Lambda_{yi}}\right)+\theta\left(\frac{P_y-D_y}{\Lambda_{yi}}\right)\right)$$

with θ(u) the primitive integral of error function erf(u):

$$\theta(u)=u\times erf(u)+e^{-u^2}/\sqrt{\pi}$$

From this exact calculation of $\bar{p}$ autocovariance function, we can obtain simple expressions of the variance of device pair mismatch in asymptotic cases of correlation lengths. These asymptotic expressions are summarized in table below.

	$\Lambda_{yi} \ll D_y$	$D_y \ll \Lambda_{yi}$
$\Lambda_{xi} \ll D_x (< P_x)$	$\frac{2\alpha_i}{D_x D_y}$	$\frac{2\alpha_i}{D_x(\sqrt{\pi}\Lambda_{yi})}$
$D_x \ll \Lambda_{xi} \ll P_x$	$\frac{2\alpha_i}{(\sqrt{\pi}\Lambda_{xi})D_y}$	$\frac{2\alpha_i}{(\sqrt{\pi}\Lambda_{xi})(\sqrt{\pi}\Lambda_{yi})}$
$(D_x <) P_x \ll \Lambda_{xi}$	$\frac{2\alpha_i}{(\sqrt{\pi}\Lambda_{xi})D_y}\left(\frac{P_x}{\Lambda_{xi}}\right)^2$	$\frac{2\alpha_i}{(\sqrt{\pi}\Lambda_{xi})(\sqrt{\pi}\Lambda_{yi})}\left(\frac{P_x}{\Lambda_{xi}}\right)^2$

Figure 1:Asymptotic expressions of the variance of mismatch between two identical devices of size (D_x, D_y), separated by a center-to-center distance P_x for a normal component of process parameter of amplitude α_i and correlation lengths $(\Lambda_{xi}, \Lambda_{yi})$.

Based on this analysis and on asymptotic expressions summarized in previous table, we have developed a simple analytical model compatible with implementation in conventional CAD flow for Monte-Carlo simulations. For each independent normal component of the process parameter PSD, this model provides very simple, although very accurate, expressions for single device variance ${\sigma_{\bar{p},i}}^2$ and for correlation coefficient between devices ρ_i:

$${\sigma_{\bar{p},i}}^2 \approx \frac{\sqrt{\alpha_i}}{\sqrt{{D_x}^2+\pi{\Lambda_{xi}}^2}}\frac{\sqrt{\alpha_i}}{\sqrt{{D_y}^2+\pi{\Lambda_{yi}}^2}}$$

$$\rho_i \approx e^{-\pi{P_x}^2/({D_x}^2+\pi{\Lambda_{xi}}^2)}e^{-\pi{P_y}^2/({D_y}^2+\pi{\Lambda_{yi}}^2)}$$

Thanks to the normal form of the correlation coefficient, this model can be implemented in conventional CAD environment quite easily. The only requirement is to get device absolute positions (referenced to arbitrary origin) as instance parameters. Then, thanks to the use of these device positions in well-chosen trigonometric expressions, the expected mismatch results, including cases of multifinger transistors, can be obtained from usual Monte-Carlo simulations.

Perspectives

This approach unifies local mismatch and statistically correlated process variation descriptions in a single formulation, and provides a way to deal with multi-scale variability sources, including sources with significant component at correlation lengths comparable to device dimensions. Therefore, it can be used to describe correctly the effect of pure local mismatch source, large scale process variations, as well as all intermediate cases of variability sources with correlation lengths of the order of magnitude of device dimensions and distance between devices. In particular, this model provides an essential correction to be brought to initial Pelgrom's approach for LER/LWR variability.

Related Publications
[1] T. Poiroux, P. Scheer, A. Juge, M. Vinet, "Multiscale statistically correlated variability: A unified model for Computer-Aided Design", *IEEE Transactions on Electron Devices*, Vol. 62, pp. 3605-3612, 2015.
[2] A. Juge *et al.*, "Variability at all levels – a challenge for the semiconductor industry", *ESSDERC Workshop on Variability*, Sept. 2015.

Tungsten and Copper Interconnection Stability for 3D VLSI CoolCube™ Integration

Research topics: CMOS, SOI, 3D Sequential, Interconnection

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Partnership: STMicroelectronics, IBM, Qualcomm
Sponsorship: NANO 2017, EQUIPEX FDSOI11

Context and Challenges

An alternative approach to conventional device scaling for future nodes is the 3DVLSI or sequential 3D integration [1]. Compared to TSV-based 3D ICs, CoolCube™ process flow offers the possibility to stack devices with a lithographic alignment precision (few nm) enabling ultra-high via density. To benefit from the full 3D opportunities and avoid global routing congestion [2], there is a need to implement local routing of the bottom tier: inter-tier metal layers need to be incorporated in the technology (Fig.1). As a consequence, Back End Of Lines (BEOL) levels need to support top FET thermal budgets. A reasonable maximum thermal budget for top FET has been determined around 500°C implying to find solutions for implementing back end material stable beyond 400°C. Currently the combination of copper (Cu) with ULK (Ultra Low-K) materials is widely used for standard BEOL (low resistivity & capacitance, and thus speed improvement). However the integration of such materials in the intermetal levels of a CoolCube™ integration faces a number of challenges. Indeed Cu metallization can cause contamination issues in the case of wafer break during the process of the top transistor where FEOL contamination environment is required. Despite the fact that its intrinsic resistance is larger, a solution can be the use of tungsten (W) as it has already been integrated in the FEOL of several products.

Main Results

In order to highlight the interest of W interconnections for 3D CoolCube™ integration, we have used the standard 28nm design rules damascene BEOL integration of the state of the art FDSOI technology.

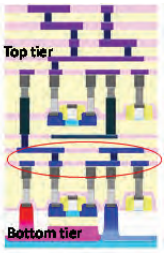

Figure 1: 3D VLSI structure with 2 levels of inter-tiers interconnections.

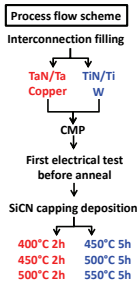

Figure 2: Process flow scheme for BEOL M1 stack and list of annealings applied on Cu or W lines.

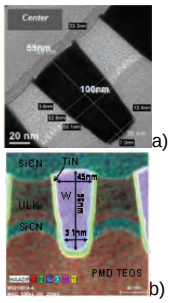

Figure 3: Metal 1 TEM cross sections filled with a) Cu and b) W before annealings.

The ULK material is a porous PECVD SiOCH with a k value of around 2.7. For both Cu and W interconnects, only metal 1 (M1) level is integrated. After the TaN/Ta/Copper or TiN/Ti/W filling, the CMP planarization is realized and a SiCN layer of 20nm is deposited as a capping layer during post-annealings.

The different annealings tested on the M1 interconnect are summarized in Fig.2. Fig.3 shows TEM cross sections of the W (bottom) and Cu (upper) interconnections before anneal.

Fig.4 shows the M1 line resistance measured on a specific multi-fingers/serpentine test structure for Copper and W interconnections before annealing. As expected, the W resistance is a factor 6 higher than the copper one for quasi-similar capacitance values. Finally, the median value of the W line resistance has been extracted and highlights no modification up to 500°C 2h annealing confirming the good thermal W stability (Fig.5). Similar results are obtained for the Cu intercos submitted to post thermal anneals (Fig.6).

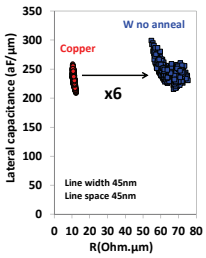

Figure 4: Comparison of Cu and W M1 intercos before annealings for a line width and space of 45nm.

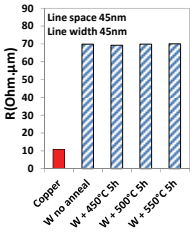

Figure 5: W resistance evolution before and after annealings. Cu resistance (no anneal) as reference.

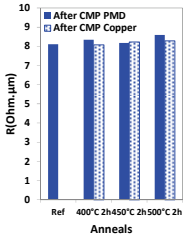

Figure 6: Cu M1 line resistance versus post thermal anneallings.

Thanks to morphological and electrical characterization for a 28nm design rules technology, Cu and W interconnections stability is highlighted up to 500°C 2h and 550°C 5h respectively [3]. Regarding dielectric, a slight performance degradation has been evidenced by our study, it was unexpected for ULK film if we refer to literature data. Regarding metals, no performance degradation was observed. Therefore this study should be completed by investigation of the reliability of the dielectric and of the integrated W and Cu interconnects.

Perspectives

In order to tackle the W BEOL metallization resistance penalty as compared to copper and to improve the capacitance stability, some alternative materials are under study. For example lower resistivity metal material coupled with SiO_2 or non-porous low-k materials could be envisaged to push forward the top tier thermal treatment limitation.

Related Publications
[1] P. Batude *et al*, "3DVLSI with CoolCube process: An alternative path to scaling", *2015 Symposium on VLSI Technology*, June 16-19, 2015, Kyoto, Japan.
[2] O. Billoint *et al*, "A Comprehensive Study of Monolithic 3D Cell on Cell Design Using Commercial 2D Tool", *Design, Automation and Test in Europe (DATE 2015)*, March 9-13, 2015, Grenoble, France.
[3] C. Fenouillet-Beranger *et al*, *International Conference on Solid State Devices and Materials (SSDM 2015)*, Sept. 27-30, 2015, Sapporo, Japan.

Nanowire MOSFET for 5nm Node and Beyond

Research topics: CMOS, SOI, Nanowire, Advanced Patterning

S. Barraud, V. Lapras, L. Gaben, M.P. Samson (STM), M. Cassé, J.M. Hartmann, C. Vizioz, C. Arvet (STM), P. Pimenta-Barros, V. Loup, F. Glowacki, V. Maffini-Alvaro, L. Grenouillet, Y. Morand (STM), N. Bernier, O. Rozeau, M.A. Jaud, S. Martinie, J. Laccord, M. Vinet

Partnership: STMicroelectronics, IBM, SOITEC
Sponsorship: NANO 2017, EQUIPEX FDSOI11

Context and Challenges

For many years, semiconductor nanowires (NWs) have offered the prospect of enabling the next generation of MOSFET devices for digital circuits. These 1D nanostructures, with optimal electrostatic confinement and consequently significant short-channel effect benefits, are often considered as the "ultimate CMOS devices". If promising preliminary developments have been carried out in order to establish a NW-based CMOS technology platform, many open questions still remain in order to address the 5nm node and beyond. During this year the "NW team" focused its work on electronic transport properties (impact of NW size and substrate orientation) in NWs, the benchmarking of stacked-NWs with FinFET, and the main challenges for the fabrication of stacked-GAA NWs.

Main Results

For 5nm node and beyond, NW-based transistors are today considered as a credible alternative to FinFET (FF) technology. However, it still remains unclear if, using the same technology constraints as for FinFET, stacked-NW devices are actually able to overcome FF performances in advanced CMOS technologies. To find answers, 3D TCAD simulations have been performed in order to benchmark the performances of stacked-NWs with FinFET and to define guidelines for 5nm node. The results of TCAD simulation allow us to know the NW dimensions (width and height) required to overcome FinFET performances for a given footprint (Fig.1). The comparison is done by assuming the same space between Fin or stack (W_S) and the same total thickness (H_{tot}). Operating voltage was V_{DD}=0.7V and the gate length has been fixed at L_G=16nm. In both cases, the use of wide NWs leads to increase the effective width (W_{eff}) as compared to FF which is a key element for improving performances. Similarly to FF, the stacked-GAA NWs configuration shows a DIBL~60mV/V but with higher W_{eff}.

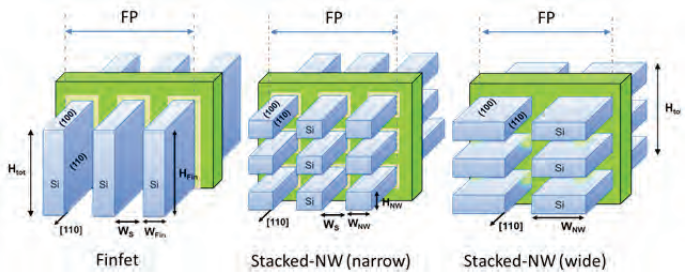

Figure 1: Schematics of FinFET, narrow stacked-GAA nanowires and wide stacked-GAA nanowires (also named "nanosheets").

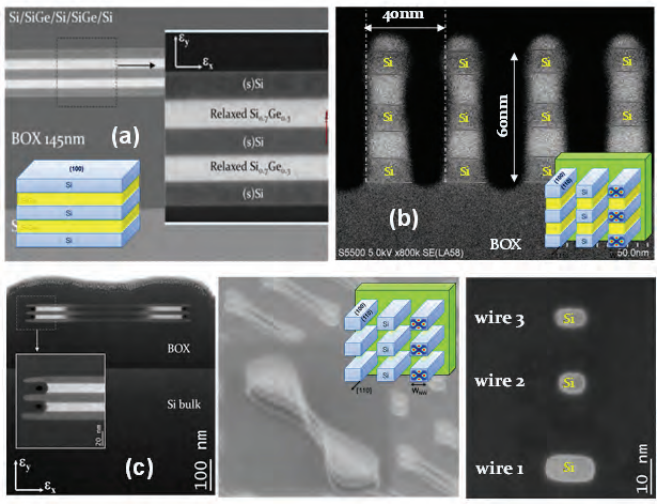

Figure 2: (a) (SiGe/Si) superlattice epitaxial growth, (b) Fin patterning by SIT (FP=40nm), (c) Selective etching of SiGe versus Si in order to release Si NWs, (d) Cross-sectional TEM image of 3D stacked-NWs.

It was shown that a significant delay reduction (>20%) can be obtained by using stacked-GAA NW technology (also named "nanosheets") for wide (>20nm) and thin NWs (T_{Si}=7nm). The delay reduction is explained by their increased effective width and limited parasitic capacitances within a given footprint.

After this first study on the design of stacked-NWs, the main challenges for the fabrication of stacked-NWs have been addressed. A replacement metal gate (RMG) integration scheme has been developed for stacked-NWs on SOI substrates including the following process steps (Fig.2); (i) an epitaxial growth of $(Si/SiGe)_{xN}$ superlattice with strained-Si channel for NFET and compressive SiGe channel for PFET, (ii) advanced patterning (Sidewall-Image-Transfer technique) for the definition of $(Si/SiGe)_{xN}$ Fins (Fin width=17nm with a 40nm Fin pitch), (iii) an inner spacers module in order to reduce the parasitic capacitances and (iv) the selective etching of SiGe (versus Si) to preserve Si channels after the dummy gate removal.

Perspectives

The perspective of this work is to develop dual-channel CMOS co-integration with Si NFET and strained-SiGe PFET in stacked-GAA nanowire device architectures.

Related Publications

[1] L. Gaben, S. Barraud, M.-A. Jaud, S. Martinie, O. Rozeau, J. Lacord, G. Hiblot, S. Monfray, F. Bœuf, T. Skotnicki, F. Balestra, M. Vinet, "Stacked-NW and FinFET transistors: guidelines for the 7nm node", *International conference on Solid State Devices and Materials (SSDM 2015)*, Sept. 27-30, 2015, Sapporo, Japan.

[2] L. Gaben, S. Barraud, P. Pimenta-Barros, Y. Morand, J. Pradelles, M.-P. Samson, B. Previtali, P. Besson, F. Allain, S. Monfray, F. Bœuf, T. Skotnicki, F. Balestra, M. Vinet, "Ω-Gate NW transistors realized by sidewall image transfer patterning: 35nm channel pitch and opportunities for stacked-NWs architectures", *International conference on Solid State Devices and Materials (SSDM 2015)*, Sept. 27-30, 2015, Sapporo, Japan.

02
MEMORIES

- Impact of MOX/Al2O3 CBRAM Bilayer Structure on Window Margin and Memory Reliability for NVM Applications
- Operation Fundamentals in 12Mb Phase Change Memory Based on Innovative Ge-rich GST Materials Featuring High Reliability Performance
- The Physical Mechanisms Involved in Resistive Memories Clarified by Advanced Studies on the Structure of Amorphous Chalcogenides
- Potentialities of Vertical Resistive RAM (VRRAM) for Neuromorphic Applications

Impact of MOX/Al_2O_3 CBRAM Bilayer Structure on Window Margin and Memory Reliability for NVM Applications

Research topics: CBRAM, NV Memory, Metal-Oxide, Bilayer, Embedded Applications

M. Barci, G. Molas A. Toffoli, M. Bernard, A. Roule, C. Cagli, E. Vianello, B. De Salvo, L. Perniola

Sponsorship: ENIAC-PANACHE

Context and Challenges

Conductive Bridge RAM (CBRAM) is presented as a promising candidate to replace the Flash memory due to CMOS compatibility, high operational speed at low voltages, low operating current and good thermal stability. Its basic working principle relies on the formation and dissolution of a conductive filament in a resistive layer sandwiched between electrochemically reactive and inert electrodes. High temperature stability [1,2], large window margin and good endurance are required for advanced non-volatile memory applications. In this work, we propose an optimized Al_2O_3 0.5nm/MO_X 4nm bilayer oxide-based CBRAM [3] in order to improve the memory performances (memory window, thermal stability and endurance).

Main Results

In Fig.1 (left) are presented typical IV characteristics of monolayer (a) and bilayer (b) CBRAM devices. Forming voltage of bilayer is almost 1V bigger than monolayer. In Fig.1 (right) R_{OFF} evolution is shown as the bit line ($|V_{BL\text{-}RESET}|$) voltage is increased for different SET conditions (in terms of V_{WL}, $V_{BL\text{-}SET}$ and P_W). Between each RESET operation, the CBRAM is set back to the ON state. As V_{RESET} is increased, RESET saturates for monolayer and R_{OFF} reaches a limit of ~ 2.10^5 Ω. On the contrary, for the bilayer, R_{OFF} continues to increase and 10^6 Ω can be attained at $V_{BL\text{-}RESET}$=2.2V. In other words, despite a slower initial RESET process in double layers (lower RESET speed), a higher R_{OFF} can be reached due to a higher R_{OFF} after saturation.

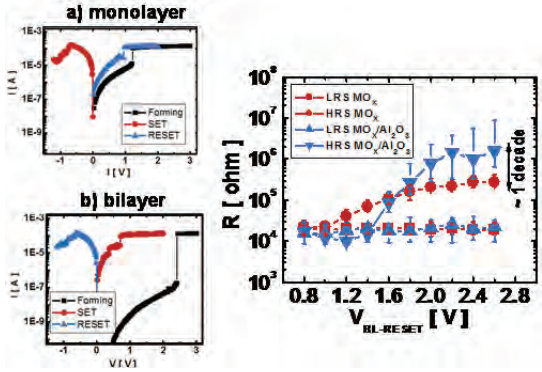

Figure 1: (left) Typical IV characteristics for mono and bilayer CBRAM devices. (right) R_{OFF} as a function of RESET |VBL| voltage (1µs pulses) for the studied samples. R_{ON} between each RESET cycle is also represented.

Fig.2 (left) presents the retention behavior of the monolayer and bilayer structures at 200°C at 250°C for 24 hours. We can observe that the window margin gain obtained with bilayers remains stable over time, highlighting the good thermal stability of this technology. In Fig.2 (right) are presented the endurance characteristics of monolayer and bilayers. In the case of bilayer Al_2O_3/MO_X, a clear improvement is demonstrated, with 10^5 cycles maintaining constant a window margin of 1 decade.

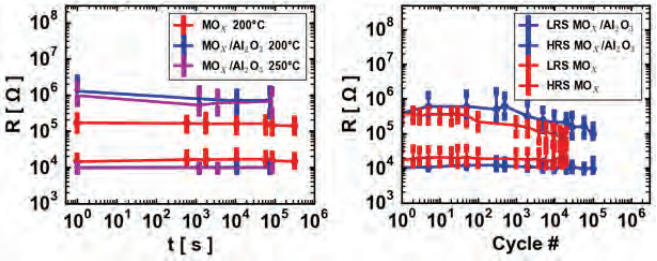

Figure 2: (left) Data retention behavior of monolayer and bilayer devices up to 250°C/24hrs. (right) Endurance behavior for monolayer (red) and bilayer (blue) devices up to 10^5 cycles.

In Fig.3, based on the TAT model, we estimated the trap and Cu contributions to the R_{OFF} drift by comparing the R_{OFF} values after cycling with and without final smart RESET (progressive increase of $V_{BL\text{-}RESET}$ until R_{target} is reached). Al_2O_3/MO_X bilayer reduces the generated trap density of 50% compared to the monolayer reference, explaining the improved reliability performances.

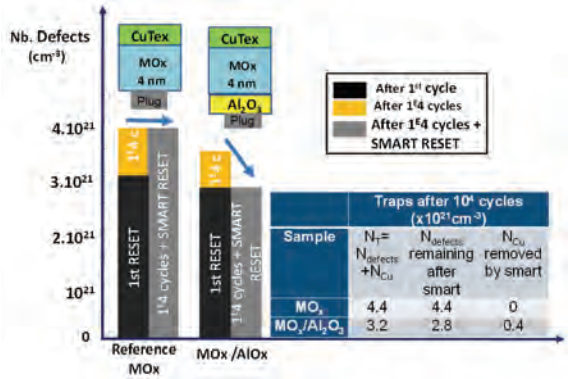

Figure 3: Slopes (v_{ON} and v_{OFF}) of LRS (square) and HRS (circle) as a function of the I_{SET} used to set the initial R_{ON} during retention at 130°C. Endurance behavior for monolayer (red) and bilayer (blue) devices up to 10^5 cycles.

Perspectives

Bilayer Cu-based/MO_X/Al_2O_3/metal plug CBRAM devices show improved reliability performances in terms of retention (250°C/24hrs) and endurance behavior (~1 decade at 10^5 cycles), confirming to be a promising technology for potential future high density memory applications.

Related Publications

[1] M. Barci, J. Guy, G. Molas, E. Vianello, A. Toffoli, J. Cluzel, A. Roule, M. Bernard, C. Sabbione, L. Perniola B. De Salvo, "Impact of SET and RESET conditions on CBRAM high temperature data retention", *2014 IEEE International Reliability Physics Symposium*, pp. 5E-3, 2014.
[2] G. Molas, E. Vianello, F. Dahmani, M. Barci, P. Blaise, J. Guy, A. Toffoli, M. Bernard, A. Roule, F. Pierre, C. Licitra, B. De Salvo, L. Perniola, "Controlling oxygen vacancies in doped oxide based CBRAM for improved memory performances", *2014 IEEE International Electron Devices Meeting*, pp. 6-1, 2014.
[3] M. Barci, G. Molas, A. Toffoli, M. Bernard, A. Roule, C. Cagli, J. Cluzel, E. Vianello, B. De Salvo, L. Perniola, "Bilayer Metal-Oxide CBRAM Technology for Improved Window Margin and Reliability", *2015 IEEE International Memory Workshop (IMW)*, pp. 1-4, 2015.

Operation Fundamentals in 12Mb Phase Change Memory Based on Innovative Ge-rich GST Materials Featuring High Reliability Performance

Research topics: Phase Change Memories, High Temperature Data Retention, Phase Field Modeling

V. Sousa, O. Cueto, G. Navarro, N. Castellani, M. Coué, V. Delaye, C. Sabbione, P. Noé, F. Fillot, L. Perniola, S. Blonkowski, P. Zuliani, R. Annunziata

Partnership: STMicroelectronics
Sponsorship: ENIAC-PANACHE

Context and Challenges

Phase-Change Memories (PCM) are today considered the most mature among novel non-volatile memory technologies. Recent results have highlighted an optimized Ge-rich GeSbTe (GST) phase change material, which is able to guarantee code integrity after soldering thermal profile and data retention in extended temperature range. Our work presents the performances of ±2at% Ge concentration around the optimized material when integrated on a 12Mbits test vehicle [1]. In order to simulate the electro-thermal characteristics of our devices and to reproduce the phase change mechanisms of the PCM material during the set and reset operations, we have developed a finite element electro-thermal solver coupled with the Phase Field Method [2]. The confrontation of the experimental observations to the simulation results allowed us to achieve the understanding of the origin of the high thermal stability of the two programmed states.

Main Results

In our study, the Ge-rich GST phase change materials have been fabricated by magnetron sputtering and integrated in state-of-the-art PCM devices. The SET/RESET distributions of the 12Mb test vehicle (Fig.1) show that the reading window is preserved after a 2h bake at 230°C for all the evaluated Ge contents in the range of ±2at% from the optimized alloy, thus illustrating the high thermal stability of the programed states and the large process window of the material.

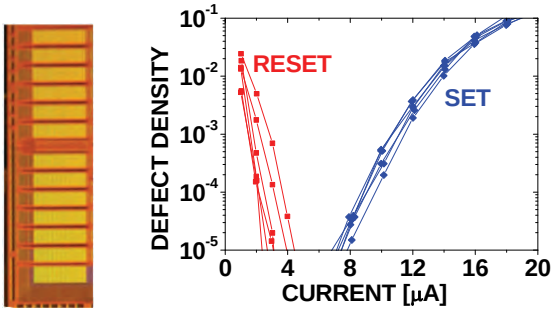

Figure 1: Micrograph of the 12Mbits test vehicle and SET/RESET distributions after a 2h bake at 230°C for Ge-rich GST alloys with Ge variations of ±2at% wrt the optimized alloy, demonstrating the large process window.

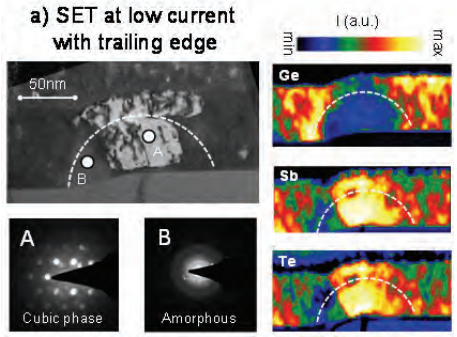

Figure 2: Superimposition of the BF/DF images and STEM/EELS signal for the SET states of GST+Ge45% devices programmed at low current : a crystalline column of single orientation is formed across the active area while the elemental distribution reveal the depletion in Germanium at the core of the cell.

The composition analysis performed by EELS at the core of the storage element (Fig.2) shows how the initially high Ge content allows retaining a Ge-rich alloy at the core of the cell, although a strong segregation effect tends to expel Ge out of the active area, thus explaining the high thermal stability of the RESET state wrt crystallization. The peculiar grain structure imaged by TEM allows us to correlate the low drift of the SET state operated at low current with the low number of amorphous-like grain boundaries standing along the conduction path. The simulation results obtained thanks to the phase field method (Fig.3) show how this crystalline structure is the result of the growth of the top crystal grain during programming.

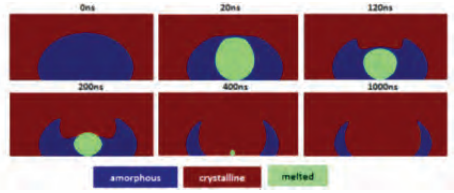

Figure 3: Simulation using the phase field method of the phase change during the SET operation at low current.

Perspectives

The introduction of the multi-phase field method in the simulation tool will enable to give account not only for the phase change during programming, but also for the evolution of the grain structure and the elemental segregation.

Related Publications
[1] V. Sousa, G. Navarro, N. Castellani, M. Coué, O. Cueto, C. Sabbione, P. Noé, L. Perniola, S. Blonkowski, P. Zuliani, R. Annunziata, "Operation Fundamentals in 12Mb Phase Change Memory Based on Innovative Ge-rich GST Materials Featuring High Reliability Performance", *Proceedings of the VLSI conference* (2015).
[2] O. Cueto, V. Sousa, G. Navarro and S. Blonkowski, "Coupling the Phase-Field Method with an Electrothermal Solver to Simulate Phase Change Mechanisms in PCRAM Cell", *Proceedings of the SISPAD conference* (2015).

The Physical Mechanisms Involved in Resistive Memories Clarified by Advanced Studies on the Structure of Amorphous Chalcogenides

Research topics: Chalcogenide, ReRAM, PCRAM, CBRAM, Amorphous Structure

P. Noé, E. Souchier, C. Sabbione, M. Bernard, V. Jousseaume, P. Blaise, N. Castellani, G. Veux, G. Navarro, V. Sousa, F. Hippert (LNCMI), F. D'Acapito (CNR)

Partnership: CRG Beamline LISA/CNR-IOM-OGG c/o ESRF, CNRS-LNCMI
Sponsorship: ANR-SESAME, ENIAC-PANACHE

Context and Challenges

Chalcogenide-based resistive random access memories (mainly Phase Change and Conductive Bridging RAM) are considered as the most promising emerging technologies for the next generation of non-volatile memory. Both of these memories involves a chalcogenide compound which can be electrically switched between two reversible and distinct resistance states. In PCRAM, a Te-based phase-change alloy is reversibly switched electrically between its amorphous and crystalline states which present a very high contrast in resistivity. Whereas, in CBRAM devices, it is supposed that ions are produced at an electrochemically active anode and migrate in the chalcognenide electrolyte to form a conducting path under the influence of an electric field. This process is reversible by applying an opposite bias. However, such technologies have to face major technological challenges that have prevented or delayed up to now their successful transfer to industry.

Resistance drift phenomenon in PCRAM

One of the main challenge for PCRAM technologies concerns the so-called resistance drift phenomenon. The drift is characterized by a spectacular increase of the resistance with ageing of the amorphous (a-) phase of the phase-change chalcogenide alloy. It is commonly attributed to a structural relaxation, the nature of which remains unknown, and has until now hindered the development of ultra-high multilevel storage devices with multi-level cell operation (MLC).

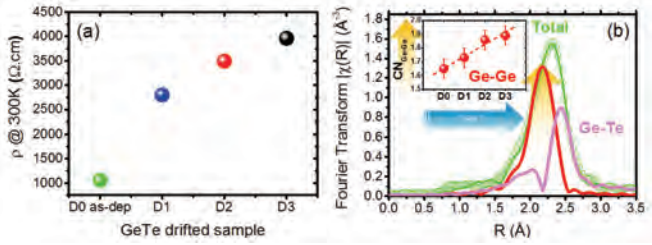

Figure 1: (a) Resistivity ρ measured at 300 K on a prototypical a-GeTe sample in as-deposited (D0) state and set at different ageing and resistance drift levels (D1, D2 and D3). (b) Fourier transform (squares) with best fit curve (continuous lines) of the EXAFS spectrum of sample D0 showing partial contribution of Ge–Ge and Ge–Te bonds. The insert is a plot of the change in Ge–Ge coordination number deduced from analysis of EXAFS data of D0 to D3 samples showing the increase in Ge-Ge homopolars bonds with drift.

In that context, we experimentally evidenced for the first time a direct structural change with resistance drift in prototypical a-GeTe thin film by grazing incidence x-ray absorption spectroscopy (GIXAS) [1]. Different pieces of the a-GeTe film were set at different resistance drift levels by thermal annealing prior to the XAS experiment at the Ge K-edge (Fig.1(a)(b)(c)). In all samples, Ge–Ge and Ge–Te bonds coexist (Fig.1(d)). Nevertheless, this study demonstrates that the drift phenomenon is concomitant to a clear change in the local Ge environment: the number of Ge–Ge homopolar bonds increases as the resistance increases (Fig.1(d)), which is contrary to current theoretical predictions in the literature.

This effect could be related to a decrease of defect states and increase of trap states in the band gap, induced by the structural changes, leading to a progressive increase in resistivity of the amorphous semiconductor. In any case, the impact of the observed structural changes will have to be taken into account in models in order to definitively conclude on the origin of drift phenomenon and are of major importance in designing phase change materials that exhibit very low resistance drift in the amorphous phase in order to develop MLC PCRAM.

Resistive switching mechanism of CBRAM

The major limitation of CBRAM is related to the poor stability of the conductive filament in the amorphous chalcogenide highlighting the lack of understanding of the switching mechanism at the nanoscale level preventing thus successful transfer to industry.

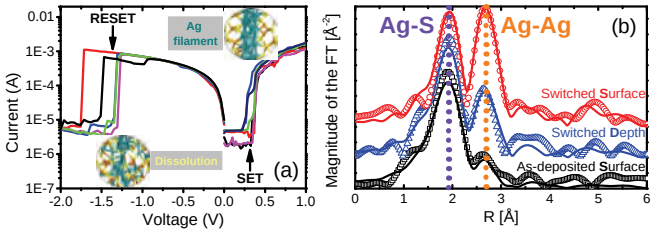

Figure 2: (a) Typical I(V) curves of a CBRAM device to be analyzed by XAS during cycles of SET and RESET between the low and high resistive states. The inserts are the schematic drawing of a silver nano-filament in GeSx and the silver filament dissolution scheme. (b) Fourier Transforms of EXAFS spectra at Ag K-edge of 3 prototypical samples (switched CBRAM using surface and depth collection mode and a non-switched CBRAM on the surface) with the best fit curves (continuous lines). The vertical arrows mark the features that grow with increasing Ag–metal content.

Our approach was based on CBRAM devices specifically designed in order to be finely characterized depending on their resistive states by means of depth-selective X-ray absorption spectroscopy (XAS) [2]. The Ag/GeSx/W CBRAM devices are analyzed using depth selective X-ray Absorption Spectroscopy before and after switching. Fig.1(a) illustrates the typical I(V) curves obtained and the reversible switching from the high to the low resistive state (SET and RESET, respectively). The study of the local environment around Ag atoms in such devices reveals that Ag is in two very distinct environments with short Ag–S bonds due to Ag dissolved in the GeSx matrix, and longer Ag–Ag bonds related to an Ag metallic phase. These experiments allow the conclusion that the switching process involves the formation of metallic Ag nano-filaments initiated at the Ag electrode. All these experimental features are well supported by *ab initio* molecular dynamics simulations showing that Ag favorably bonds to S atoms, and permit the proposal of a model at the microscopic level that can explain the instability of the conductive state due to progressive sulfidation of metallic Ag in these Ag–GeSx CBRAM devices. Finally, the principle of the nondestructive method described here can be extended to other types of resistive memory concepts.

Related Publications
[1] P. Noé, C.Sabbione, N. Castellani, G. Veux, G.Navarro, V. Sousa, F. Hippert and F. d'Acapito, "*Structural change with the resistance drift phenomenon in amorphous GeTe phase change materials' thin films*", *J. Phys. D: Appl. Phys*. 49, 035305 (2016).
[2] E. Souchier, F. d'Acapito, P. Noé, P. Blaise, M. Bernard and V. Jousseaume, "*The role of the local chemical environment of Ag on the resistive switching mechanism of conductive bridging random access memories*", *Phys. Chem. Chem. Phys*. 17, 23931 (2015).

Potentialities of Vertical Resistive RAM (VRRAM) for Neuromorphic Applications

Research topics: OxRAM based VRRAM for Neuromorphic

Authors: G. Piccolboni, G. Molas, J. M. Portal, R. Coquand, M. Bocquet, D. Garbin, E. Vianello, C. Carabasse, V. Delaye, C. Pellissier, T. Magis, C. Cagli, M. Gely, O. Cueto, D. Deleruyelle, G. Ghibaudo, B. De Salvo, L. Perniola

Sponsorship: ENIAC-PANACHE

Context and Challenges

Combining Resistive RAM concept with Vertical NAND technology and design, Vertical RRAM (VRRAM) was recently proposed as a cost-effective and extensible technology for future mass data storage applications. 3D RRAM based neural networks were also proposed to emulate the potentiation and depression of a synapse, but more complex circuits were not discussed. In previous works [3-4], various RRAM based neuromorphic circuits were proposed and investigated, using planar devices.

Main Results

Vertical RRAM were fabricated (Fig.1) and investigated obtaining promising results (20ns switching time, up to 10^7 cycles and stable 200°C retention). VRRAM was then proposed as a solution to increase the density of neuromorphic circuits thanks to the staking of memory cells and the reduced use of transistors. 1TnR pillars are proposed to emulate synapses (Fig.2). For cochlea application [3,4], good agreement with planar binary OXRAM configuration with random generator is obtained (Fig.3), with an area gain of more than a factor 3. Resistance correlation between adjacent cycles improves the reliability for neuromorphic applications requiring low endurance performances. Thus, for convolutional neural network, 10-15 RRAM levels are sufficient to reach a recognition rate of more than 98%. VRRAM based synapses open the path to high-density neuromorphic circuits requiring aggressive synaptic levels.

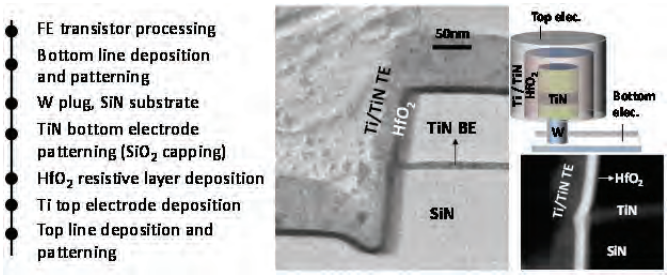

Figure 1: Description of the integration flow, and TEM cross sections (high resolution and dark field) of the TiN/HfO2/Ti/TiN VRRAM.

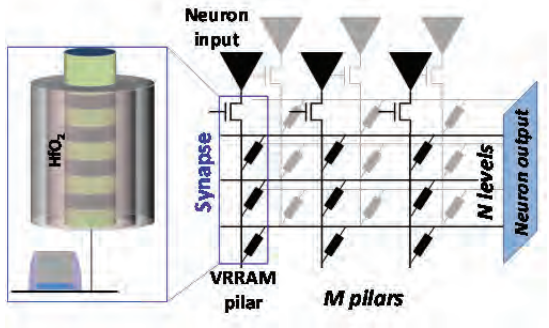

Figure 2: Simulated neuromorphic network. A synapse is composed by N VRRAM cells in a pillar addressed in parallel. The output neuron collects the contributions of all synapses.

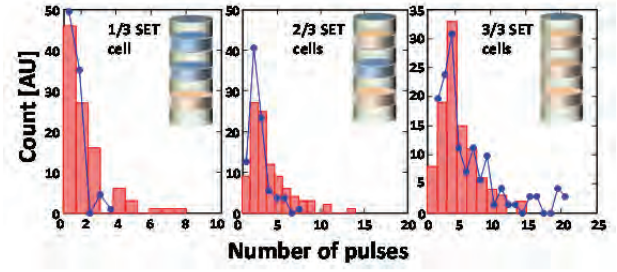

Figure 3: Cochlea application: circuit simulated with synapses composed of 3 stacked VVRAM. SET conditions are fixed to target 20% of occurrence probability (fig. 19). Distributions of required # of pulses to SET respectively 1, 2 or 3 cells per pillar are represented and compared with a theoretical case.

Perspectives

The following step in the process/integration is to perform electrical characterization on 2-level VRRAM, comparing the 2 levels. Concerning the design a more detail study is needed to properly dimension all the circuital components in order to verify the limitations (max number of levels, etc.) for our neuromorphic solution.

Related Publications

[1] G. Piccolboni *et al.*, "Investigation of the Potentialities of Vertical Resistive RAM (VRRAM) for Neuromorphic Applications", *IEDM Tech. Digest, 2015.*.
[2] G. Piccolboni *et al.*, "Investigation of HfO2/Ti based vertical RRAM - Performances and variability", *2014 NVMTS Tech. Dig.* pp.1-5.
[3] M. Suri *et al.*, "CBRAM devices as binary synapses for low-power stochastic neuromorphic systems: auditory (cochlea) and visual (retina) cognitive processing applications", *IEDM 2012 Tech. Dig.*, pp.235-238.
[4] D. Garbin *et al.*, "Variability-tolerant Convolutional Neural Network for Pattern Recognition Applications based on OxRAM Synapses", *IEDM Tech. Dig.*, 2014.

03

PATTERNING

- Mask-Less Lithography for Advanced CMOS Technology
- NanoImprint Lithography Industrial Platform Assessment within INSPIRE
- DSA Integration Challenges for Contact Hole & Via Patterning
- Computational Aspects of Lithography
- Advanced Patterning of Stacked Nanowires Transistor

Mask-Less Lithography for Advanced CMOS Technology

Research topics: Advanced Lithography, Data Preparation, Lithography Process, Resist Outgassing

L. Lattard, S. Berard Bergery, Y. Blancquaert, B. Dalzotto, L. Dubus, K. Lepinay, M.L. Pourteau, J. Pradelles, G. Rademaker, I. Servin

Partnership : MAPPER Lithography, TSMC, STMicroelectronics, NISSAN Chemical, ASELTA Nanographics, Mentor Graphics, SOKUDO, TEL, Nova
Sponsorship: IMAGINE Program

Context and Challenges

With the recurrent introduction delay of EUV lithography for High Volume Manufacturing and its constant increasing cost of ownership, mask less lithography (MLL) remains a credible alternative to answer to CMOS manufacturing industry expectations thanks to its cost attractiveness, its intrinsic resolution capability and the high-throughput of the massively parallel writing concept. Since 2009, Leti launched the collaborative program "IMAGINE" to push the insertion of the Mask Less Lithography approach developed by MAPPER lithography (Netherlands).
After technology demonstration achieved on pre-alpha tool in Leti, Mapper lithography introduced a new pre-production 300mm technological platform compatible with CMOS 28/20/14 nm technologies. Mapper and Let are now working together for qualification of this new platform.

Main Results

Several new part of the electronic optic were installed in the tool FLX-1200 at Leti. Please refer to Fig.1.
A new version of the so-called Individual Beam Corrector which allow to align individually the 1300 beams. On Fig.2 alignment results are plotted and we were able to demonstrate that 97% of the beams are in specification for alignment of the optical column [1].

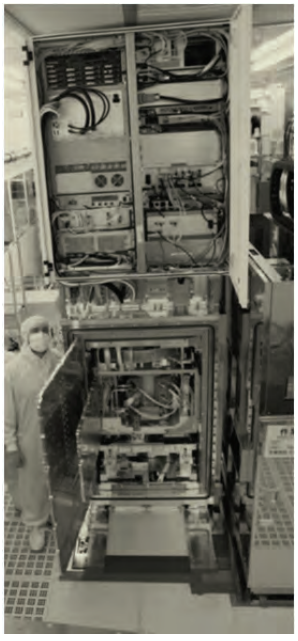

Figure 1: Picture of the complete electronic optic of the FLX-1200 tool.

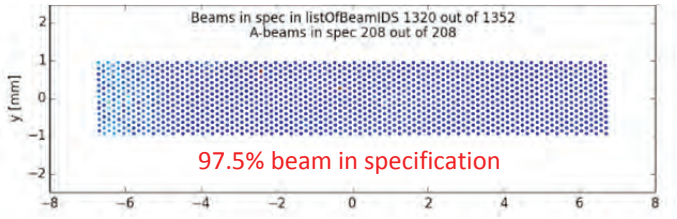

Figure 2: Results of the alignment off all 1352beams inside Electronic optic.

Our greatest achievements in 2015 are the demonstration of a CDU for one beam over a complete 300mm wafer of 2nm (3 sigma) in agreement with the requirement of semiconductor industry for a 28nm technology node with measurement on a 42nm Half Pitch features [2].

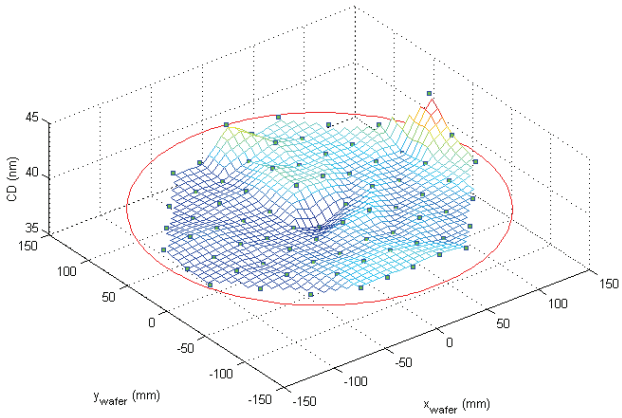

Figure 3: Picture of the Critical Dimension Uniformity on 300mm wafer.

Perspectives

The main 2016 objectives is the qualification of the blanker module which is now in qualification at Mapper Lithography (Netherlands). This blanker module is the cornerstone for Direct Writing lithography tool. This will allow all types of printing features with upload of the design files directing on the wafer thanks the blanker module.

Related Publications
[1] J. Pradelles, J. Reche, Y. Blancquaert, C. Constancias, L. Lattard, N. Vergeer, Y. Ma, P. Wiedemann, G. de Boer, M. Wieland, "Multiple e-beam direct write enters pre-production mode", *Proc. SPIE*, 2015.
[2] G. De Boer, M.P. Dansberg, R. Jager, J.J.M. Peijster, E. Slot, S.W.H.K. Steenbrink, L. Lattard , L. Pain, M.J. Wieland, "Performance validation of MAPPER's FLX-1200", *9423-34, Proc. SPIE*, 2015.

NanoImprint Lithography Industrial Platform assessment within INSPIRE

Research topic: Nano Imprint Lithography, INSPIRE

H. Teyssedre, M. Louro, S. Landis

Partnership: EVG

Context and Challenges

Nanoimprint techniques stick out from other more conventional lithography processes because of the fundamental mechanism of creating the structures. In classical approaches, they are created through a chemical contrast. In the case of NanoImprint, the contrast is topographic and the flow of the resist through the stamp's cavities shapes the pattern. As during the last decades, significant efforts have been made to overcome the contact between the photomask and the resist coated wafer (to limit defectivity and enhance the resolution), NIL technology appeared to be for many years an UFO, since the process is based on the intimate contact between the working stamp and the resist to be embossed.

In twenty years, consequent technical developments have been achieved to make the technology more mature and ready for high volume manufacturing. Even a plenty of technology alternatives were proposed, the UV based imprint, using transparent stamp, became the standard technology. Two well established options are now available on the market: the full wafer imprint (the size of the stamp correspond to the size of the wafer to be printed) and the step and flash imprint were a small stamp (i.e. die size) is stepped like in optical lithography across the wafer to be processed.

If the step and flash technology is more prone to address the semiconductor markets (NAND Flash memory, DRAM and logic) with high requirement levels for alignment capability and defectivity density, the full wafer option seems to be the reference for the emerging and growing markets like LED and Photonics based devices [1]. The wafer scale imprint solution, much cheaper than the step and flash option, however still lacks from quantitative data regarding technology assessment for high volume manufacturing. Commercially available equipment and resist are cornerstones of this technology, however some blocs of a full supply chain (design rules, master manufacturing and repair, in line metrology, integration solutions) need to be established and qualified to make the technology mature enough to rapidly meet market's needs.

Main Results

To accelerate this technology adoption Leti and EV Group launched a new program [2] called INSPIRE (see Fig.1) to demonstrate the benefits of NIL technology and spread its use for applications beyond semiconductors. Much more than an industrial partnership, the INSPIRE program is designed to demonstrate the technology's cost-of-ownership benefits for a wide range of application domains, by supporting the development of new applications from the feasibility-study stage to the first manufacturing steps and transferring integrated process solutions to their industrial partners, thus significantly lowering the entry barrier for adoption of NIL for manufacturing novel products.

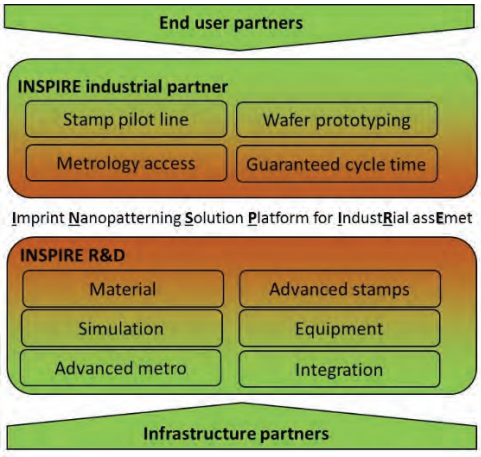

Figure 1: INSPIRE program organization and philosophy.

This program focused first on Critical Dimension uniformity (see Fig.2) as well as defectivity assessments onto 200 mm wafers printed with the smart NIL© technology available in the HERCULES® NIL equipment platform. The work brings focus on sub micrometer resolution features fully covering 200 mm silicon master. Repeatability tests were performed over more than 100 printed wafers to collect statistics within a wafer and also wafer to wafer.

Perspectives

Further technology assessments are already planned within the INSPIRE project. They will help us to propose new development to make the technology more mature and to qualify this solution with respect to customers' needs already involved in the project.

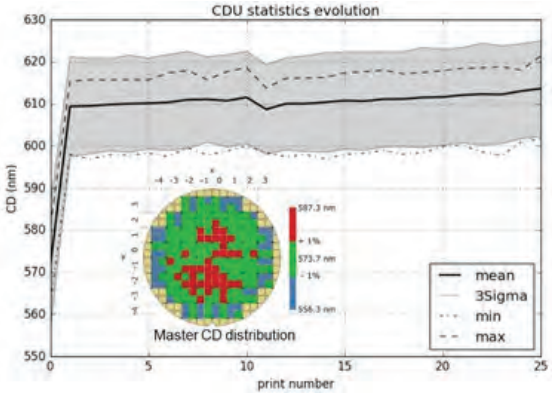

Figure 2: CD-SEM characterization of the feature size distribution 25 200 mm wafers printed with the smart NIL© technology available in the HERCULES® NIL equipment platform. The value are measured over 208 sites on each wafer.

Related Publications
[1] L. Pain, R. Tiron, L. Lattard, S. Landis, C. Laviron, "Lithography alternatives: Why are they essential?", *Solid State Technology*, September 2015.
[2] S. Landis, H. Teyssedre, L. Pain, "NIL for industrial early adopters, INSPIRE project", *NIL Industrial Day* Berlin 2015.

DSA Integration Challenges for Contact Hole & Via Patterning

Research topics: Advanced Lithography, Directed Self-Assembly, Block-Copolymers, DSA planarization

R. Tiron, A. Gharbi, M. Argoud, P. Pimenta-Barros, I. Servin, G. Chamiot-Maitral, A. Sarrazin, C. Lapeyre, S. Bos, S. Bouanani[2], X. Chevalier[1], C. Nicolet[1], C. Navarro[1]

Partnership: ARKEMA[1], STMicroelectronics[2], SOKUDO, TEL
Sponsorship: ARKEMA, STMicroelectronics, FP7-COLISA, ENIAC-PLACYD

Context and Challenges

Directed-self-assembly (DSA) of block copolymers (BCPs) is still one of the most promising solution for advanced patterning in sub-10nm technology nodes. For its high resolution capability, cost effectiveness and process compatibility, DSA continues to attract the semiconductor industry. Nevertheless, some challenges need to be addressed before the final insertion of DSA into an industrial production flow. By this way, Leti and Arkema are working together in the frame of a multi-partnership program named IDeAL.

Main Results

Since the commonly-used graphoepitaxy process in DSA is shown to be dependent on the pattern density which is a showstopper for DSA integration, Leti has recently developed and patented a new process flow called *DSA planarization*, fully integrated on the 300mm pilot line [1-4]. This new approach is based on the overfilling of the pre-pattern cavities with high BCP film thickness followed by a plasma etch-back step. It allows us to ensure a uniform control of the BCP thickness, inside guiding cavities, through different opening densities. Thus, defect-free isolated and dense patterns for both contact shrink and multiplication (doubling and more) are performed on the same processed wafer.

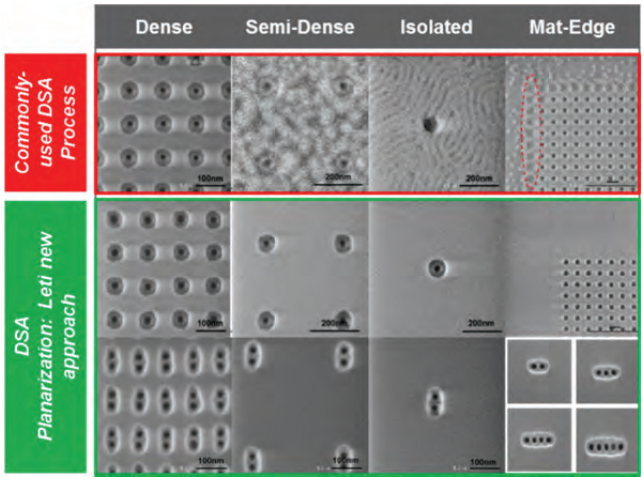

Figure 1: DSA planarization process overcoming the pattern density dependence issue: a full control of BCP thickness over pitch on the same processed wafer.

In addition, the control of the pre-pattern surface chemical affinity seems to be a key to improve DSA performances. By using grafted brush layers, it is found that lower defectivity level can be achieved which leads to overcome potential transfer etching issues and avoid final circuit-yield drop [5]. CD uniformity and placement error are also enhanced as shown in Fig.2.

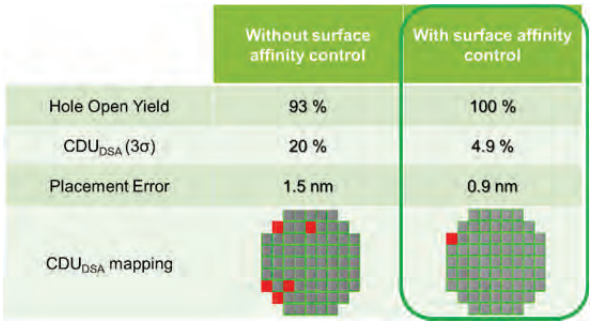

Figure 2: Influence of surface affinity on key manufacturing-process parameters.

As 3D BCP morphology is key parameter for DSA process control, advanced characterization (SEM cross section, AFM-3D…) and 3D simulation were developed. Fig.3 presents an example of cross sectional SEM image after BCP self-assembly inside guiding patterns [4] which is in agreement with the 3D-simulation [6].

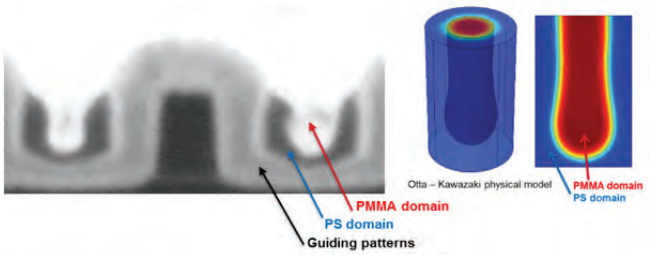

Figure 3: Experimental (SEM X-section) and simulated 3D morphology of CH shrink structure obtained with cylinder-forming PS-b-PMMA BCP.

Perspectives

To be fully adopted by IC manufacturing, DSA technology needs to demonstrate very low defectivity level at different step of the process (DSA and etching) as required by the ITRS roadmap for the future nodes. For that, more efforts must be focused on process conditions with regards to materials properties. Furthermore, DSA should satisfy the needs of IC design rules by taking into account both guide lithography and material capabilities.

Related Publications
[1] R. Tiron *et al.*, *Proc. SPIE 9423, Alternative Lithographic Technologies VII, 942317*, 2015.
[2] P. Pimenta Barros *et al.*, *Proc. SPIE 9428, Advanced Etch Technology for Nanopatterning IV, 94280D*, 2015.
[3] M. Argoud *et al.*, *60th EIPBN Conference*, San Diego, USA, 2015.
[4] A. Gharbi *et al.*, *DSA Symposium*, Leuven, Belgium, 2015.
[5] L. Pain *et al.*, *Solid State Technology, Vol. 58 NO.6*, 2015.
[6] A. Fouquet *et al.*, *Proc. SPIE 9423, Alternative Lithographic Technologies VII, 942324*, 2015.

Computational Aspects of Lithography

Research topics: Lithography, Proximity Correction, DSA, Multibeam

S. Bérard-Bergery, A. Fay, L. Perraud, P. Quéméré, J. Bustos (STM),
A. Fouquet, C. Masclaux, J. Chartoire, J. Belissard, J. Hazart

Partnership: Mapper, ASELTA, Mentor Graphics, STMicroelectronics

Context and Challenges

For advanced lithography technologies, data preparation is a key step to reach pattern fidelity. It consists in correcting patterning parameters with advanced algorithms by predicting lithography and its physical limitations. In optical lithography these parameters are mask and illumination sources. In electron lithography, these parameters are dose and shot shape and position. In 2015, we faced major challenges on two topics: Directed Self-Assembly (DSA) of block copolymers (BCP) and multi-beam technologies.

Main results: DSA patterning for via layers

DSA is a very promising technology for two reasons: It can enable lithography for nodes 7 nm and below and is a good low cost candidate for the replacement of multiple patterning used since node 14 nm. Two different options are currently investigated: lamellar DSA for lines/spaces patterning and cylindrical DSA for holes (via layers).

The use of cylindrical DSA consists in confining BCP in finely tuned cavities and letting BCP assemble to form arrays of vias. The first main difficulty is the design of the cavity giving the most stable assembly process for a given BCP.

The second difficulty is to provide suitable Optical Proximity Correction (OPC) to enable the lithography of the guiding pattern with 193 nm immersion scanner.

We recently demonstrated that 193 nm optical lithography is compatible with DSA technology provided that advanced masks and sources are used [1]. The study has empathized of peanut-shaped guiding patterns, as schematically represented in Fig.1.

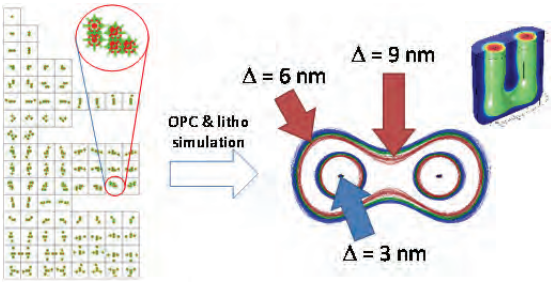

Figure 1: Simulation flow: Form a 10 nm node design, critical configurations are extracted. OPC and lithography are optimized to enhance their process window. After peanut-shapes extraction from the design, guiding pattern variation is computed as a function of 193 nm immersion lithography performance. Guiding pattern contours are subject to a maximum variation of 6 to 9 nm. Self-assembled BCP has consequently a placement uncertainty of 3 nm.

First experiments with a dedicated lithography mask have confirmed the ability of immersion scanner to build such guiding. This opens the way to the use of DSA in most of advanced foundries down to 10 nm node and below. Future work will be to assess process stability (defectivity, overlay) and to extend from the 10 nm to more aggressive nodes.

Main results: Data preparation for multi-beam technology

Mapper is developing a massively parallel multibeam technology. The ability to perform data preparation from customers design to machine format was questionable, first technically but also from an industrial point of view. We have shown, thanks to our partner ASELTA, that Mapper machine specifications and flow is supported by industry.

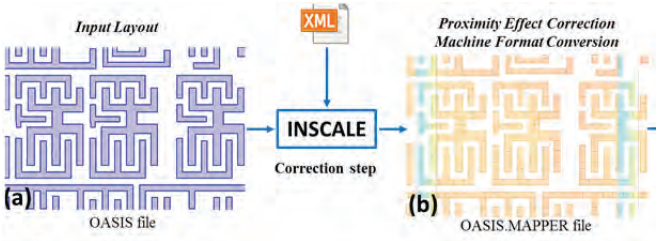

Figure 2: Schematic view of proximity effect correction.

Proximity Effect Correction: a model-based correction is applied to the layout presented in the first part of this section, in order to compensate for both short-range and long-range electronic effects (see Fig. 2).

Machine Format Conversion: the FLX-1200 tool accepts user layout files of a specific format called OASIS.MAPPER. Comparable in its principle with the conventional Fracturing step from the optical mask data-preparation, this step consists in converting the corrected file into a dedicated format readable by the multi-beam tool.

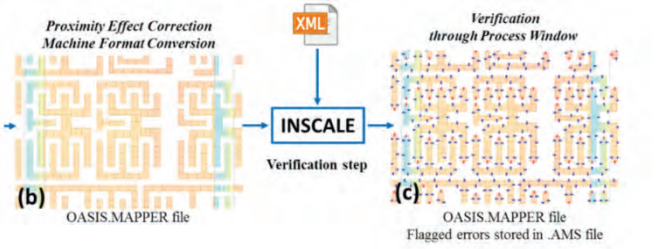

Figure 3: Schematic view of verification step.

Verification: prior to exposure, the applied correction accuracy has to be ascertained. The verification is a full chip model-based step (see Fig.3), allowing to simulate directly on the OASIS.MAPPER file the deviation of the printed pattern with respect to its target, for several process conditions (both exposure dose & tool spot size variations).

The layout used is a 28 nm metal layer from a real product. Including the verification step the total runtime is around 24 hours, which is acceptable in a production flow.

The flow has now to be confronted to real world as soon as Mapper's multibeam tool is operational.

Related Publications

[1] A. Fouquet *et al*. "193i lithography for contact doubling with grapho-epitaxy DSA: a simulation study", *Alternative Lithographic Technologies VII, Douglas J. Resnick, Editors, Proceedings of SPIE Vol. 9423, 942324,* 2015.

[2] A. Fay *et al*. "Complete data preparation flow for massively parallel e-beam lithography on 28nm node full-field design", *Direct-Write E-Beam Lithography, Proceedings of SPIE Vol. 9777* (SPIE, Bellingham, WA 2015), 9777-39.

Advanced Patterning of Stacked Nanowires Transistor

Research topics: 3D Devices, Stacked Si/SiGe Nanowire, Plasma Etching

P. Pimenta Barros, C. Arvet, C. Vizioz, A. Campo, N. Posseme, S. Barnola

Partnership: IBM, STMicroelectronics
Sponsorship: Nano2017

Context and Challenges

Fully depleted SOI devices have shown competitive electrical performances versus bulk approaches. In the continuity of conventional scaling (<10nm), Leti investigates the interest of Tri-gate and Nanowires (NW) architectures for better electrostatic control. This new 3D devices lead us to develop advanced patterning and new etching processes for both active, spacer and gate levels.

Main Results

Pitch lower than 40nm are required at the active level for sub-10nm node. Such pitch dimension can be achieved by Sidewall Image Transfer (SIT) approach [1]. We have recently demonstrated the electrical functionality of tri-gate SOI transistors fabricated by SIT [2]. Now SIT approach is developed to pattern Si/SiGe stacked NWs devices. First morphological demonstration of 60nm thick SiGe/Si fins with a pitch of 40nm has been performed this year (Fig.1a). A lateral SiGe loss has been observed after HF on both isolated and dense NW fins due to etch/wet interaction. Therefore, an alternative dry etching chemistry has been developed and seems very promising to avoid SiGe lateral loss (Fig.1b).

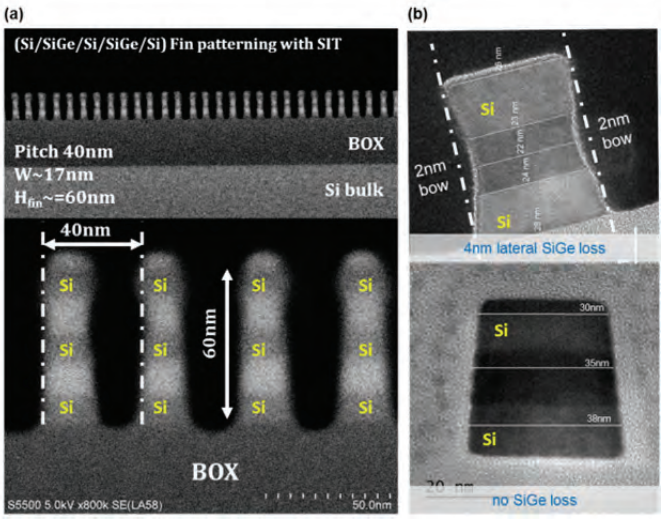

Figure 1: (a) SEM images of Si/SiGe fin patterned by SIT achieving a 40nm-pitch and 60nm-height. (b) TEM images of isolated Si/SiGe fin showing different profile after HF due to etch/wet interaction.

After the active patterning of NW channels, gate last processes can be then used to build the final transistor. There are many challenges to overcome for gate and spacer etching. The first one is to get straight gate profile on non-planar active with a topography varying from 36nm to 60nm-height (Fig.2).

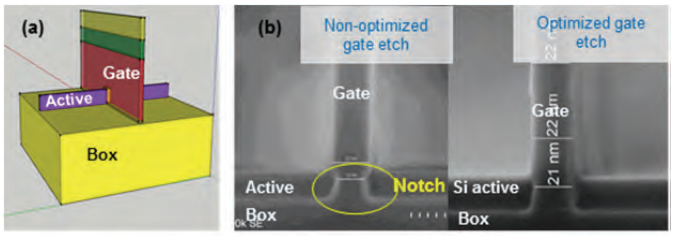

Figure 2: (a) 3D scheme of NW transistor architecture. (b) SEM images of gate profile obtained on 36nm-height active.

In the same way, spacer etching is critical. Indeed, a trade-off has to be found to etch all spacer residues on active sidewall minimizing Si active recess and spacer CD loss on gate. To achieve this, Atomic Layer Etching (ALE) process for SiN spacer etching step are under development at Leti [3].
Finally, the last critical step is the SiGe isotropic etching to Si (or Si to SiGe). This etching process is used at different steps of the NW transistor integration flow, as for example in order to form the suspended nanowires as shown on Fig.3.

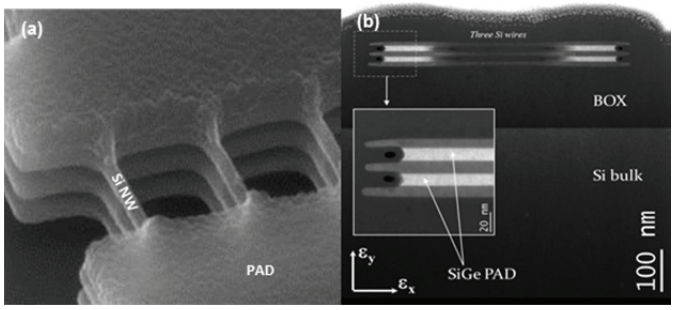

Figure 3: (a) Tilted-SEM image of suspended Si NWs after selective SiGe etching (b) Cross-sectional TEM image showing the three suspended Si NW and the remaining SiGe on PAD area.

Perspective

Our final goal will be to demonstrate electrical results for dense and isolated stacked nanowires using gate last approach.

Related Publications

[1] S.Barnola, N.Posseme, P.Pimenta Barros, C.Vizioz, C.Arvet, O.Pollet, A.Sarrazin, M.Garcia Barros, L.Desvoivres, O.ROS-Bengoechea, S.Barraud, "FEOL Patterning Challenges for Sub 14nm FDSOI Technology", *Proc. American Vacuum Society Conference*, October 2015.

[2] L. Gaben, S. Barraud, P. Pimenta-Barros, Y. Morand, J. Pradelles, M.-P. Samson, B. Previtali, P. Besson, F. Allain, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra, and M. Vinet, "Ω-Gate Nanowire Transistors Realized by Sidewall Image Transfer Patterning: 35nm channel pitch and opportunities for stacked-Nanowires architectures ", *International conference on Solid State Devices and Materials (SSDM)*, Sept 2015.

[3] O.Pollet, N. Posseme, V. Ah-Leung, M. Garcia Barros, "Silicon nitride etching by light ion implantation: a comprehensive study of layer modification and selective removal", *Proc. Dry Process Symposium (DPS) Conference*, November 2015.

04

ENERGY

- AlGaN/GaN-on-Si HEMT e-mode Devices
- Electrode Materials for 3 Volts All-Solid-State Lithium Microbatteries
- Highly Flexible Composite Thermal Harvesters - Autonomous Wireless Temperature Threshold Sensors

AlGaN/GaN-on-Si HEMT e-mode Devices

Research topics: AlGAN/GAN Power Devices, HEMT, GaN Epitaxy, 2DEG

E. Morvan, A. Torres, C. Leroux, L. Di Cioccio, M. Plissonnier, M. Charles

Partnership : RENAULT
Sponsorship: ENIAC-AGATE

Context and Challenges

Development of GaN-on-Si e-mode technology for high power applications requires high voltage epitaxy and suitable device architectures to enable normally off operation. Physical phenomenon understanding as key technological stages are of importance especially in order to monitor key parameters such as Ron (resistance of the device on the on mode, threshold voltage and leakage current on the reverse mode)

Main Results

Epitaxy: Buffer layers are needed to manage both the initial growth of GaN on silicon and to adjust the stress in the layers to control the wafer bow. By improving the insulating behavior of these layers by changing the growth parameters a leakage current of 80nA/mm2 at 600V has been achieved for a total thickness less than 4µm [1]. Furthermore, the hole defect density known to impact electrical devices has been drastically lowered thus increasing the blocking voltage limit. As a consequence devices up to 12mm² can be produced with no impact on the leakage current. This surface area is more than sufficient for the drain area of devices capable of passing 90A, which is currently our largest transistor size (Fig.1). To enable these developments we have developed a methodology that allows a rapid evaluation of epitaxial wafers and does not involve any sample preparation [2].

Ron: Ron improvement is also an important issue. We have studied the influence of epitaxy and gate process on the Ron (resistance on the on mode). Degradation of the 2DEG caused by the fluorine based etching of the Si3N4 was evidenced (Fig.2). We have demonstrated that fluorine defects located at the AlGaN/GaN interface can cause important deterioration of 2DEG density and mobility. A positive impact of Cl based etching to remove fluorine induced defects has been evidenced on mobility. Finally, the influence of epitaxy was demonstrated and an AlN spacer of 2nm was found to be an efficient way to improve ns (electron density) [3].

Thanks to these developments a 600 V MOSCHEMT channel was obtained (Fig 3) with a leakage of less than 80nA/mm^2 at 600 V, a $R_{on}S$ @ 25°C of 3 mohm.cm².and a V_{th}: >0,5V. Other parameters such as Id (600V) ~0,3µA/mm , Ig (600V) < 50 nA/mm and current collapse :Imax / Istressed =1,1 (10%) confirmed that these devices are at the state of art.

Perspectives

Extensive technological developments are ongoing, such as current collapse phenomenon understanding, fail analysis, epitaxial p type doping, high voltage epitaxy, precise etching, low leakage gate stack, innovative devices architecture to allow low Ron and high Vh. Improved 600V and 1200V devices are to be expected on 2016.

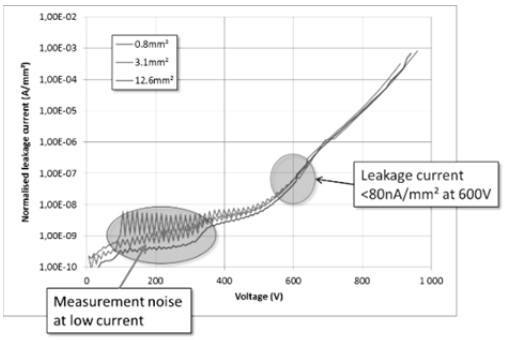

Figure 1: For a low hole defect density, the test structure area can be increased up to 12mm² with negligible impact on leakage current.

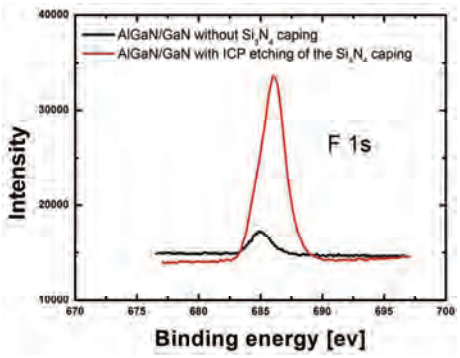

Figure 2: (a) XPS analysis of etched and non-etched sample. Important peak was found for the etched sample at 686,27eV. For the non-etched sample the small peak at 685,18eV is due to contamination. Both are related to F 1s peaks.

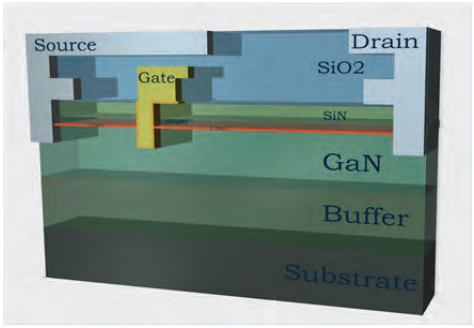

Figure 3: Cross section schematic of a Moshemt device. The off mode is obtained thanks to a gate recess. The gate stack is an Al_2O_3 dielectric and a tungsten metal gate.

Related Publications

[1] L. Di Cioccio, E. Morvan, M. Charles, *et al*. "From Epitaxy to Converters Topologies what Issues for 200 mm GaN/Si," *2015 IEEE International Electron Devices Meeting (IEDM 2015)*, 07 Dec - 09 Dec 2015, Washington, DC, USA.

[2] J. Lehmann ; C. Leroux ; G. Reimbold *et al*. "Novel sheet resistance measurement on AlGaN/GaN HEMT wafer adapted from four-point probe technique", *2nd International Conference on Tomography of Materials and Structures (ICTMS 2015)*, June 29th - July 3rd, Québec, Canada.

[3] Lehmann, J, Leroux, C, Charles, M "Influence of epitaxy and gate deposition process on Ron resistance of AlGaN/GaN-on-Si HEMT", *IEEE 27th International Symposium on Power Semiconductor (ISPSD)*, 10-14 May 2015, Hong Kong.

Electrode Materials for 3 Volts All-Solid-State Lithium Microbatteries

Research topics: All-Solid-State Microbatteries, Lithium-Ion Batteries, Intercalation Materials

F. Le Cras, H. Porthault, N. Bailly

Partnership : STMicroelectronics, ICMCB, IPREM
Sponsorship: PIA-TOURS2015

Context and Challenges

All-solid-state thin film batteries are rechargeable power sources that are manufactured by vacuum deposition techniques. Having a low footprint (from ~10 µm thick and few mm^2), they are well-adapted for being embedded in various microelectronic systems. So far, most of the microbatteries available on the market are 4 volts systems using a $LiCoO_2$ positive electrode material, similarly to conventional Li-ion batteries usually used as a main power supply, and a lithium anode. Nevertheless, a specific need for microbatteries able to supply a stable 3 V voltage for some particular applications was recently highlighted by our industrial partner. Consequently, alternative positive electrode materials had to be identified and optimized as thin films in order to meet this very narrow specifications.

Main Results

Among transition metal oxides, manganese (IV) oxides are the most prone to react with lithium at ~3.0 $V/Li^+/Li$. Moreover, the requirement for a very flat discharge curve (plateau) implies to use preferably a material intercalating lithium according to a two-phase mechanism. Therefore, lithium manganese oxide spinels (Fig.1) $Li[Li_xMn_{2-x}]O_4$ known to undergo a two-phase transformation to the rocksalt $Li_{2+x}Mn_{2-x}O_4$ were studied at first [1,2]. Li-Mn-O thin film electrodes, deposited by sputtering from $Li[Li_xMn_{2-x}]O_4$ targets prepared in-house, were optimized in terms of composition and degree of ordering by varying the conditions for sputtering and post-annealing. Finally, the specified discharge curve was achieved (Fig.2). Nevertheless, the biphasic reaction itself and the resulting anisotropic volume variation were found to hinder both the practical capacity (~25$\mu Ah.cm^{-2}.\mu m^{-1}$) and the capacity retention upon cycling. $Li_{0.33}MnO_2$, a more disordered variant of these materials was also investigated (Fig.2), without leading to significant improvements.

$Fe_2(MoO_4)_3$, an iron(III) molybdate having a Nasicon-type structure (Fig. 1) was also identified as a possible candidate. Indeed, a consequence of the inductive effect induced by the presence of the MoO_4 polyanions, the Fe^{3+}/Fe^{2+} redox potential is fortunately raised at about 3 V. This material, which undergoes a two-phase transformation to $Li_2Fe_2(MoO_4)_3$, was successfully synthesized as crystalline thin film electrodes after a low temperature annealing. The latter were found to exhibit a very flat discharge plateau at 3.05 V (Fig. 2) and a practical capacity at low rate close to theoretical one (32 $\mu Ah.cm^{-2}.\mu m^{-1}$). Further electrochemical measurements showed finally that both its low electronic conductivity and the anisotropic character of the Li^+ diffusion paths did not allow to maintain such a performance at higher current rates.

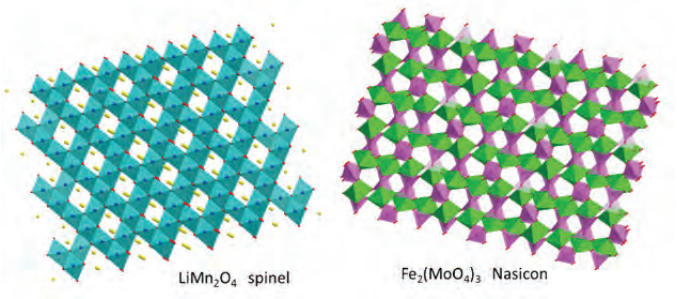

Figure 1: Crystal structure two types of 3 V intercalation materials: $LiMn_2O_4$ (spinel-type) and $Fe_2(MoO_4)_3$ (Nasicon-type). MnO_6 octahedra (light blue), FeO_6 octahedra (green), MoO_4 tetrahedra (purple).

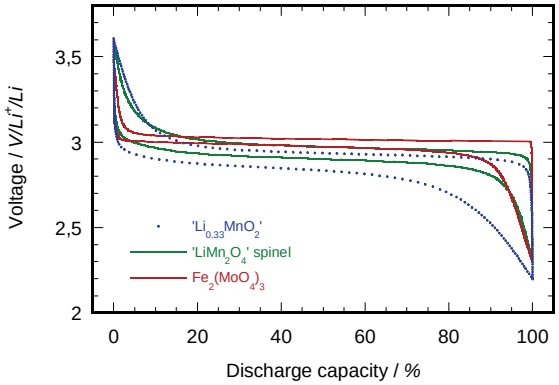

Figure 2: Comparison of voltage profiles for lithium intercalation/de-intercalation in three '3 V' thin-film cathode materials.

Perspectives

Since the beginning of this study, relaxation of the constraints on the flatness of the discharge curve occurs. This opens the way to more adapted solutions than the choice of materials undergoing a two-phase transformation upon lithiation (inherently limited in terms of ionic and electronic transport kinetics). Besides, the use of Li-ion configurations [3] will be an opportunity to widen the choice for suitable electrode materials.

Related Publications
[1] S. Cotte, B. Pecquenard, F. Le Cras, R. Grissa, H. Martinez, L. Bourgeois, "Lithium-rich manganese oxide spinel thin films as 3 V electrode for lithium batteries", *Electrochimica Acta*, 180, 528-534 (2015).
[2] N. Bailly, B. Mirvaux, J.-M. Boissel, H. Porthault, "Spinel $LiMn_2O_4$ thin films for 3 V operating all-solid-state lithium microbatteries", *228th Electrochemical Society Meeting*, 11-15 October, Phoenix, USA (2015).
[3] F. Le Cras, B. Pecquenard, V. Dubois, V. P. Phan, D. Guy-Bouyssou, "All-solid-state Li-ion microbatteries using silicon nanofilm anodes : high performance and memory effect", *Adv. Energy Mater.*, 5, 1501061 (2015).

Highly Flexible Composite Thermal Harvesters Autonomous Wireless Temperature Threshold Sensors

Research topics: Energy Harvesting, Pyro-Piezoelectricity, Polymers, Autonomous Sensors

B. Viala, E. Gusarova, B. Gusarov, S. Boisseau, L. Gimeno (G2ELab), O. Cugat (G2Elab)

Partnership : LITEN, PIEZOTECH-ARKEMA, NIMESIS

Context and Challenges

Energy harvesting is necessary when button cell batteries cannot be mounted or replaced. This will become real with the idea of an invisible IoT world made of ubiquitous connected objects (abandoned sensors, wearable electronics, intelligent packaging, smart skin etc.). All these objects must come increasingly autonomous, thin, flexible and transparent. All-polymer devices are becoming a key enabler of this idea. In this context electroactive polymers are booming as they can produce electrical energy with different daily and ordinary stimuli, like temperature variations and force. High performance pyroelectric and piezoelectric polymers are available as commercial sheets (Piezotech) or screen-printing materials (Arkema). The aim of this work is to explore the ability of both to produce efficient highly flexible thermal harvesters (no radiator needed). However the two properties (pyro and piezo) separately taken are not sufficient to easily power IoT sensors. The idea driven by our group is to combine them with a smart composite structure. The good pyroelectric performance of PVDF is assisted by enhanced direct-piezoelectric effect. To do so, we use thermal shape memory alloys SMA (wires) which can produce large thermally-induced strains (4%) that PVDF will then transform into additional electricity. As a result the produced energy is 200% more than just the pyroelectric effect (Fig. 2).

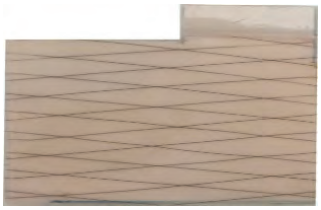

Figure 1: Thermal flexible composite harvester using commercial-grade PVDF and Nitinol wires on both sides used for demonstration (3 x 4.8 cm^2).

Main Results

The smart composite structure is shown in Fig.1. Crossing the temperature threshold of 38°C (fixed by the SMA), the composite harvester is able to produce a peak voltage of 300V, with energy of 200µJ (per event). When considering cycles (heating and cooling), the total energy density per cycle is 1mJ/cm^3. The PVDF voltage is high and needs to be lowered to store the energy or immediately power a sensor. Here we wanted to test the idea of an autonomous wireless over temperature detector powered by single event. After conversion, we were able to achieve a stable output of 1.86V with nearly 50% efficiency, delivering 100µJ energy, which was enough to power a wireless transmission module. The system emitted a signal without battery, demonstrating the autonomous wireless over temperature detector.

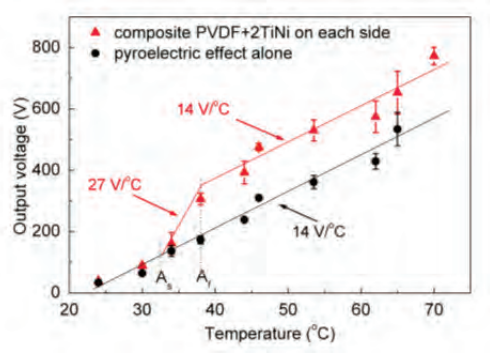

Figure 2: Output voltage vs. temperature (with no radiator).

PVDF is a very performing commercial material but the drawback is that it is factory polarized with complex stretching procedures and if depolarization occurs it cannot be repolarized, which may affect the harvester performances and durability after assembly. This is why we turned to screen-printing with P(VDF-TrFE) formulated inks. Clearly with thin films the energy will be lower but microcapacitors are easy to (re)polarization in house and optimal voltage adjustment before conversion can be realized by design. Fig.4 shows the screen-printed pyro-piezo harvester fabricated by our group. When combined with SMA, it is able to produce 35V with energy of 100µJ (before conversion). Currently 2 layers are required for wireless transmission.

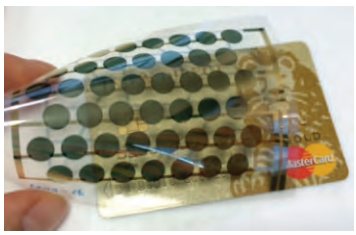

Figure 3: Flexible screen printed pyro-piezo microgenerators (8.5 x 5.5 cm^2).

Perspectives

We have demonstrated that simple temperature variations can be used efficiently (with no radiator) with original flexible smart composite structures. Now the perspectives are to achieve fully transparent all-polymer devices with using conductive polymer electrodes and thermal shape memory polymers. Screen printing offers the potential to address very large flexible surfaces (A4 and bigger). In fine, power management and RF emitter will be realized with ultra slim PCB mounting or flexible electronics.

Related Publications

[1] Gusarov, B., Gusarova, E., Viala, B., Gimeno, L., & Cugat, O. “PVDF piezoelectric voltage coefficient in situ measurements as a function of applied stress”, *Journal of Applied Polymer Science*, 133(14), 2016.

[2] Gusarov, B., Gimeno, L., Gusarova, E., Viala, B., Boisseau, S., Cugat, O., “Flexible composite thermal energy harvester using piezoelectric PVDF polymer and shape memory alloy”, *Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, 2015, pp. 722-725.

[3] Gusarova, E., Viala, B., Plihon, A., Gusarov, B., Gimeno, L., Cugat, O., “Flexible screen-printed piezoelectric P (VDF-TrFE) copolymer microgenerators for energy harvesting”, *Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, 2015, pp. 1901-1904.

05

MODELING & SIMULATION

- Simulation of Carrier Transport in CMOS and post-CMOS Devices
- Benchmarking of Device Architectures for 10nm & 7nm CMOS Technological Nodes
- RF Modeling of Advanced Devices from State-of-the-Art FDSOI to GaN Based III-V HEMTs
- Multiphysics Simulation and Modelling of RRAM

Simulation of Carrier Transport in CMOS and post-CMOS Devices

Research topics: Simulation, Transport, Nanoelectronics

F. Triozon, Y. M. Niquet, I. Duchemin, G. Mugny (STM), D. Rideau (STM), C. Delerue (IEMN)

Partnership : CEA-INAC, STMicroelectronics, IEMN
Sponsorship: ANR-NOODLES

Context and Challenges

Quantum effects play an increasing role when reducing the dimensions of the transistors and/or when using alternative channel materials with low carrier effective mass such as InGaAs alloys. In particular, carrier scattering is enhanced by quantum confinement. To be predictive, transport simulations require a 3D description of the device with its structural imperfections. The code TB_Sim [1], developed at Leti, addresses this challenge. New progress has been made in 2015 for the simulation of CMOS and post-CMOS devices.

Main Results

Carrier mobilities in FDSOI devices have been simulated using the Non-Equilibrium Green's Functions (NEGF) formalism, which treats elastic and inelastic scattering in a fully quantum mechanical description. In addition to the scattering mechanisms previously considered (phonon, remote Coulomb, and Si/SiO_2 roughness), an additional mechanism has been studied [2]: the remote surface roughness scattering due to the SiO_2/high-κ interface. It has been shown that the mobility degradation is correlated to the amplitude of the fluctuations of the interfacial layer thickness (see Fig.1). This has been cast into an analytical model for the mobility. The effect becomes important for very thin interfacial oxide thickness at high gate voltage, which is consistent with experimental data.

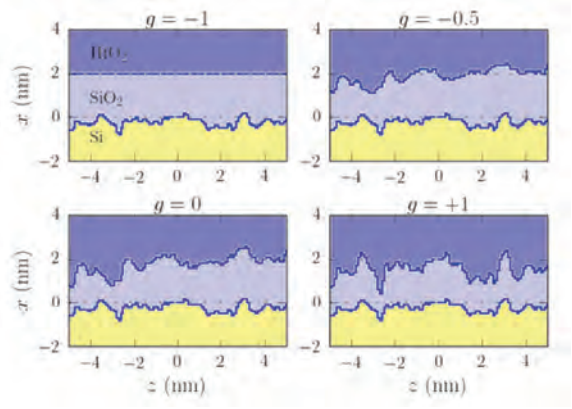

Figure 1: Different interface roughness profiles in the high-κ gate stack, considered in the carrier mobility simulations of Ref. [2].

The NEGF code has also been used to simulate single-electron transistors fabricated at Leti [3]. The channel is made of an ultra-thin silicon nanowire surrounded by a thick gate oxide and long spacers, thus enhancing Coulomb interactions: some of the fabricated devices exhibit Coulomb blockade even at room temperature. The simulated geometries have been chosen as close as possible to the real devices (see Fig.2). It has been shown that surface roughness creates quantum wells which trap the electrons. NEGF cannot describe transport in the Coulomb blockade regime but it has provided charging energies of the quantum wells and transmission probabilities which are in good agreement with the experimental data [3].

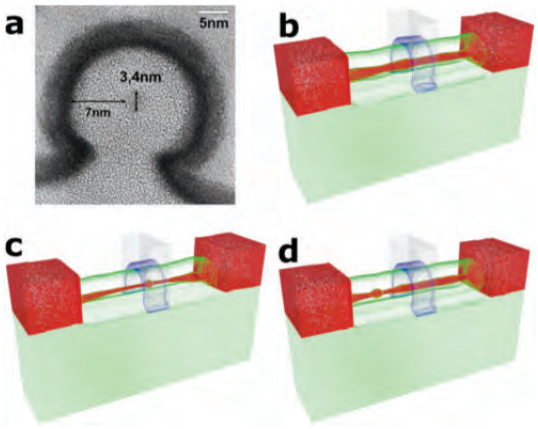

Figure 2: (a) Transmission electron microscopy cross section of a single-electron transistor. (b, c, d) Simulated structures with different interface roughness profiles. The silicon nanowire and its bulk-like source and drain are represented in red, and the thick SiO2 layer surrounding the channel in green. From Ref. [3].

Another part of our activity has focused on III-V channels, where quantum effects and non-parabolicity of the band structure cannot be neglected. Different band structure models for InGaAs alloys have been evaluated [4], in order to obtain accurate values for the conduction band valleys energies and effective masses. The effect of non-parabolicity on MOS capacitance has also been studied [5].

Perspectives

The NEGF simulations of silicon MOSFETs are currently extended to non-planar geometries and to the large bias voltage regime. In particular, the contact resistances in the source and spacer regions are under investigation. The simulation of single-electron transistors will be refined by taking into account electron correlations in the quantum wells. The validated III-V band structures models will be used in device simulations.

Related Publications
[1] http://inac.cea.fr/L_Sim/TB_Sim/
[2] Y.-M. Niquet, I. Duchemin, V.-H. Nguyen, F. Triozon, D. Rideau, *"Remote surface roughness scattering in fully depleted silicon-on-insulator devices with high-κ/SiO_2 gate stacks"*, *Applied Physics Letters 106*, 023508 (2015).
[3] R. Lavieville, F. Triozon, S. Barraud, A. Corna, X. Jehl, M. Sanquer, J. Li, A. Abisset, I. Duchemin, Y.-M. Niquet, *"Quantum Dot Made in Metal Oxide Silicon-Nanowire Field Effect Transistor Working at Room Temperature"*, *Nano Letters 15*, 2958-2964 (2015).
[4] G. Mugny, D. Rideau, F. Triozon, Y.-M. Niquet, C. Kriso, F.G. Pereira, D. Garetto, C. Tavernier, C. Delerue, *"Full-zone k.p parametrization for III-As materials"*, *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2015)*, Washington DC, pp. 28-31.
[5] G.Mugny, F.Triozon, J.Li, Y.-M.Niquet, G.Hiblot, D.Rideau, C.Delerue, *"Band structure of III-V thin films: an atomistic study of non-parabolic effects in confinement direction"*, *2015 EUROSOI Workshop*, pp. 301-304.

Benchmarking of Device Architectures for 10nm & 7nm CMOS Technological Nodes

Research topics: Benchmark, Compact model, FDSOI, FinFET, Nanowire

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S. Barraud, F. Triozon, M. Vinet, J-C. Barbé

Partnership : STMicroelectronics
Sponsorship: ENIAC-Places2Be

Context and Challenges

Pursuing CMOS device down scaling to the ultimate technological nodes requires to be able to identify the most promising architectures to fulfill performance requirements. Device architectures benchmark is then a challenge which aims to evaluate the potentiality of a particular technology at IC level. Then benchmarking results allow to put more focus on adequate technological developments depending on the targeted application.

Main Results

Benchmark activity requires to integrate the full virtual fab. capability ranging from TCAD simulations to Circuits simulation through compact/SPICE modeling and associated parameter extraction methodology.
First, process and device TCAD decks are developed to reproduce the process flow of the envisaged different device structures (see Fig.1). Full validation is based on the comparison with the large experimental database we built with our partners. This validation step makes the TCAD tools predictive. For instance strain/stress fields are simulated to assess the efficiency of different mobility boosters [1] (Gate Last, raised source/drain, etc.). For example Fig.2.a illustrates the comparison between TCAD and experimental strain maps obtained by Precession Electron Diffraction (PED) before dummy gate removal. This result demonstrates the accuracy of the TCAD simulation.

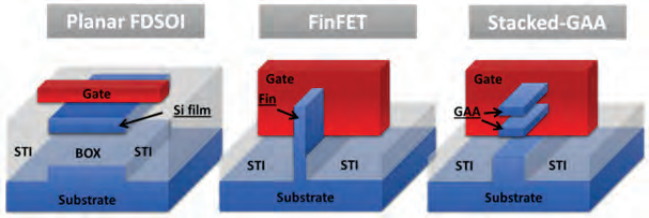

Figure 1: Schematics of benchmarked MOSFET architectures.

Then Compact/SPICE model and predictive model cards are needed to link process development and circuit design. Thus performance and power consumption analyses are carried out from IC simulations to validate or to retarget device performances to fulfill application requirements.
However, model card predictivity or retargeting is a delicate exercise which relies on optimization steps which consist in demonstrating that electrostatic and transport performances are achievable. While electrostatics is considered through process and electrical TCAD simulations, electronic transport realistic models are based on our large experimental database (from STMicroelectronics and Leti). From this database the mobility tradeoff are built for the different studied architectures including impact of quantum confinement.

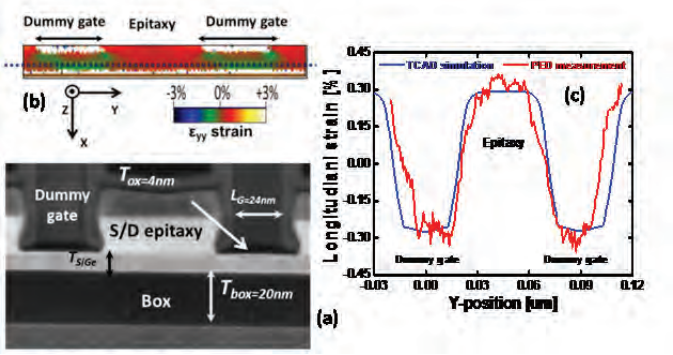

Figure 2: GL integration: (a) TEM image of pMOSFET transistor along the channel direction, (b) corresponding strain measurement by PED and (c) comparison of the longitudinal strain profiles along Y-direction of 2D mechanical simulation & experimental PED Diffraction (i.e. εyy≈-0.3% below dummy gate).

As presented in [2], final benchmark is possible using calibrated and predictive model cards based on both experimental data and TCAD simulations. As illustrated in Fig.3, the proposed benchmark methodology allows us to draw clear conclusions concerning the benefits of the envisaged CMOS architectures for future technological nodes. For the 10nm node, FDSOI and Fin-FET give the same speed at constant static power. However, FDSOI consumes less dynamic power thanks to lower load capacitances per stage (-19% compared with FF) at constant speed. At 7nm, the Fin-FET will require additional stressors to satisfy performance specifications. From a performance point of view, the Stacked-GAA architecture is then the most credible option and could be the most promising architecture to address the sub 7nm technological node.

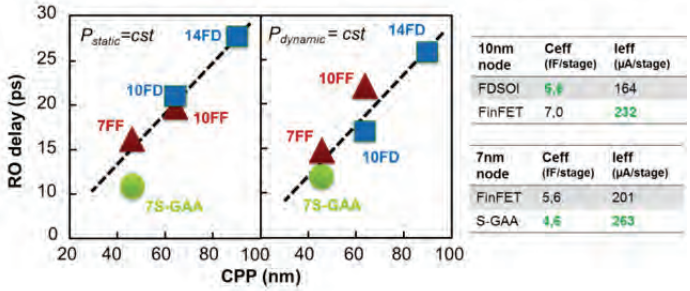

Figure 3: RO delay versus nodes for all architectures. Symbols are RO simulations; dashed line is the trend of +35% on speed per node.

Perspectives

The developed benchmark methodology will be used as a standard for the future developments at LETI. Stacked nano-wires/nano-sheets will be considered to address the 5nm CMOS technological node.

Related Publications
[1] T. Poiroux *et al.*, "Mechanical simulation of stress engineering solutions in highly strained p-type FDSOI MOSFETs for 14-nm node and beyond", *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2015)*, Sept. 9-11 2015, Washington DC, USA.
[2] O. Rozeau, J. Lacord, S. Martinie, A. Idrissi-El Oudrhiri, M.-A. Jaud, S. Barraud, T. Poiroux, M. Vinet, J.-C. Barbé, "Performance benchmarking of device architectures for the sub-10nm CMOS technological nodes", 5th *International Workshop on Nanotechnology and Application (IWNA 2015)*, November 11 -14 2015, Vung Tau, Vietnam (invited paper).

RF Modeling of Advanced Devices from State-of-the-Art FDSOI to GaN Based III-V HEMTs

Research topics: RF, FDSOI, III-V

L. Lucci, P. Martin, M. Pala (CNRS, INPGrenoble)

Partnership: CNRS-INP Grenoble

Context and Challenges

There is a growing interest in high-frequency applications of end-of-the-roadmap technologies, like FDSOI. Applications in the RF and mmW segments are fostering the demand for accurate RF models, a need that in the past was reserved to technology nodes two steps back the digital one. This combination of fast-pace timing and high accuracy represents a challenge the simulation and modeling lab of Leti is trying to face by abating the distinction between characterization and modeling. Continuous support and improvement of physically-based models like Leti-UTSOI and Leti-HSP are also a major activity focus.

FDSOI: RF modeling and benchmarking

Fully-depleted silicon-on-insulator (FDSOI) is a promising candidate for the continuous downscaling of MOS transistors. Ultra-thin body and box (UTBB) technology, as implemented in the last generations of FDSOI, has already provided improved DC performances compared to standard bulk.
RF applications were already reported and the technology provides better RF performances due to the reduction of parasitic capacitances.
However, although specific SPICE models do exist for FDSOI transistors, such as Leti-UTSOI or Berkeley BSIM-MG, their suitability for high-frequency RF designs have yet to be evaluated.

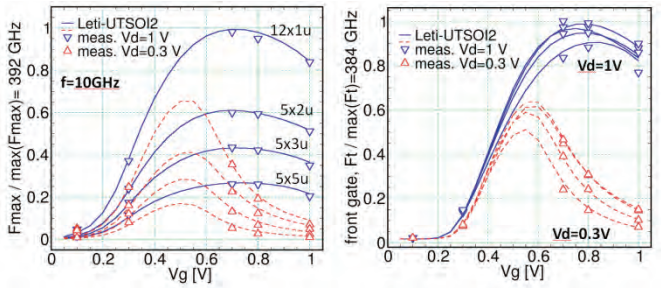

Figure 1: High-frequency figures of merit (left: maximum oscillating frequency, fmax and right: current gain cut-off, ft) for fully-depleted NMOS devices at the 28nm technology node. Measured device is minimum channel length (Lnom=30nm). Symbols are experimental data, dashed and continuous lines are Spice simulations done with the Leti-UTSOI2 model with RF-add-on.

In this framework we planned an assessment of the Leti-UTSOI2 compact model for RF applications. RF small-signal performances of Ultra-Thin Body and Box FD-SOI transistors were evaluated using state-of-the-art 4-port characterization in the 100MHz - 40GHz frequency range both at the 14nm and 28nm technology node.

Front-Gate cut-off frequencies and related figures of merit were extracted to assess the capabilities of the FDSOI technology. Back-Gate cut-off frequency was also extracted and shown to be as high as 80 GHz while front-gate cut-off peaked at 380 GHz [1].
A 4-port-structure based RF extraction flow was implemented and a SPICE model add-on for the Leti-UTSOI2 featuring gate width scalability was demonstrated to correctly model both the front- and the back-gate for RF purposes.

HSP: from power to RF

In parallel to the technology development and optimization of AlGaN/GaN HEMTs [2], there is also a need for accurate compact SPICE models to simulate the electro-thermal behavior of such transistors. Empirical models are at present used for circuit simulation of e.g. RF power circuits and fall short in terms of accuracy and predictive capability.

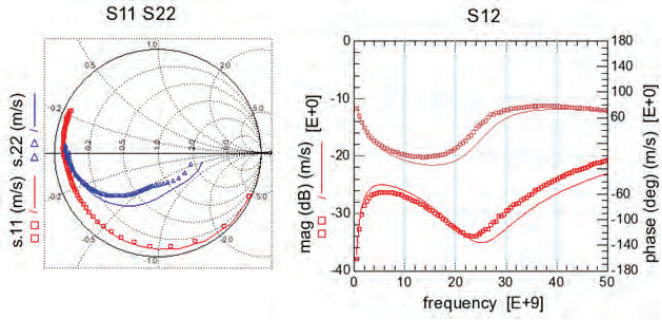

Figure 2: Comparison between simulated and measured S-parameters for one bias point of a reference Foundry GaN HEMTs. Measurements up to 50 GHz were provided by the CMC member foundry. Simulations were carried out in ELDO with Leti-HSP model in Verilog-A.

The need for a more physical approach to compact modeling was expressed already in 2013-2014 by the industrial consortium under the Compact Modeling Coalition (CMC/Si2) which called a selection for an open standard model. The Leti-HSP GaN model [3] has been examined as a possible standard model and passed the first two phases of the standard selection procedure, both for power RF amplification and power switching applications. To this end, a substantial set of experimental data was provided by CMC both for switching and RF applications and candidate models were required to demonstrate a complete extraction flow for the two applications to benchmark the model in terms of speed, convergence, ease-of-use and physical soundness.

Related Publications

[1] J.-C. Barbé, L. Lucci, A. Siligaris, P. Vincent, O. Faynot, "4-port RF performance assessment and compact modeling of UTBB-FDSOI transistors," *in 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 355-358, 17-19 May 2015, Phoenix, USA.

[2] L. Lucci, J.-C. Barbé, M. Pala, "Full-quantum study of AlGaN/GaN HEMTs with InAlN back-barrier," *in 2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pp.128-131, Sept. 9-11 2015, Washington DC, USA.

[3] P. Martin, L. Lucci, J.-C. Barbé, "The Leti-HSP Surface-Potential-Based SPICE Model for AlGaN/GaN Power Devices", *Compound Semiconductor Week (CSW 2015)*, pp. 308-309, June 28 – July 2, 2015, Santa Barbara (CA, USA).

Multiphysics Simulation and Modelling of RRAM

Research topics: OxRRAM, CBRAM, Atomistic Simulation, Device Modelling

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Partnership : Stanford University
Sponsorship: STMicroelectronics, Nanoscience Foundation, ENIAC-PANACHE

Context and Challenges

Oxide based RRAMs may revolutionize the future computing systems for replacing FLASH technology due to their low power operation, high switching speed and capability to be used in neuromorphic applications. However, a clear and a comprehensive microscopic view of several essential mechanisms is still missing. Here we concentrate onto the low-resistance state thermal stability, the impact of various doping materials, the connection between the device electrical characteristics and the metal electrode material.
Moreover, compact model is a mandatory tool to design innovative circuits using RRAMs. Thus, CBRAM and OxRRAM compact models are developed.

Low resistance state stability and doping

1T1R devices were integrated in a 65-nm CMOS technology with PVD bottom electrode TiN (35 nm) and top electrode Ti (10 nm). For the dielectrics 5 nm of HfO_2 and $Hf_{1-x}Al_{2x}O_{2+x}$ (9:1) (i.e. HfAlO) were deposited by atomic layer deposition at 300 °C where (9:1) stands for 9 cycles of HfO_2 followed by 1 cycle of Al_2O_3. The data retention measurements were performed by programming the devices with a compliance current of 100µA. The R_{on} retention evolution of HfO_2 and HfAlO with time at 200 °C shows that R_{on} fails toward high resistance values as the retention time increases which we associate to the diffusion of oxygen vacancies V_O. Fig1.a) shows the extracted activation energy E_a at 1.49 eV and 1.75 eV for respectively HfO_2 and HfAlO which has a better R_{on} stability. Under the hypothesis that R_{on} retention is mainly dominated by neutral V_O diffusion process in the oxide and that the activation energies from experiment and theory are directly related, we calculated the diffusion barriers of V_O (using CI-NEB) by considering different atomic positions in HfAlO and HfO_2, as shown in Fig.1.b).

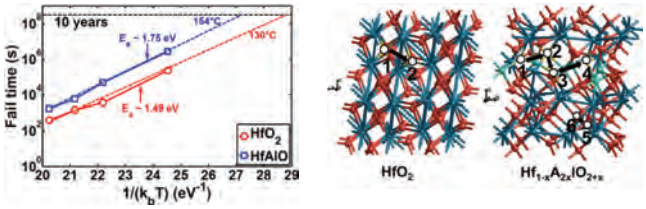

Figure 1: (a) Extracted failure time for HfO_2 and HfAlO RRAM. A higher activation energy E_a is extracted for HfAlO. (b) m-HfO_2 structure with the atomic positions numbered 1 and 2 considered for V_O diffusion inside HfO_2 and atomic positions numbered 1, 2, 3, 4, 5, and 6 considered for V_O diffusion in HfAlO.

The calculated V_O diffusion barrier in HfO_2 was 2.16 eV for the considered atomic positions. In order to compare this calculated E_a with V_O diffusion in HfAlO, depending onto the different atomic positions considered the calculated $E_a$varies from 2.08 to 2.69 eV. Since diffusion is a statistical process with different paths involved, the activation energy is determined by the energy of the highest transition state which explains the better HfAlO thermal stability [1].

Role of the top electrode

Depending onto the oxygen reactivity of the top electrode the forming voltage can be largely reduced using a high oxygen solubility metal like Ti. Moreover, thermal stability and RESET progressive character are largely improved with Ti. Therefore, we investigated the stability of oxygen point defects in HfO_2 by ab initio calculations for various charged states of V_O, O_i (interstitial) and Frenkel Pair. Our results are summarized onto Fig.2.a) and we propose a consistent scenario depending onto the oxygen reactivity of the electrode and the effective polarization onto Fig. 2.b).

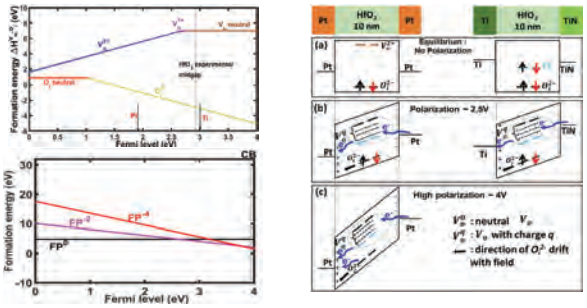

Figure 2: (a) Formation energy of neutral and charged V_O, O_i and FP with respect to the Fermi level measured from the VB (b) Simplified energy band diagrams of Pt/HfO_2/Pt and TiN/HfO_2/Ti stacks during FP formation via e− injection under (a) equilibrium conditions with no polarization (b) a polarization of around 2.5 V and (c) a high voltage polarization ≥ 4V.

Physical Compact Modelling

To design innovative circuits using RRAMs, a compact model is mandatory. This model should be fast, robust and accurate. We developed compact models for the different RRAM technologies: CBRAM, OxRRAM and also PCRAM. Models are written in Verilog-A and calibrated on electrical measurements. Statistical dispersion is also taken into account as shown in figure 3 for a CBRAM device. Monte Carlo simulations are done with adapted Gaussian law on Ron and Roff to reproduce the variability of the technology. Then, compact models are incorporated in Cadence design flow using Eldo simulator. Different electrical circuits are tested to prove the robustness of the proposed models [2].

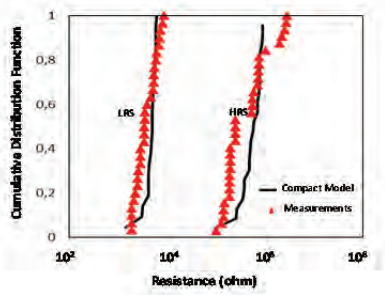

Figure 3: Monte Carlo simulations are done with adapted Gaussian law on Ron and Roff to reproduce the variability of the technology.

Related Publications
[1] Traore, B.; Blaise, P.; Vianello, E.; Grampeix, H.; Jeannot, S.; Perniola, L.; De Salvo, B.; Nishi, Y., "On the Origin of Low-Resistance State Retention Failure in HfO_2-Based RRAM and Impact of Doping/Alloying ", *IEEE Transactions on Electron Devices*, Volume:62, Issue: 12, 2015.
[2] M. Reyboz, O. Cueto, P. Blaise, P. Dorion, A. Payet, G. Le Carval, E. Vianello and G. Molas, "From Ab-Initio to Compact Modeling of Resistive Memories", *MOS-AK Workshop*, March 12, 2015, Grenoble, France.

06

PASSIVE & RF COMPONENTS

- No-Loss Magnetic Nanocomposite Materials for RF
- Doped PZT Thin Films for Tunable Capacitor Applications
- Leakage Current and Reliability on Planar High k Capacitor with Al2O3 Dielectric Deposited by ALD
- Frequency Tunable Bulk Acoustic Wave Resonators

No-Loss Magnetic Nanocomposite Materials for RF

Research topics: Magnetic Materials, Radiofrequency Devices

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Partnership: CNRS-LTM, CEA-INAC
Sponsorship: NanoSciences Fundation, PIA-TOURS2015

Context and Challenges

Metal-polymer nanocomposites define a class of new materials (non-conductive by definition) renewing established ideas in microelectronics or flexible electronics. They have astonishing properties (permeability with no loss, giant permittivity, tunnel conductivity switching etc.), leading to strong paradigm shifts in physics. Many functional composite structures can be designed with surface functionalization of metallic particles and modified polymers. This is the final arrangement of particles (volume fraction and spacing) that gives the desired property. For instance with magnetic nanoparticles, the least compact (square lattice) gives antiferromagnetic properties (AF) while the most compact (triangular lattice) gives ferromagnetic properties (F). The aim of this work is to achieve the ideal F-magnetic material with virtually no loss at high frequency.

Main Results

To reach this goal, we used high magnetization carbon-coated cobalt nanoparticles (Co/C) and polystyrene (PS). The carbon coating was the process key enabler. It offers an efficient protection against oxidation, preserving the high magnetization of cobalt at the end, and allows efficient carbon-chemistry to firmly attach a thin layer (few nm) of PS directly on the surface of the nanoparticles. Like this, tiny non-conductive core-shell nanoparticles of cobalt are formed, making them electrically insulated from each other. Then, they can be densely packed (up to ~ 20 vol. %) and embedded in supporting matrix of polymer (same or not). The achieved nanocomposite solution was easy to spin-coat to form uniform films (1 to 20 µm thick). Details of the film microstructure are shown in Fig.1. Homogeneous and very mechanically resistant films were obtained. Additionally, the films can be easily hot pressed, structured and transferred onto another substrate (like Kapton). Two patents were filled on non-conventional integration means.

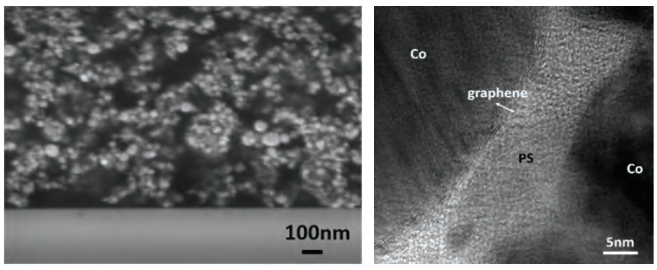

Figure 1: cross-section and close view of Co/C nanocomposite film.

As reported in the general phase diagram for RF magnetic materials shown in Fig. 2, we achieved a remarkable high film-resistivity while the material retains a high magnetization. This puts metal-polymer magnetic composites in direct competition with microwave ferrites but with the very significant difference that there is no loss here. Indeed, the RF spectrum shown in Fig.3 attests on the absence of dispersive phenomena and loss, whether electric or magnetic. Finally, the effective constants are μ_{eff}~2 and ε_{eff}~3, with extremely low loss ~ 10^{-3} and these performances are maintained up to at least 10 GHz.

Perspectives

The characteristics of the nanocomposite of Co/C are in the target of ideal (non-conductive) materials for antenna miniaturization. However, besides the achievement of these unique properties, the permeability may seem low for others applications at few GHz and in particular inductors. Therefore, perspectives of work to meet the demand of a higher permeability include new compositions (softer alloys) and bigger nanoparticles (to switch from single to multi-domains) but in the limit of 200 nm to avoid eddy currents.

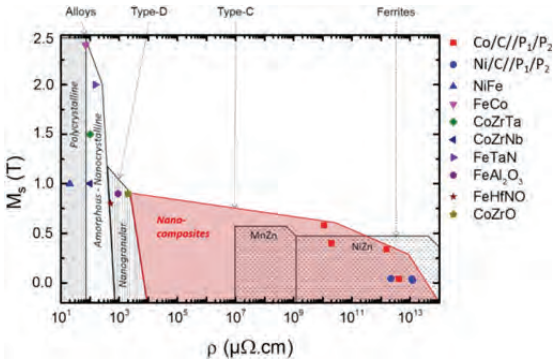

Figure 2: General M_s vs. ρ phase diagram for RF magnetic materials.

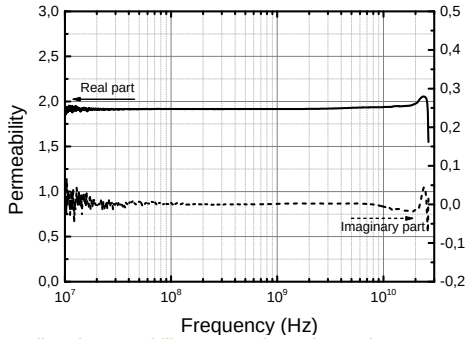

Figure 3: Broadband permeability spectra (experimental set-up was limited above 10 GHz.

Related Publications

[1] H. Takacs, B. Viala, J.H. Tortai, V. Hermán, F. Duclairoir, "Non-conductive ferromagnetic carbon-coated (Co, Ni) metal/polystyrene nanocomposites films", *Journal of Applied Physics*, 2016, 119(9), 093907.
[2] H. Takacs, B. Viala, V. Hermán, J. Alarcon Ramos, J.H. Tortai, F. Duclairoir, "New Approach to Closely Spaced Disordered Cobalt–Graphene Polymer Nanocomposites for Non-Conductive RF Ferromagnetic Films", *IEEE Transactions on Magnetics*, 2015 51(11).
[3] V. Hermán, H. Takacs, F. Duclairoir, O. Renault, J.H. Tortai, B. Viala, "Core double–shell cobalt/graphene/polystyrene magnetic nanocomposites synthesized by in situ sonochemical polymerization", *RSC Adv.*, 2015, 5, 51371.

Doped PZT Thin Films for Tunable Capacitor Applications

Research topics: Tunable Capacitors, Ferroelectric, PZT, Doping

W. Benhadjala, G. Le Rhun, C. Dieppedale, F. Sonnerat, J. Guillaume, C. Bonnard, P. Renaux, H. Sibuet, C. Billard, P. Gardes (ST), P. Poveda (ST)

Partnership : STMicroelectronics
Sponsorship: PIA-TOURS2015

Context and Challenges

Modern RF systems have triggered an important and urgent demand for inexpensive voltage controlled capacitors (i.e. tunable capacitors) used for a wide range of applications such as tunable antennas or low-noise voltage-controlled oscillators (VCO). Development of tunable capacitors requires optimized dielectric thin films to minimize device loss (i.e. increase the quality factor) and maximize tunability. Indeed, these properties play a decisive role in RF applications. Ferroelectric thin films have particularly attracted considerable interest for tunable applications due to their high permittivity and large dielectric non linearity under DC bias field. Lead zirconate titanate ($Pb[Zr_xTi_{1-x}]O_3$, PZT) which has been actively investigated and used in various industrial domains including non-volatile memories and microelectromechanical systems (MEMS), is especially a well-known candidate due to its remarkable ferroelectric properties and stability in device operating ranges. However, there are several issues that PZT-based capacitors must address, in particular the voltage tunability. Therefore, much attention has been focused on the PZT properties optimization by adding a small amount of dopants.

Main Results

In this work, integrated metal-insulator-metal (MIM) capacitors using sol-gel PZT doped with lanthanum (La, PLZT), manganese (Mn, PMZT) and niobium (Nb, PNZT) were successfully processed and characterized for tunable applications [1]. The capacitor structure is shown on Fig.1.

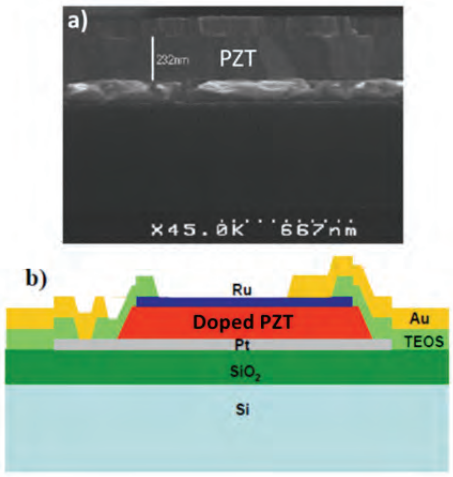

Figure 1: (a) SEM image and b) schematic representation of the developed MIM structures.

Electrical properties of PZT, PMZT (2% Mn), PLZT (2.5% La) and PNZT (2% Nb) films were investigated for tunable capacitor applications. We demonstrated that leakage current density can be significantly decreased by 1 (with La or Mn) to 3 (with Nb) orders of magnitude by modifying PZT. Developed thin films exhibit high dielectric strengths achieving 2.5 MV/cm (with Mn or Nb) and outstanding tunabilities above 75% at 10 kHz and 430 kV/cm. By comparing our results to the state of the art, we observed that PMZT tunability, which reaches 89% at 100 kHz and 870 kV/cm is among the highest ones reported in the literature for PZT derived thin films, but also for other ferroelectric materials. Indeed, in comparison, the tunability of BST-based materials, typically studied for voltage tunable applications, are generally inferior to 80 %.

Dielectric properties of studied PZT, PMZT, PLZT and PNZT thin films are summarized in Table 1. PMZT films exhibit moderate permittivity, high quality factor, very high tunability and dielectric strength and low leakage current. These remarkable results indicate that Mn doped PZT thin films are the most promising candidates for RF tunable capacitors [2].

	PZT	PMZT	PLZT	PNZT
Permittivity	++	+	++	++
Quality factor	+	++	-	+
Tunability	+	++	-	-
Leakage current	-	+	+	++
Dielectric strength	-	++	+	++

Table 1: Comparative table of dielectric properties of PZT-based thin films.

It is noteworthy that performance of PNZT thin films, such as extremely low leakage current and very high permittivity and dielectric strength are especially attractive for decoupling capacitor applications.

Perspectives

Further investigations are currently conducted to determine the properties of Mn doped PZT at RF frequencies.

Related Publications
[1] W. Benhadjala, G. Le Rhun, Ch. Dieppedale, F. Sonnerat, J. Guillaume, C. Bonnard, Ph. Renaux, H. Sibuet, Ch. Billard, P. Gardes, P. Poveda. "Sol-gel doped-PZT thin films for integrated tunable capacitors", *International Symposium on Microelectronics: FALL 2015,* Vol. 2015, No. 1, pp. 256-261.
[2] W. Benhadjala, F. Sonnerat, J. Guillaume, Ch. Dieppedale, Ph. Renaux, G. Le Rhun, H. Sibuet, Ch. Billard. "Highly tunable Mn-doped PZT thin films for integrated RF devices", *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT),* January 2015, Vol. 2015, No. DPC, pp. 2095-2127.

Leakage Current and Reliability on Planar High k Capacitor with Al_2O_3 Dielectric Deposited by ALD

Research topics: Capacitor, ALD, High Voltage, Al_2O_3

S. Madassamy, F. Voiron (IPDiA), A. P. Nguyen (IPDiA), A. Lefèvre, G. Parat, D. Buttard (SiNaPS), A.Sylvestre(G2ELab)

Partnership: IPDiA, G2ELab, SiNaPS
Sponsorship: PIA-Medilight2017

Context and Challenges

New applications in microelectronics need the integration of high capacitance devices. One way for this development is the use of silicon wafers micromachining to create arrays with a very high developed surface. But, the challenge is to deposit conformal dielectric layers all along the deep structures with ultra-high aspect ratio of 1:40. Atomic Layer Deposition (ALD) is a technique of choice to realize this technology. But, the dielectric has also to present a high permittivity and high breakdown strength to meet the requirements of future devices. Due to its wide band-gap, Al_2O_3 is known to have a moderate leakage current and a good dielectric strength and could be deposited in high aspect ratio structures by ALD. Recently, leakage currents for very thin layers of Al_2O_3 (thickness <10 nm) were studied and the S-shape trend of the current vs electric field was explained. This S-shape trend is in relation with an increase on the dielectric strength observed typically for dielectric thicknesses lower than 40 nm. To go further and develop interesting capacitance that can withstand higher voltage (>10 V), higher thickness above 50 nm is needed and few studies were carried out to analyze the leakage mechanisms and breakdown strength.

Main Results

MOS (Metal/Oxide/Semiconductor) planar capacitors, with top aluminum electrodes are studied to determine the intrinsic properties of Al_2O_3 before its integration in 3D technology. A 50 nm-thick Al_2O_3 dielectric is deposited on a p-Si substrate. The Al_2O_3 dielectric is deposited below 400°C by thermal ALD with trimethyl aluminum (TMA) and ozone precursors. Voltage ramp (VRamp) and capacitance-voltage (C-V) were carried out. The MOS device is used for the quantitative determination of the dielectric characteristics: i.e. dielectric bulk defects and conduction mode. The density of bulk defects is calculated back from C-V measurements, through the determination of the flatband voltage. The determination of the conduction mechanisms at high field is based on I(V) linearization and fit with classical Poole-Frenkel model. The dielectric strength evaluation is performed using a VRamp experiment considering the breakdown voltage.

It is interesting to verify experimentally how the dielectric trap characteristics are linked to the dielectric strength. It is recalled that the dielectric strength corresponds to the net charges that can flow across the dielectric until the point where failure is detected.

The die to die correlations between Ebd and ΦT are presented on the Fig.1. The Pearson correlation coefficient is around 0.73, corresponding to a good correlation level. Therefore it is concluded, on these samples, that the breakdown field is clearly correlated to the trap density.

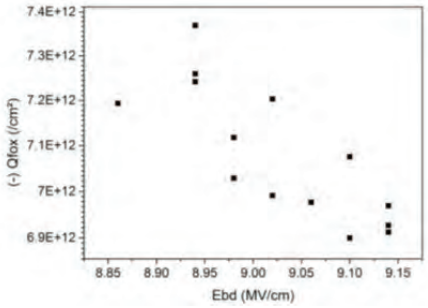

Figure 1: Correlation of trap density vs Ebd.

Further investigations of the leakage measured demonstrate that a Poole Frenkel conduction mechanism can be observed as pictured in Fig.2. After linearization of the variation of leakage with temperature, a dielectric constant can be calculated. The value is ranging from 9.4 to 11.3 over 32 measured samples which is in accordance with MOS C-V measurements in accumulation, and are in good agreement with values found in the literature for this material.

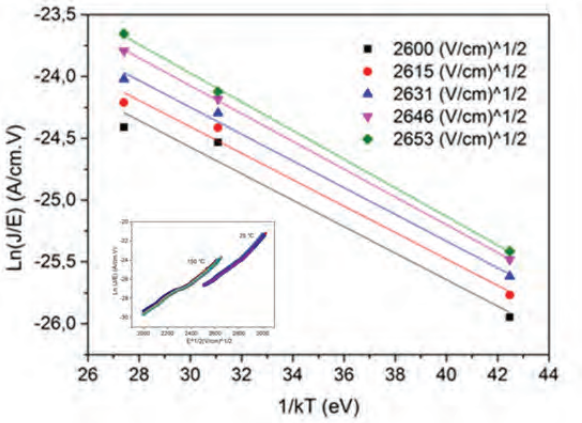

Figure 2: Arrhenius plot Ln(J/E) vs 1/kT (Inset) Poole-Frenkel Ln(J/E) vs E1/2 plot.

Perspectives

High thickness of Al_2O_3 deposited by ALD was studied in MOS structures. An important amount of oxide traps was found in the high thickness dielectric that clearly lead to higher leakage and earlier breakdown in MIM structures. It means that annealing is required to decrease the trap density in the dielectric to improve its breakdown strength and lifetime. Nevertheless, ALD demonstrates its capability to deposit high thickness of dielectric and it is promising to develop 3D capacitors that could address the high voltage market.

Related Publications

[1] S. Madassamy, F. Voiron, A. P. Nguyen, A. Lefèvre, G. Parat, D. Buttard, and A. Sylvestre, "Leakage Current and Reliability on Planar High-k Capacitor with Al2O3 Dielectric Deposited by Thermal-ALD", *Materials Research Society (MRS) Spring Meeting*, San Francisco, United States, 2015.

[2] A. Salem, A. Lefevre, A. Rouahi, F. Voiron, F. Jomni, B. Yangui, A. Sylvestre, "Electrical properties of metal-insulator-metal structure based on HfO2-Al2O3 nanolaminate stacks", *Materials Research Society (MRS) Spring Meeting*, San Francisco, United States, 2015.

Frequency Tunable Bulk Acoustic Wave Resonators

Research topics: Tunable Resonators, Lithium Niobate, BAW Resonators

N. Boudou, J.S. Moulet, L. Benaissa, G. Audoit, A. Reinhardt

Partnership: PTA (Upstream Technological Platform)
Sponsorship: Nanosciences Fundation, CNRS Renatech network

Context and Challenges

The increasing complexity of RF front-ends used in mobile phones requires the integration of more and more RF band-pass filters (currently over 40, and up to 200 expected in a near future). Tunable filters are seen as a possible way to reduce this integration complexity and to reduce the number of components to introduce in front-ends. However, demonstrated tunable resonators needed to synthesize tunable filters usually exhibit prohibitive losses, limited tuning range and/or electromechanical coupling factor. We proposed a few years ago a promising concept based on composite bulk acoustic wave resonators made of two stacked piezoelectric films (Fig.1), one acting as a transducer and the other enabling frequency tuning of the whole component through the acoustoelectric effect (change in effective acoustic velocity depending on the electrical boundary conditions applied). So far, we only explored theoretically this solution, but the proof of concept remained to be done.

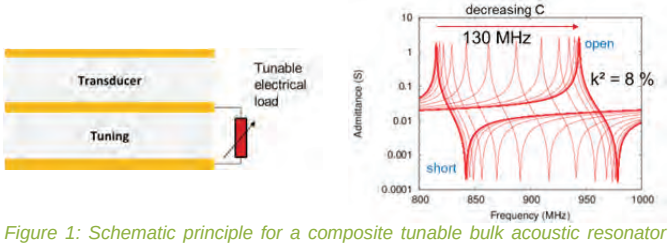

Figure 1: Schematic principle for a composite tunable bulk acoustic resonator (left) and example of simulated electric response for various capacitors connected to the tuning layer (right).

Main Results

In the concept we explore, tunability arises directly from the piezoelectric effect in the "tuning" layer of composite resonators. Hence, a large tuning range requires using a material with large piezoelectric properties. In order to maintain a large electromechanical coupling factor, needed to synthesize a wide bandwidth filter, the "transducer" layer must also be made of a similar material. Therefore, we focused on lithium niobate ($LiNbO_3$) as the piezoelectric material for this application. The most efficient crystal orientation being X-cut, conventional material growth was not possible. Hence, we relied on film transfer techniques such as wafer bonding and thinning to integrate thin films of this material onto silicon substrates. This process was repeated twice and included full sheet tungsten electrodes (Fig.2). Electrical contacts towards these buried electrodes were etched through the piezoelectric film and a top electrode made of Aluminum was sputtered and patterned to define resonator geometry (Fig.3). Resonators were released by etching cavities through the silicon substrate by deep reactive ion etching. The obtained device had two electrical ports, one connected to the transducer film and the other to the tuning film. Electrical measurements were performed and a theoretical capacitor was connected to the tuning port in a circuit simulator during post-processing. Varying the value of this capacitor between short and open circuit conditions allowed to tune the resonance frequency by 1.5 MHz around 204 MHz, in excellent agreement with theoretical expectations when considering the material stack and the resonator geometry [1].

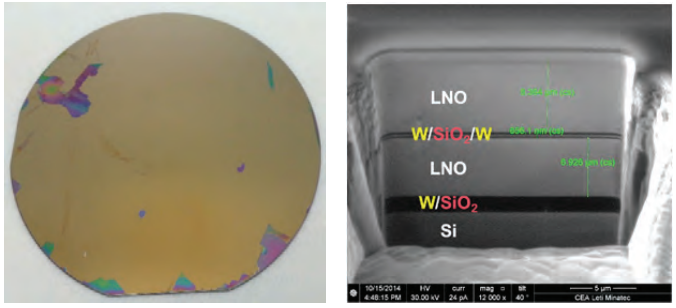

Figure 2: Photograph of a 4" wafer after two successive transfers of a $LiNbO_3$ layer (left) and FIB+SEM cross section revealing the two layers and three buried W electrodes (right).

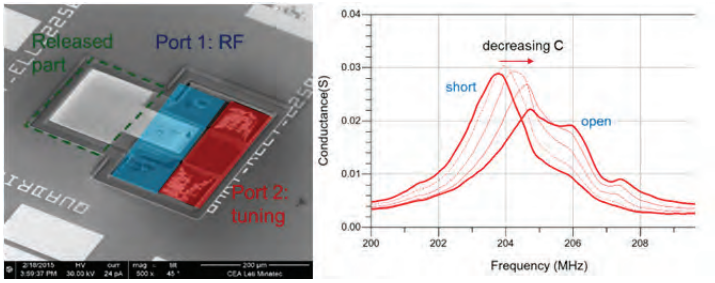

Figure 3: SEM photograph of the fabricated tunable resonator (left) and measurement under various electrical loads applied to the tuning port (right).

Perspectives

We proved the concept of tunable composite bulk acoustic wave resonator based on lithium niobate films. Tuning range, center frequency and quality factors are still limited by the simplicity of the approach taken in the fabrication of this first prototype, therefore future work will be devoted to the optimization of the process and the design of these components to improve resonator performance and tuning range and be able to synthesize a tunable filter.

Related Publications
[1] N. Boudou, J.S. Moulet, L. Benaissa, G. Audoit, A. Reinhardt, "Frequency tuning with lithium niobate composite BAW resonators", *Joint European Frequency and Time Forum and International Frequency Control Symposium*, April 12-16, 2015, Denver, USA.

07

MEMS ACTUATORS & SENSORS & RELIABILITY

- NEMS-Based Mass Spectrometry Goes Neutral and Compact
- NEMS-CMOS Co-Integration
- Resonant MEMS Sensors Based on Piezoresistive Silicon Nanowires
- A 256 MEMS Membrane Digital Loudspeaker Array Based on PZT Actuators
- Effect of Pb Content and Doping on PZT Properties
- Piezoelectric Actuator Based on Thin-Film AlN for Haptic Applications

NEMS-Based Mass Spectrometry Goes Neutral and Compact

Research topics : Nanomechanical Sensing, Mass Spectrometry, NEMS

M. Sansa, G. Gourlat, G. Jourdan, P. Villard, G. Billiot, E. Sage, T. Alava, E. Sage, A. Brenac, C. Masselon, S. Hentz

Sponsorship: CARNOT Funding

Context and Challenges

Of all analytical techniques, Mass Spectrometry (MS) has grown fastest over the past two decades and is now recognized as an essential tool in a variety of fields of modern research. After ionization of the analytes of interest, the spectrum generated is interpreted on the mass-to-charge ratios of the different ions. Routine use of MS in the MDa to GDa range remains challenging as, in this mass range, correct analysis requires a large number of charges per particle. Moreover, it has been estimated that only one analyte ion out of 10^3-10^5 generated at ambient pressure is generally detected. NEMS are ideally suited for sensing in this mass range, but the possibility to perform analysis of neutral species with NEMS-MS was never proven. NEMS-MS had never been compared to a reference measurement as there is no mass standard in this mass range. Moreover, very large scale NEMS arrays would allow ultra-fast analysis, but compact NEMS pixels remained to be demonstrated.

Main Results

A NEMS was placed in a sputtering gas aggregation system (see Fig. 1). Metallic nanoclusters with tunable size and deposition rate can be produced, expelled into vacuum and weighed by either the NEMS detector or a conventional Time-of-Flight (TOF) Mass Spectrometer.

The comparison of the same tantalum cluster population by both NEMS and TOF showed that that NEMS-MS analysis is insensitive to charge state: the spectrum consists of a single peak whatever the species' charge state, making it significantly clearer than existing MS analysis. This simplifies analysis and facilitates identification of the sample. In subsequent tests, all charged particles are electrostatically removed from the beam, and unlike TOF-MS, NEMS-MS can still measure masses (see Fig. 2). This demonstrates directly, for the first time, that NEMS-MS is compatible with analysis of neutral particles[1].

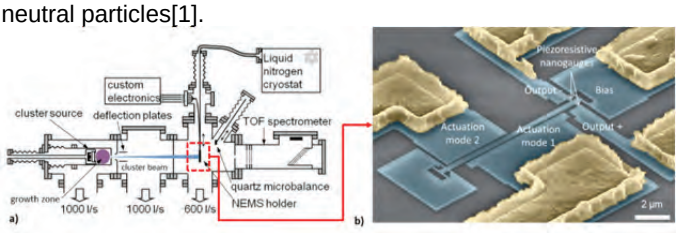

Figure 1: Hybrid setup for TOF-MS and NEMS-MS of nanoparticles.

It is nevertheless very difficult if not impossible to focus a particle beam to the size of a single NEMS device. The implementation of Nanoelectromechanical systems (NEMS) arrays is of importance for fast analysis and good sensitivity. The monolithic co-integration of the NEMS resonators with CMOS circuitry for data processing has potential to achieve a very good density of integration. The factor limiting the density of integration is nowadays the area of the circuitry required to read the response of the resonator, typically much larger than that of the sensor itself. The homodyne self-oscillating scheme is the most straightforward readout scheme but is extremely delicate to handle at high frequencies. Phase-Lock-Loop schemes are more robust but are very area consuming. We have then demonstrated a new topology, using heterodyne self-oscillating loops for multi-mode operation and frequency downmixing through electrostatic actuation. We have shown that it represents a simplified set-up compared to the conventional down-mixing circuit, while it does not change the response of the resonator. We have also demonstrated that the Allan deviation is limited by noise sources coming from the resonator itself, and therefore the circuit does not introduce additional noise or instability. We have also shown the multi-mode capabilities of this topology, by measuring the first two modes of a clamped-clamped beam resonator using a time-multiplexing method with switching times in the order of milliseconds [2-3].

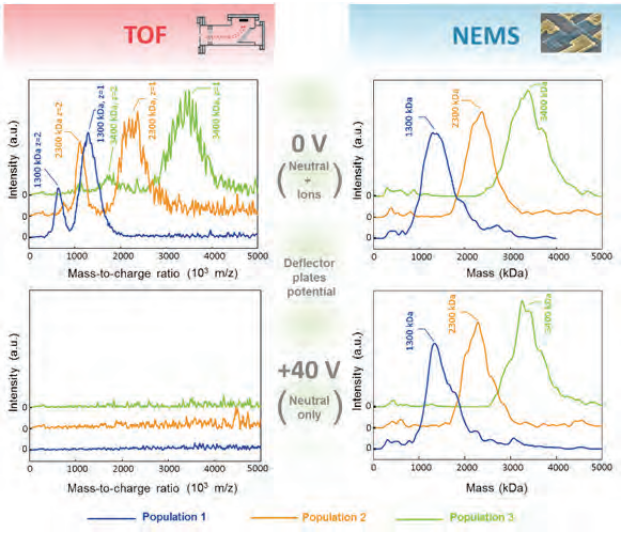

Figure 2: Demonstration of neutral particle Mass Spectrometry.

Perspectives

Combining architectures dedicated to the analysis of neutral particles and ultra-dense arrays of NEMS offers the potential of new analytical capabilities and limits-of-detection several orders of magnitude lower than today's technology. These features could help elucidate unsolved questions in various fields, such as the study of new materials, or easily-dissociated, poorly soluble membrane proteins in structural biology. A similar combination could also be used to monitor nanoparticle levels in the environment and residual diseases in real-time.

Related Publications

[1] E. Sage, A. Brenac, T. Alava, R. Morel, C. Dupré, M. S. Hanay, M. L. Roukes, L. Duraffourg, C. Masselon, S. Hentz, "Neutral particle mass spectrometry with nanomechanical systems," *Nat. Commun.*, vol. 6, p. 6482, 2015.

[2] G. G. Gourlat, M. S. Perna, G. Jourdan, P. Villard, G. Sicard, S. Hentz, "Dual-Mode NEMS Self-Oscillator for Mass Sensing," in *International Frequency Control Symposium 2015*.

[3] M. Sansa, G. Gourlat, G. Jourdan, P. Villard, G. Sicard, S. Hentz, "Compact heterodyne NEMS oscillator for sensing applications," in *ESSDERC 2015*.

NEMS-CMOS Co-Integration

Research topics: NEMS, CMOS, Integration, Sensors

I. Ouerghi, W. Ludurczak, J. Philippe, M. Sansa, M. Gely, C. Tabone, V. Larrey, J. Arcamone, S. Hentz, T. Ernst

Partnership : Applied Materials, LASSE
Sponsorship: ERC Starting Delphins, FP7-NEMSIC, CARNOT Funding

Context and Challenges

Monolithically fabricating both a MEMS or a NEMS device and its readout circuit is extremely appealing for several reasons. Scaling down dimensions also scales down the amplitude of the signals. These signals are more susceptible to parasitics, in particular for resonant NEMS sensing in the 10 to 100MHz range. Also, many applications require dense integration of devices in large arrays. CMOS co-integration is the only viable solution to this complex addressing issue. Moreover, in the case of a vertical integration such as Coolcube for M/NEMS, stacking circuit and mechanical device can be a competitive advantage for footprint reduction of MEMS sensors.

Main Results

Top-down piezoresistive nanoelectromechanical resonators among the smallest resonators listed in the literature were fabricated (see Fig. 1). To overcome the fact that their electromechanical transduction is intrinsically very challenging due to their very high frequency (100 MHz) and ultimate size (each resonator is a 1.2 µm long, 100 nm wide, 20 nm thick silicon beam with 100 nm long and 30 nm wide piezoresistive lateral nanowire gauges), they have been monolithically integrated with an advanced fully depleted SOI CMOS technology [1]. This integration scheme results in a frequency stability of 2×10^{-7}, leading to a limit of mass detection of 1.3 kDa. By advantageously combining the unique benefits of nanomechanics and nanoelectronics, this hybrid NEMS-CMOS device paves the way for NEMS-based mass spectrometry or hybrid NEMS/CMOS logic.

The fabrication of nanoresonators in monocrystalline silicon is a stringent constraint when it comes to NEMS-CMOS integration. We investigated the performance of polysilicon (poly-Si) NEMS fabricated with a low temperature process (laser annealing) compatible with a NEMS above IC 3D integration, in terms of frequency stability, quality factor, Signal-to-Background ratio, as well as piezoresistive and elastic properties [2-4]. Laser annealing conditions and dopant concentration were studied to optimize these features compared to monocrystalline silicon.

Perspectives

Coolcube for NEMS, a monolithic 3D co-integration process above-IC, is particularly adapted to ultra-dense arrays of nanomechanical resonators. Those can be patterned in a polysilicon layer as described above, or in a monocrystalline silicon layer obtained by direct bonding of a SOI wafer [5] on a CMOS substrate. Large arrays of NEMS will next be demonstrated for, for example, mass sensing.

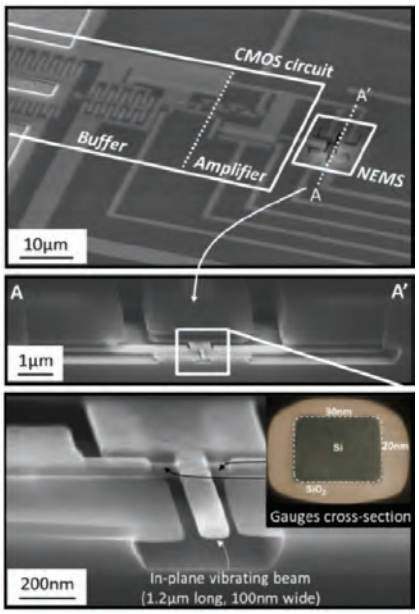

Figure 1: Global overview and zoom-ins of the FDSOI circuit and of the nanoresonator.

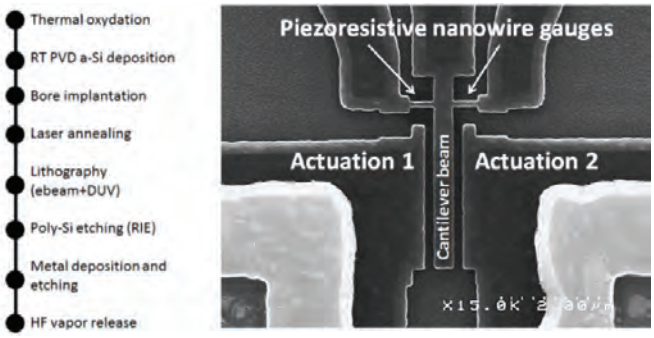

Figure 2 : PolySi NEMS and its fabrication sequence.

Related Publications

[1] T. Ernst, I. Ouerghi, W. Ludurczak, J. Arcamone, L. Duraffourg, E. Ollier, J. Philippe, and S. Hentz, "CMOS and NEMS hybrid architectures," *ECS Trans*., vol. 69, no. 10, pp. 253–8, 2015.

[2] I. Ouerghi, M. Sansa, W. Ludurczak, L. Duraffourg, K. Benedetto, P. Besombes, T. Moffitt, B. Adams, D. Larmagnac, P. Gergaud, C. Poulain, A. I. Vidaña, C. Ladner, J. M. Fabbri, D. Muyard, G. Rodriguez, G. Rabille, O. Pollet, P. Brianceau, S. Kerdiles, S. Hentz, and T. Ernst, "Polysilicon Nanowire NEMS fabricated at low temperature for above IC NEMS mass sensing applications," in *IEEE International Electron Devices Meeting*, 2015.

[3] I. Ouerghi, J. Philippe, C. Ladner, P. Scheiblin, L. Duraffourg, S. Hentz, T. Ernst, "A nanowire gauge factor extraction method for material comparison and in-line monitoring," in *IEEE MEMS*, 18-22 January, 2015, pp. 17–20.

[4] I. Ouerghi, W. Ludurczak, L. Duraffourg, C. Ladner, A. I. Oudrhiri, P. Gergaud, M. Vinet, and T. Ernst, "Piezoresistive transduction optimization of p-doped Poly-silicon NEMS," in *European Solid-State Device Research Conference, 2015*, no. 120, pp. 17–20.

[5] W. Ludurczak, V. Larrey, O. Girard, F. Fournel, R. Crochemore, M. Gély, C. Tabone, I. Ouerghi, T. Ernst, S. Hentz, "Wafer to wafer bonding for 3D monolithic co-integration of NEMS above CMOS back-end," in *Waferbond*, 2015.

Resonant MEMS Sensors Based on Piezoresistive Silicon Nanowires

Research topics : Resonant Sensing, Silicon Nanowires, Pressure Sensor

G. Lehée (SAGEM), Y. Deimerly, P. Rey, A. Berthelot, F. Souchon, J.-C. Riou (SAGEM), A. Bosseboeuf (CNRS-IEF), G. Jourdan

Partnership: SAGEM Défense Securité, Safran Group
Sponsorship: FP7-NIRVANA

Context and Challenges

Resonant MEMS sensors have the ability to turn a physical parameter (pressure, acceleration, etc.) into a resonance frequency shift of a mechanical mode. The measurement process consists in actuating a mechanical resonator around its resonance peak and sensing the response modifications, such as resonance frequency, to benefit from the outstanding sensitivity of resonators to external stimuli. This type of sensor is suitable for high performance applications such as pressure sensors, accelerometers, since they usually offer high resolution sensing and excellent long term stability. In this context, MEMS resonators based on piezoresistive silicon nanowires have been studied to evaluate their potentials as resonant sensors. A noticeable advantage is that P-doped silicon ($5.10^{19}cm^{-3}$) piezoresistive nanogauges do not suffer from leakage currents since they are suspended and then electrically isolated. This property makes silicon nanowires based sensors appropriate for high temperature applications, as required in aeronautic or automotive fields.
Elsewhere, some recent works at Leti [1,2] focused on damping processes that occur in nanowires and then on the impact of the resulting quality factor Q on frequency resolution.

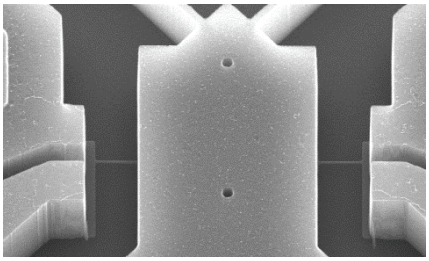

Figure 1: SEM picture of nanowires anchored to a MEMS resonator.

Main Results

Silicon nanowires can have a strong impact on the mechanical response of a MEMS resonator. Despite their tiny dimensions ($250 \times 250\ \mu m^2 \times 5\mu m$) compared to the whole MEMS (larger than $100 \times 100 \times 10\mu m^3$), [1] showed that nanowires dominate the resonance frequency of the device and most of all limit its quality factor when operating under high vacuum without air damping. By comparing the mechanical response of various devices, nanowire behavior has been modeled as a damped spring, in compliance with experimental results depicted in Fig.2 obtained for various gauge positions along a given resonator design. Several damping mechanisms have been investigated such as flexural and longitudinal thermoelastic damping that couples mechanical strain to temperature field for flexural and longitudinal nano beam motions. As a result, quality factors of nanowires based MEMS can be anticipated and optimized to meet high performance sensor specifications.

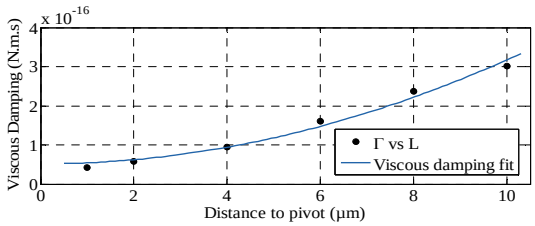

Figure 2: Viscous damping coefficient for various gauge positions associated to a MEMS resonator exhibiting a motion of rotation. The damping coefficient increases when the gauges move away from the pivot point since nanowires increasingly extend.

This parameter strongly affects the frequency resolution of a resonant MEMS sensor as studied in [2], where resonance frequency fluctuations have been investigated at various time scales. Silicon nanowires have here an excellent displacement sensitivity due to their tiny cross-section. This is a prerequisite to obtain very high signal to noise ratio up to 115 dB above a few kHz, limited by thermomechanical noise, and then to achieve excellent frequency resolution, which has been shown to be inversely proportional to Signal to Noise Ration and quality factor. Frequency resolution of only 40 ppb at short time scale (0.1s) has been obtained (Fig.3) and complies with the frequency noise model presented.

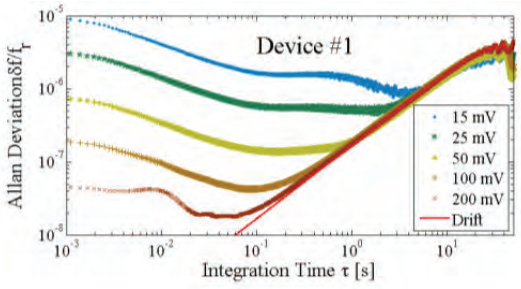

Figure 3: Allan deviation of a nanowire based resonator for various actuation amplitudes (increasing SNR).

Perspectives

Silicon nanowire based mechanical devices are suitable for resonant sensing applications thanks to their large sensitivity and high frequency resolution. This concept has been implemented in a resonant pressure sensor currently under fabrication. Based on the results obtained in 2015, a resolution of 1 Pa is expected for a 10 bar full scale pressure sensor.

Related Publications
[1] G. Lehée, Y. Deimerly, P. Rey, A. Berthelot, J.-C. Riou, A. Bosseboeuf, G. Jourdan, "Damped spring model of a piezoresistive silicon nanowire coupled to a low frequency MEMS resonator". *26th MME Workshop*. Toledo Spain 2015.
[2] G. Lehée, F. Souchon, J-C. Riou, A. Bosseboeuf, G. Jourdan "Transduction performance of piezoresistive silicon nanowires on the frequency resolution of a resonant MEMS sensor", *IEEE Sensors. Busan Korea* 2015.

A 256 MEMS Membrane Digital Loudspeaker Array Based on PZT Actuators

Research topics: Piezoelectric, Thin-Film, PZT, Loudspeaker

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R. Morisson (Easii-IC), Y. Bohard (Easii-IC), JP. Goglio (Easii-IC), J. Escato (FOCAL), S. Fanget

Partnership: INSA, FOCAL, Easii-IC
Sponsorship: FUI-SONAT

Context and Challenges

A Digital Loudspeaker Array (DLA) is an electromechanical transductor which receives a numerical signal as input data and allows the analogical conversion directly in the air. Developing DLA on silicon micro technology allows the fabrication of very thin and directive loudspeakers that is very useful for consumer electronics. For this purpose, we designed high performances PZT actuated membranes deposited by sol-gel method over a polysilicon layer to generate higher acoustic pressure as possible. We report here MEMS loudspeakers and the demonstration of digital acoustic reconstructions using low actuation voltage.

Main Results

Through a mixt Finite Element Method (FEM) and analytical study, we designed high performances PZT actuated membranes. We focused on membranes (radius R = 1300 µm) which theoretically present a resonant frequency of 18 kHz. Due to the ferroelectric properties of PZT, we implement a double-actuator design able to generate positive or negative acoustic pulses (Fig. 1).

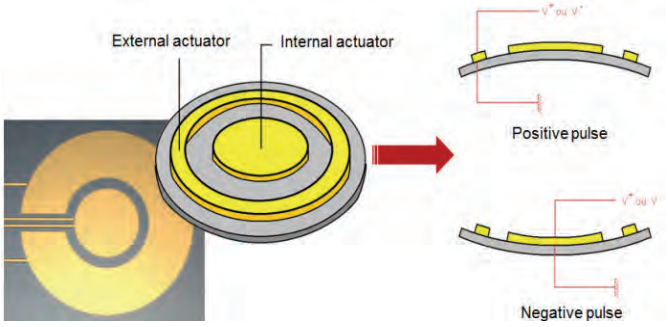

Figure 1: Thin-film PZT actuated membrane schematic view. The double actuator design allows to obtain positive and negative acoustic pulses.

We used a generic technology to build demonstrators, compatible with RF MEMS or haptic interfaces. Devices were manufactured out of 200 mm standard silicon wafers. First the structural layer was deposited (1.9 µm silicon-oxide and 4 µm poly-silicon). Then we deposited and etched the piezoelectric stack (Fig. 2-a). It consists of 2 µm thick sol-gel PZT in between 200 nm thick Pt bottom electrode and 100 nm thick Ru top electrode. Then, membranes were released by back side etching the substrate. Finally, we sawed the substrate to obtain individual ultra-thin DLA, presenting a thickness finer than 735 µm (Fig.2-b). In parallel, an electronic board was design and manufactured using discrete components.
Electromechanical characterizations were performed on MEMS-DLA and prove that the implemented design allows obtaining quite symmetric positive and negative pulses.

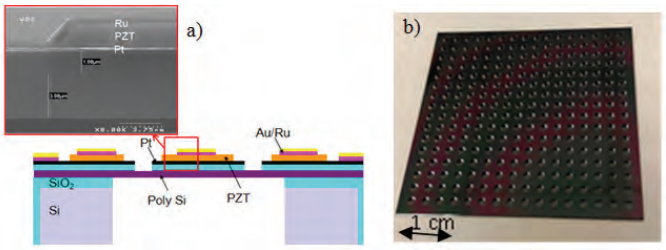

Figure 2: (a) Schematic cross section of the technological stack and SEM cross section of the sol-gel thin film PZT actuator and (b) Photography of a 256 MEMS membrane DLA (6×6 cm²).

Acoustic characterizations were also performed on 256 membranes MEMS-DLA. We measured the response spectrum of the DLA playing in the digital reconstruction mode a 5.5 kHz sinus with a sampling rate of 44.1 kHz. It shows a satisfying SPL value of about 100 dB at 13 cm (Figure 3) [2]. The acoustic pressure generated by the MEMS-DLA in its analogic mode was also investigated using an actuation voltage of only 8 V. We compare the acoustic pressure measured by a microphone placed 13 cm face to our MEMS-DLA, with the acoustic pressure of a 64-membranes MEMS-DLA [1] when we play a sinus with frequency ranging from 500 Hz up to 50 kHz. It shows an acoustic pressure increase of about 40 dB, coming from membrane surface and number increase but also actuator optimization. Sounds audible as far as several meters from the loudspeaker have been generated.

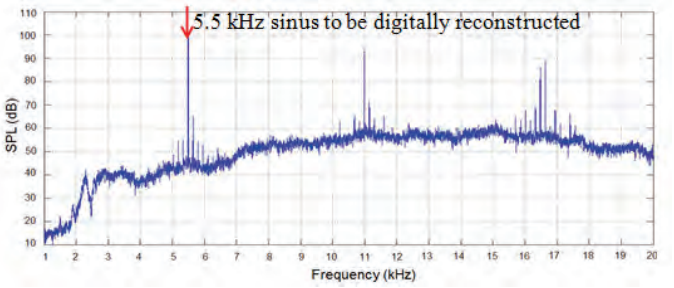

Figure 3: Response spectrum of the 256-MEMS DLA (R = 1300 µm) playing in digital mode a 5.5 kHz sinus.

Perspectives

Electromechanical and acoustic characterizations were reported on a 256 MEMS membranes DLA based on PZT actuators. Digital acoustic reconstructions using our MEMS-DLA have been demonstrated using low actuation voltage. The sound quality is still to be improved by reducing distortion and noise. It can be done by reducing the discrepancy between individual membrane responses. These results are promising for the development of ultra-thin DLA.

Related Publications
[1] S. Fanget *et al.* « MEMS digital loudspeaker based on thin-film PZT actuators", *International congress on Ultrasonics*, 2015.
[2] F. Casset *et al.* «A 256 MEMS membranes digital loudspeaker array based on PZT actuators », *29th International Conference on Solid-State Sensors, Actuators, Microsystems, Transducers* (Eurosensors), 2015.

Effect of Pb Content and Doping on PZT Properties

Research topics: Piezoelectric Thin Film, Actuators, Dielectric, Capacitors, PZT, Surface, Interface, Doping

G. Le Rhun, I. Gueye, S. Pelloquin, W. Benhadjala, Ch. Dieppedale, C. Bonnard, J. Guillaume, Ph. Renaux, H. Sibuet P. Gergaud, O. Renault, E. Defay (LIST), N. Barrett

Partnership : STMicroelectronics
Sponsorship: PIA-TOURS2015

Context and Challenges

Lead zirconium Titanate Pb(ZrxTi1−x)O3(PZT) is widely used in applications such as microelectromechanical systems (MEMS), piezoelectric actuators, infrared pyroelectric detectors, and decoupling capacitors. Capacitor device performances in particular are determined not only by the bulk dielectric properties, which depend on the stoichiometry, the doping and the manufacturing process but also by the interface with the electrodes. Sol–gel synthesis is well adapted for mass production of PZT but lead loss produced during the necessary crystallization annealing requires excess lead precursor for obtaining the near stoichiometric values. This may also lead to changes in surface composition and hence modifications of the PZT/electrode interface chemistry. Surface phases have been observed, which appear dependent on the excess Pb content and growth process. However, little is known about their chemistry and even less regarding their effect on device performance. Here we look at the effect of Pb content on PZT surface state, as well as the effect of doping on PZT capacitors properties.

Main Results

In sol–gel synthesis, excess lead precursor is used to maintain the target stoichiometry. Surface nanostructures appear at 10% excess (PZT10) whereas 30% excess (PZT30) inhibits their formation (Fig.1).

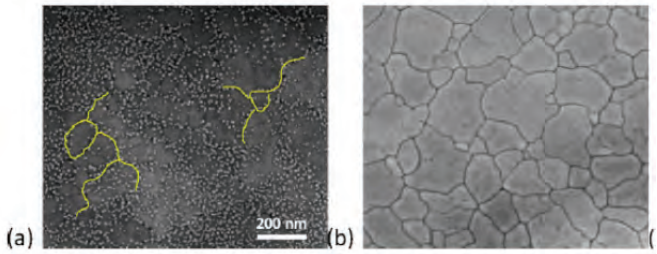

Figure 1. SEM top view images of (a) PZT10 as deposited, (b) PZT30.

We investigate the role of lead excess on the surface composition, chemistry and micro-structure of PZT thin films. In particular, we exploit the surface chemical sensitivity of XPS to identify the chemistry of the secondary surface phase observed on PZT10. Using the surface-sensitive, quantitative X-ray photoelectron spectroscopy and glancing angle X-ray diffraction (Fig.2), we have shown that the chemical composition of the nanostructures is ZrO1.82−1.89 rather than pyrochlore often described in the literature [1]. The presence of such interfacial layer in the PZT MIM capacitor results in a decrease of global capacitance value (-8%).

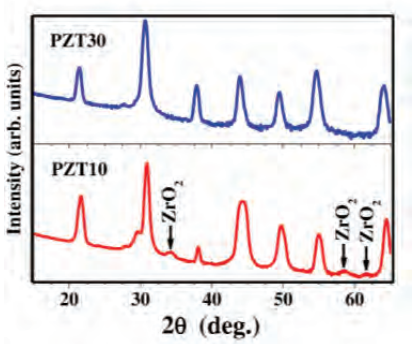

Figure 2. XRD scans at grazing incidence of PZT10 (bottom, red) and PZT30 (top, blue).

The effect of doping (La, Nb and Mn) of PZT films, in the range of 0 – 4 at%, on both capacitance and breakdown voltage values has also been investigated. Lanthanum substitutes the Pb ions in the A site of the perovskite ABO3, whereas Niobium and Manganese substitute Ti or Zr in the B site. Surface capacitance (Cs) was determined from CV measurements. Breakdown voltage (BV) was statistically obtained using a Weibull law of reliability by analyzing Linear Ramp Voltage Stress measurements results. Table 1 gathers the measurements results for optimal percentage of each dopant found. It also shows the variation (in %) of Cs and BV compared to the reference undoped PZT capacitor. We have shown that both surface capacitance and breakdown voltage can be enhanced by doping with either La or Nb.

	PZT 220nm			
dopant (optimal %)	None	La (2.5%)	Nb (2%)	Mn (2%)
Cs (nF/mm²)	41	46 (+12%)	47.5 (+16%)	40 (-2.5%)
BV (V)	43	48 (+12%)	57 (+32%)	56 (+30%)

Table 1: Evolution of Cs and BV with doping.

Perspectives

The presence of a possibly discontinuous layer of wide band gap ZrO1.82−1.89 could be of importance in determining the electrical properties of PZT-based metal-insulator-metal heterostructures. In addition an excess of Lead in PZT films could result in early breakdown of the capacitor. This is under current investigation in order to eventually fine tune the lead content in PZT films. As for doping, we are studying the effect each dopant on PZT piezoelectric properties.

Related Publications
[1] I. Gueye, G. Le Rhun, P. Gergaud, O. Renault, E. Defay, N. Barrett, "Chemistry of surface nanostructures in lead precursor-rich PbZr0.52Ti0.48O3 sol-gel films", *Applied Surface Science*, Vol. 363, pp. 21-28, 2015.
[2] G. Le Rhun, S. Pelloquin, I. Gueye, W. Benhadjala, C. Dieppedale, J. Guillaume, P. Renaux and H. Sibuet. "Optimization of PZT dielectric properties by doping with La, Nb or Mn elements", *Joint ISAF-ISIF-PFM Conference*, Singapore, 24-27 May 2015.

Piezoelectric Actuator Based on Thin-Film AlN for Haptic Applications

Research topics: Piezoelectric Thin-Film, AlN, MEMS Actuators, Haptic

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Partnership: Hap2U, TIMA
Sponsorship: FUI-Touch It

Context and Challenges

Recent demand in new tactile interfaces in many customers' application such as Smartphones or tablet PCs, has focused research efforts towards developing high performances transparency haptic interfaces. Among the different haptic solutions, squeeze-film effect is one of the most promising. It provides high granularity level of haptic sensation, playing with the variable friction between a finger and a resonant haptic plate, when the plate displacement amplitude (PDA) reaches about 1 µm in a flexural anti-symmetric Lamb mode [1]. To promote it, we use piezoelectric actuators and bimorph effect. To address transparency, low temperature process was used to deposit AlN actuators directly on transparent glass substrate [2]. We report here on the design and the characterization of thin-film AlN actuated haptic plates.

Main Results

We designed high performances thin-film AlN actuated haptic plates using Finite Element Method (FEM) approach implemented inside CoventorWare® tool. Our model consists in the study of unclamped 700 µm thick plates made of glass (EAGLE XG®) with 2 µm thick AlN actuators. We neglected top and bottom electrodes on both sides of the AlN layer due to their low impact on the plate displacement amplitude (PDA). Modal simulation performed on a 110 × 65 mm² plate gives the frequency of the desired mode, namely 24.68 kHz. We accurately positioned the actuators by taking the deformed shape of the mode into account, and matching the actuators' position with the maximum PDA. The complete implementation can be observed in Fig. 1. One can note that different actuation configurations are possible [3].

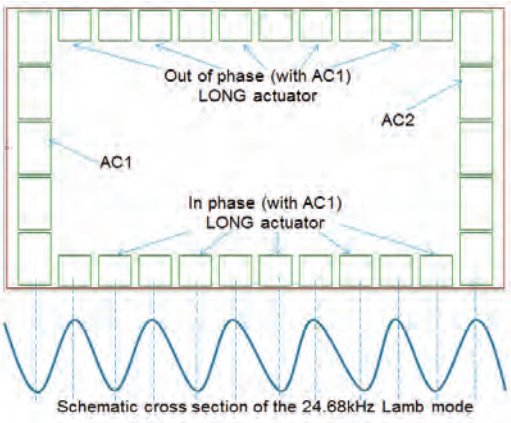

Figure 1: Optimum design for the 24.68 kHz Lamb mode obtained on the 110×65 mm² glass plate.

AlN-based devices were manufactured out of 200 mm glass substrates. The piezoelectric stack consists of 2 µm thick AlN in between 200 nm thick Molybdenum bottom electrode and 200 nm thick Molybdenum top electrode. Then we deposited and patterned a passivation silicon oxide layer followed by gold lines and pads. Fig. 2 gives a schematic view of the technological stack. Finally, we sawed the glass substrate to obtain individual plate.

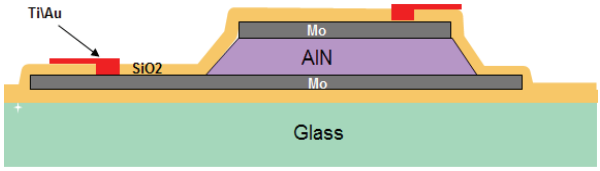

Figure 2: AlN-on-glass schematic technological stack cross section.

Optical measurements of 110×65 mm² AlN-actuated vibrating plates were also performed using laser vibrometry (POLYTEC®). In particular, the PDA regarding the actuation configuration was measured and compared to simulation. A micrometric displacement can be obtained using various actuator configurations, as expected. In particular, a PDA of 1.7 µm is measured using +/-60 V and all the actuators. Fig. 3 shows that a good agreement is observed between simulation and measurement.

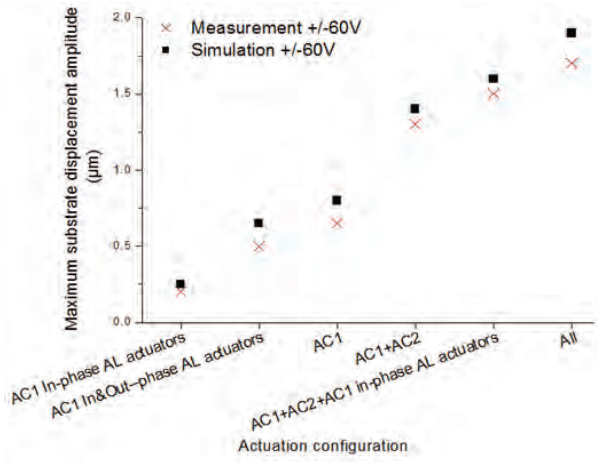

Figure 3: Comparison of the measured and the simulated (damping parameter = 7.10-8) PDA of the 110 × 65 mm² plate under ±60 V.

Perspectives

Transparent haptic interfaces based on AlN-actuators deposited above glass substrate were designed, built and characterized. Micrometric PDAs were measured whereas a weak haptic effect was felt under 60V. This small haptic sensation is under investigation to make possible the 110 × 65 mm² plate integration in a thin-film haptic demonstrator in a close future.

Related Publications

[1] M. Wiertlewski, JE. Colgate, "Power optimization of ultrasonic friction-modulation tactile interface", *IEEE Transaction on haptics*, vol. 8, n° 1, 2015, pp. 43-53.
[2] F. Bernard, M. Gorisse, F. Casset, C. Chappaz, S. Basrour, "Design, Fabrication and characterization of a tactile display based on AlN transducers", *European Conference on Solid-State Transducers (Eurosensors)*, 2014, pp. 1877-7058.
[3] F. Casset, JS. Danel, C. Chappaz, F. Bernard, S. Basrour, B. Desloges, S. Fanget, "Design of thin-film AlN actuators for 4-inch transparent plates for haptic applications", *Int. Conf. on Thermal, mechanical and multi-physics simulation and experiments in microelectronics and microsystems (Eurosime)*, 2015.

08

3D INTEGRATION & PACKAGING

- Advanced 3D-Technological Bricks: State-of-the-Art Developments for Future Industrial Applications
- CMP: Enabling the Third Dimension
- Thermal Management
- Hermiticity and Biostability of Packaging for Medical Implantable Microsystem Devices
- Nanopackaging, Innovative Interconnection Solutions at Nanoscale

Advanced 3D-Technological Bricks: State-of-the-Art Developments for Future Industrial Applications

Research topics: 3D Integration, Direct Bonding, Bonding

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Partnership: STMicroelectronics, ShinEtsu Chemical corp., CNRS-IM2NP, UJF-SIMaP, Sherbrooke University-C2MI
Sponsorship: IRT Nanoelec.

Context and Challenges

3D-IC packaging has been extensively developed to meet form factor and low power consumption demands driven by new semiconductor markets. To ensure the success of these future products some associated technological key challenges are addressed in LETI since early 2000.
Among them, stress/deformation management of the silicon interposer as well as finding solutions to increase the top/bottom die interconnection density are critical. Therefore, the purpose of this paper is to firstly present our interposer stress management strategies recently obtained as well as present our work regarding hybrid bonding technologies optimization and qualification.

Main Results

Stress management strategy: Experimental die-level curvature has been measured using shadow moiré interferometry during complete thermal cycle. Finite element modeling aims at understanding the curvature behavior observed experimentally and to propose warpage compensation strategies (Fig.1). It has been found that back-side dielectrics deposited at low-temperature have a critical impact on die curvature magnitude, compared to other layers typically found in Si interposer. Experiments carried out on
Si-bulk and SOI substrates have shown that: in the case of SOI substrates, optimized compressive stress regime in the BS layers counteracts the residual stress in front-side layers, especially the compressive stress of the BOX alone. Finally, we demonstrated that optimized BS SiN/SiO2 stack can be implemented to adjust the stress induced by the FS layers [1].

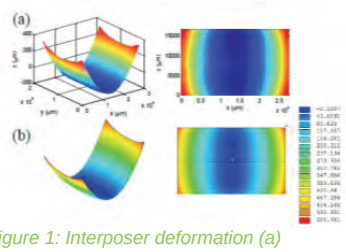

Figure 1: Interposer deformation (a) Thermoiré measurement (b) and FEM simulation.

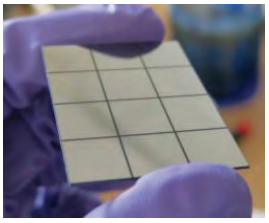

Figure 2: Pictures of Interposer–like dies with planarization polymer.

Emerging materials required to facilitate interposer realization, could also have an impact on interposer stress and then electrical performances. Therefore a second study has been driven this year in order to evaluate the compatibility of silicon-based wafer-level molding material with the whole interposer flow (filling & grinding capacities as well as induced deformation on 300mm wafers populated with 1x1cm dies presenting 500µm thickness – Fig.2) and then evaluate its impact on electrical performances of simplified silicon interposer (100µm thickness) mounted on BGA [2]. We demonstrated that this material does not affect the environmental reliability performances of thinned interposer and can even extend the mechanical resistance of packages thanks to adapted elastic properties. Next step is now to integrate such materials and strategy in active 3D devices.

Direct Hybrid bonding: This technology is quite promising for 3D industry because it enables very high interconnection densities compare to standard thermocompression packaging technologies. We have optimized surface preparation process in order to enable 200mm wafer to wafer bonding while each wafers presented 6 levels of BEOL (Fig.3). Dimension of patterns at the interface (line and pads) range from 5 to 24µm. After bonding, wafers have been baked at 400°C to ensure proper copper grain reconstruction. Additionnaly to that, electromigration experiments have been carried out highlighting that in the case of direct bonding, the voiding mechanisms is similar to the known damascene architecture, confirming excellent copper reconstruction (Fig.4). This work will be rapidly applied to 3D advanced imagers with direct assembly of BackSideIlluminated wafers on the Display Processor.

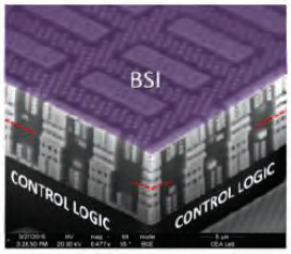

Figure 3: SEM images (TOP view, 3D view) of the 3D assembly including all metal levels of the BSI imager structure. (Dashed lines highlight bonding interface).

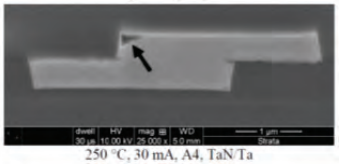

Figure 4: Example of electromigration failure in copper/oxide direct bonding: copper/barrier depletion.

Related Publications
[1] B.Vianne, A.Farcy, V.Fiori, P.Chausse, N.Chevrier *et al*., "Stress Management Strategy to Limit Die Curvature During Silicon Interposer Integration", *Proceeding of 3DIC 2015 Conference*.
[2] A.Jouve, Y.Sinquin, A.Garnier, H.Kato *et al*., "Silicon based Dry-Films Evaluation for 2.5D and 3D Wafer-level System Integration improvement", *Proceeding of 3DIC 2015 Conference*.
[3] L. Benaissa, L. Di Cioccio, Y. Beilliard, P. Coudrain *et al*., "Next Generation Image Sensor via Direct Hybrid Bonding", *Proceeding of EPTC 2015*.
[4] S. Moreau, Y. Beilliard, P. Coudrain, D. Bouchu, L. Di Cioccio, L. Arnaud, "Electromigration in Hybrid Bonding Interconnects for 3-D IC, Impact of the diffusion barrier", *Proceeding of EPTC 2015*.

CMP: Enabling the Third Dimension

Research topics: 3D Integration, Direct Wafer Bonding, CoolCube™, 3D Gates

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Partnership: STMicroelectronics
Sponsorship: IRT 3D

Context and Challenges

For the past 50 years, semiconductor industry inexorable quest to cost reduction drove integrated circuits miniaturization and provided increased transistor density and performances. If transistor shrinking to follow Moore prediction seems to hit an end, solution is transistor stacking, going from 2D to 3D paradigm [1]. In 2D technology, lithography scaling down was enabled by introducing the chemical-mechanical planarization process in semiconductor manufacturing. Today, stacking and going up to 3D is CMP-enabled, whether we are talking about 3D transistors, CoolCube™ monolithic 3D IC, or 3D stacked IC through wafer direct bonding (Fig.1).

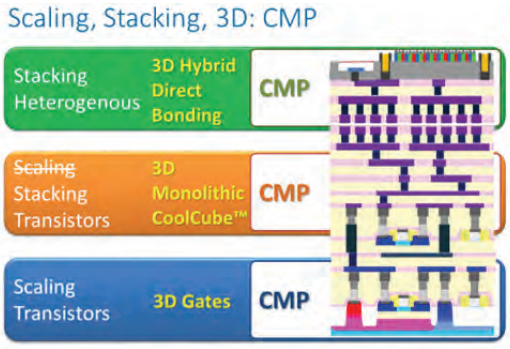


Figure 1: New CMP steps required for 3D applications: 3D gates, CoolCube™ 3D monolithic integration and 3D Hybrid Direct Bonding.

Main Results

At Leti we developed new CMP processes in order to address the 3D applications [2]. For 3D gates, polysilicon planarization on top of fins is required with excellent control of final thickness (Fig.2). Careful benchmarking of slurries and pads was done in order to select best planarization performances. As we stop in polysilicon film, with no help of special stopping layer, thickness variation control across wafer was obtained by developing special endpoint using advanced close-loop control and with in-situ pressure adjustments.

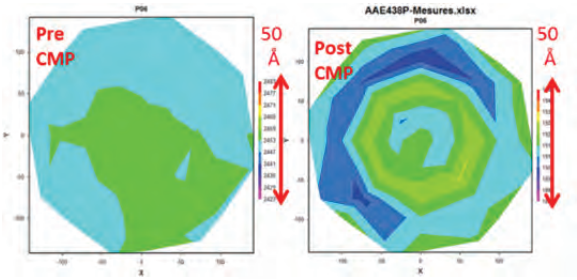


Figure 2: Polysilicon planarization on top of FINS for 3D gates: pre and post CMP film measurement showing excellent thickness control.

Final post-CMP thickness range was same order as pre-CMP range: 5nm across 300 mm diameter (Fig. 2).
For CoolCube™ monolithic integration of stacked transistors, direct wafer bonding requires excellent planarization efficiency at device to die scale but also, excellent film thickness control – diameter planarization. Optimized CMP process showed perfect planarization across different device size and densities allowing excellent bonding quality, with controlled dielectric thickness between the two stacked transistors levels (Fig. 3).

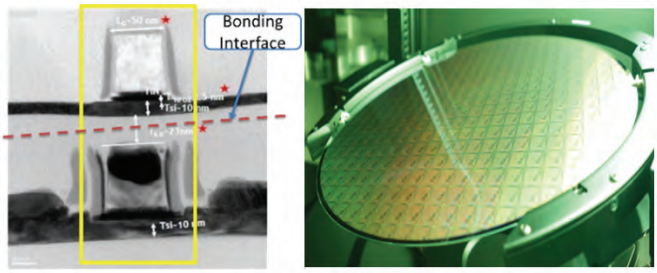


Figure 3: CoolCube™ monolithic integration by transistor stacking by wafer bonding.

Concerning 3D Hybrid Direct Bonding the key is to have very flat and very smooth surfaces of both oxide and copper pads. Improved damascene CMP process we developed at LETI allows us to obtain excellent planarization at different involved spatial wavelengths, from device to die scale. (Fig.4). Moreover, copper pads roughness was addressed through optimized CMP step and reduced below 0,5nm RMS. This allowed excellent copper pad bonding and, therefore excellent electric properties (Fig. 4).

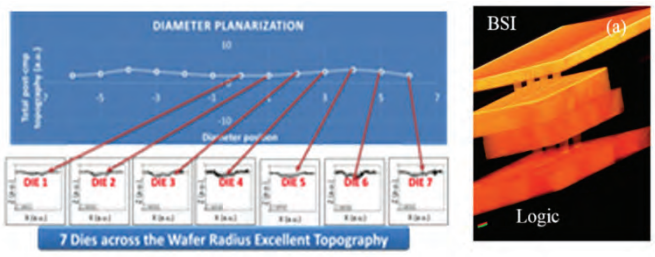


Figure 4: Improved copper CMP process showing excellent device to diameter planarization (left side); 3D FIBSEM analysis of single element of a 30k daisy chain (pad size 4.4µm)

Perspectives

The increased costs of lithography steps and wafer processing in general at the next-generation silicon nodes are driving the industry to find alternatives to improve the performance and functionality of our electronic devices, lower the cost, reduce power consumption. Additionally, the need to integrate disparate technologies (logic, memory, RF, sensors, etc) in small form factors is driving the industry to 3D integration as a solution. Going up and using third dimension needs perfect planarization of stacked layers so CMP is key enabling process. Therefore, further work shall be done in understanding and improvement of planarization performances of CMP consumables – pads and slurries, in parallel with developing robust endpoint algorithms.

Related Publications
[1] H. Metras *et al.*, "Going up! Monolithic 3D as an alternative to CMOS Scaling", online at http://www.advancedsubstratenews.com/
[2] V. Balan *et al.*, "CMP – 3D Enabler", *2015 International Conference on Planarization/CMP Technology (ICPT)*, Chandler, AZ, USA, 2015 (invited paper)

Thermal Management

Research topics: Thermal Management, Heat spreader, Micro-fluidics

J.P. Colonna, P. Coudrain, L-M Collin, R. Prieto, S. Cheramy

Partnership: STMicroelectronics, Sherbrooke University, G2ELab
Sponsorship: IRT Nanoelec

Context and Challenges

The microelectronics sector is facing many challenges to produce smaller and more performant computing chips. Thermal management accounts for one of them, especially in the context of modern packaging trends such as flip chip and 3D stacking, and considering the ever increasing power densities. In addition to increased cooling needs, applications like mobile devices tend to reduce the space available for heat dissipation. In this context, Leti has developed a set of test chips dedicated to thermal studies, with multi-scale objectives covering microscopic design to macroscopic packaging studies. A conjugate approach of experimental measurements coupled with FEM simulations has been systematically set up to provide predictive models and assess technological optimizations. They have been first employed to investigate dissipation in TSV-based three-dimensional ICs (3DIC). Technological developments have been focused on heat spreaders benefits in single flip-chip and 3DIC packages, and have shown large opportunities for performance improvement. Fluidic cooling using microchannels is also under investigation for higher power applications.

Main Results

Among different Leti thermal test chips, the "Wioming" System-on-Chip includes 8 heaters and 7 thermal sensors and can be integrated in a standalone version, stacked with a Wide I/O memory or stacked on itself (3D-NoC) [1]. Copper and carbon-based heat spreaders have been tested on this test vehicle in a standalone "die exposed" flip-chip configuration as shown in the figure below [2].
Experimental results in the figure below show the temperature reduction for two sizes of graphite heat spreader, die or package area. These results were then retro-simulated and the thermal path analyzed, with or without heat spreader. The vertical heat flux (W/m²) at the silicon top surface is shown for the 3 configurations in the figure below. It shows a complete redistribution of the heat flux with a heat spreader: heat is "pumped" from the hotspot into the graphite sheet, spread and then goes back into the coldest area of the package including the molding.

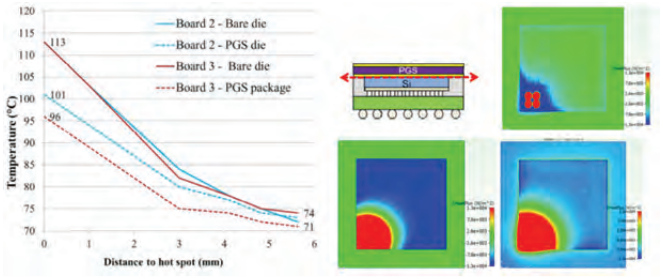


Figure 1: Left: 2.13Watts hotspot temperature for different heatspreader surface – right: retro simulated heat flux in Z-axis [2].

As a result, Graphite sheets exhibit a better thermal performance than copper, especially for hotspot mitigation. Beside, carbon-based materials have the advantage of a coefficient of thermal expansion (CTE) more similar to that of silicon. This allows decreasing the thickness of the interface material, which in turn improves thermal benefits of the heat spreader.
The same test chip has been used to evaluate the impact of microchannel cooling in a flip chip and a 3D assembly of two stacked chips with localized heat sources. This simulation study has been performed with a hybrid analytical / FEM approach (Matlab/Comsol) [3].

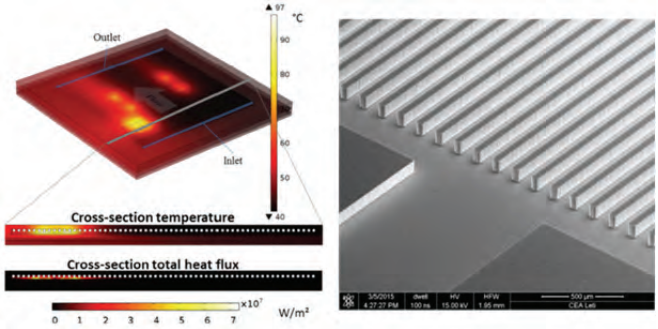


Figure 2: Left: microchannels simulation dissipating 16W with 60 microchannels of 125 µm deep and 75 µm wide (flow rate 0.75 cm³/s) – right: microchannels processed by DRIE [4].

Results indicate that increasing the flow rate is not as beneficial as increasing the number of channels (with constant total cross-section area). The effect of heat spreading was also found to be critical, favoring thicker dies. However, when switching to 3D chip configuration, the underfill layer drastically increases the total thermal resistance and must be considered for thermal design.

Perspectives

The experimental measurement of microchannels cooling is currently underway. New packaging approaches are also tested, in order to achieve a satisfying compromise between thermal efficiency of microchannels and their integration cost. The next study will be the integration of a two-phase cooling system in the same environment.
New 3D test chips are also under investigation to assess performance improvement in the perspective of new applications including patterned heat spreaders.

Related Publications
[1] P. Coudrain *et al.*, "Experimental Insights into Thermal Dissipation in TSV-Based 3D Integrated Circuits", *IEEE Design and Test,* Issue: 99, 2015.
[2] R. Prieto *et al.*, "Thermal measurements on flip-chipped system-on-chip packages with heat spreader integration", *Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)*, 2015.
[3] L-M. Collin *et al.*, "Modeling conjugate heat transfer in 3D microelectronics with embedded microchannels using a hybrid analytical and finite element method", *13th International Conference on Nanochannels, Microchannels, and Minichannels (ASME)*, 2015.
[4] P. Coudrain *et al.*, "Thermal management in Compact system – From wishes to implementation", *THERMINIC Workshop*, Paris, Sept 2015.

Hermiticity and Biostability of Packaging for Medical Implantable Microsystem Devices

Research topics: Medical Devices, Bio-Packaging, Microsystem

J.-C. Souriau, G. Simon, L. Castagné, K. Amara (LivaNova Sorin CRM), P. D'hiver (LivaNova Sorin CRM), B. Boutaud (LivaNova Sorin CRM)

Partnership : Sorin CRM SAS

Context and Challenges

Facing demographic aging and surging demand for advanced healthcare, the global market for active medical devices has greatly expanded these last years. Furthermore, microsystem improvement in term of miniaturization offers fascinating perspectives for medical applications. A prerequisite for the development of devices packaging is to preserve the human body from toxic elements exposure. Moreover, electronics parts need to be preserved from corrosive substances for functionality and reliability.

The development of an innovative packaging solution of silicon device for cardiac medical applications was proposed by the Leti and Sorin. A hermetic and low profile silicon box which allow to encapsulate electronics components such as ASIC and Mems accelerometer was developed and manufactured. The gas content and hermeticity of the package were analyzed using Residual Gas Analysis and the degradation of packaging was tested in a saline solution.

Main Results

The silicon box sealing was performed at the wafer level using eutectic AuSi. A device manufacturing sizing ~6.5x1.5x0.85mm3 with an internal cavity of 4mm3 was achieved. The wall thickness of the silicon box is typically from 100 to 200 µm.

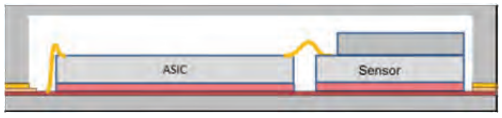


Figure 1: Hermetic Silicon Package schematic.

Residual Gas Analysis (RGA) was chosen to access to our cavity gas content and an estimation of water standard leak rate. The test consists in breaking devices placed under ultra-high vacuum in a first test bench, and analyzing with a mass spectrometer the gaseous species released from the cavity during the opening process and flowing through a calibrated diaphragm. The partial pressure of different gas inside cavity is plotted in figure 2 for several devices.

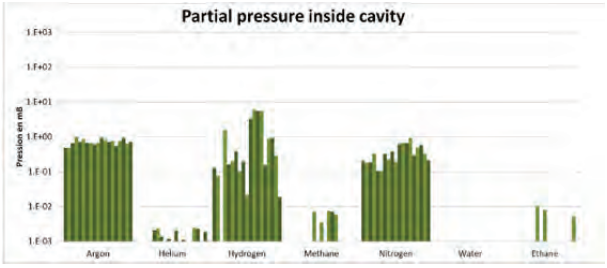


Figure 2: Partial pressure of different gas inside cavity.

In order to assess the hermetic properties of the sealed devices, it has been pressurized under gas such as Helium, Ar, or C2H6 for a given bombing time and then transferred to the RGA test bench. After pumping the test bench, the bombed devices were broken under UHV, and the gas partial pressure inside the cavity were measured. Assuming a molecular flow during the bombing period, it is then possible to calculate standard leak rate (L) as defined by the equation for the gas used during pressurization.

$$\Delta Pt = \Delta P0 e^{\frac{-Lt}{VP0}}$$

The water standard leak rate is calculated from the measured gas standard leak rates using following equation:

$$L_{H2O} = L_{gas}\sqrt{M_{gas} / M_{H2O}}$$

Finally, using this procedure, the water standard leak rate was estimated ~1 10^{-15} atm.cc/s which guarantees a life time much more than 20 years in water solution at 37°C.

Bio stability of some devices was tested to degradation in Phosphate Buffer Saline (PBS) at 90°C. PBS solutions are used to simulate the ionic concentrations of blood plasma. The PBS solution containing KH2PO4, Na2HPO4•2H2O, NaCl dissolved with DI water. RGA test were performed on devices after 40, 70 and 90 days and no water infiltration was detected which is an excellent result.

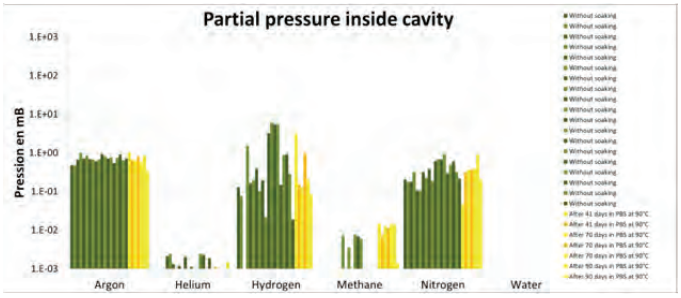


Figure 3: RGA test for devices with and without soaking in PBS at 90°C.

Perspectives

The complete process flow including functional devices has to be achieved and characterized. The Biodegradation test in complex biological environments like the NaCl/FBS medium which is more pertinent to predict the aging behavior of biomaterials used for encapsulating prolonged and chronic implants has to be performed.

Related Publications

[1] J-C. Souriau, J.M. Herrera Morales, L. Castagné, G. Simon, K. Amara and B. Boutaud, "Miniaturization and Biocompatible Encapsulation for Implantable Biomedical Silicon Devices" *ECS J. Solid State Sci. Technol.* Vol. 4, issue 12, P445-P450, 2015.

[2] G. Simon, J-C Souriau, "Electronics for Medical Applications" *DeMESys 2015, 1st International Conference & Exhibition for Development And Manufacturing of Electronic Systems,* April 1-2, Rabat Design Center, Morocco, 2015.

[3] J-C Souriau, L. Castagné, G. Simon, K. Amara, B. Boutaud, "Development of a New Wafer Level Packaging Process for the Manufacturing of Implantable Low Profile Silicon Box" *The 4th Advanced Technology Workshop on Microelectronics, Systems and Packaging For Medical Applications in Lyon 7-8 dec. 2015.*

Nanopackaging, Innovative Interconnection Solutions at Nanoscale

Research topics: Nanotechnology, 3D Integration, High Density Interconnections, Bionanoelectronics

A. Thuaire, P. Reynaud, C. Brun, D. Sordes, C. Carmignani, E. Rolland, X. Baillin, G. Poupon, S. Cheramy

Partnership: IBM, Jagiellonian University, CNRS-Cemes, CEA-DSM, CEA-DSV
Sponsorship: FP7-SiAM, FP7-AtMol, CEA-A3DN

Context and Challenges

Following the components miniaturization trend, packaging solutions, and especially interconnections, should be addressed at nanoscale. At the crossroads of bottom-up and top-down approaches, we report on the investigation of nano-objects electrical properties and integration for innovative interconnections, based on the development of a generic platform allowing both the nano-objects packaging and electrical characterization. Two approaches are considered, depending on the nature of the nano-objects and corresponding to two versions of the generic nanopackaging platform: a homogeneous approach in the case of silicon-based atomic wires, and a heterogeneous approach in the case of biological wires, such as DNA (DeoxyriboNucleic Acid) or amyloid fibers. In both approaches, these nano-objects are considered as possible planar interconnections.

Main Results

In the homogeneous approach, silicon-based atomic wires have been investigated as possible planar interconnections. Such wires are fabricated by STM-assisted hydrogen-resist lithography (STM: Scanning Tunneling Microscope) and require a Si(001)-(2x1):H reconstructed surface. A nanopackaging platform has been developed accordingly in order to ensure atomic wires fabrication (through surface reconstruction and preservation with a temporary cap), as well as their electrical investigation (through vertical interconnects) [1]. It is schematically illustrated on Fig.1. NOR/OR logic gates have been shown and measured [2] on such reconstructed and temporarily preserved surfaces.

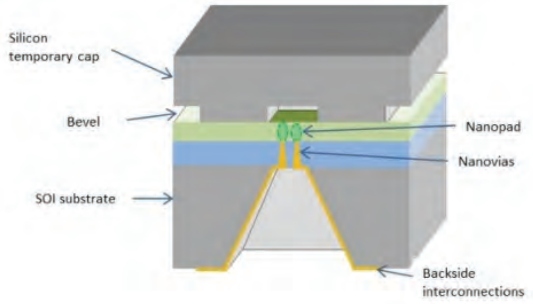


Figure 1: Illustration of the nanopackaging platform designed for atomic wires.

In the heterogeneous approach, biological wires (DNA and amyloid fibers) have been investigated, as possible planar interconnections as well. DNA is an attractive material for interconnections applications due to its size (2nm in diameter), its auto-assembling properties and its ability to be immobilized on a surface. Being however insulating, DNA has to undergo a metallization process. Such a plating process has been developed with Cu ions, as well as an immobilization and alignment processes. A dedicated characterization platform has been designed in order to collect statistical parameters [3], as shown on Fig.2.

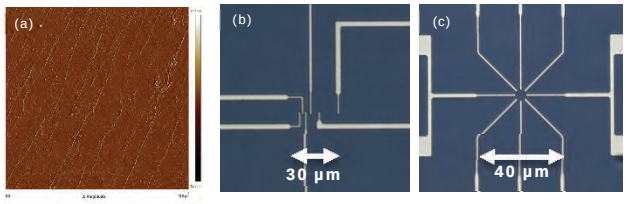


Figure 2: (a) AFM image of copper coated nanowires based on DNA and achieved by an electroless metal plating process (10x10 µm); (b)(c) Optical microscope images of 2 patterns of Ti/Au electrodes fabricated by lift-off process. Nanowires will be aligned following the white arrow direction.

Amyloid fibers are self-assembled protein-based nanowires of 4nm in diameter and a few microns long. Showing a similar morphology to DNA, these fibers have however shown an electrical conduction, as concluded from electrochemical measurements. This electrical behavior has been investigated, in particular through the development of a dedicated characterization platform [4], as illustrated on Fig.3.

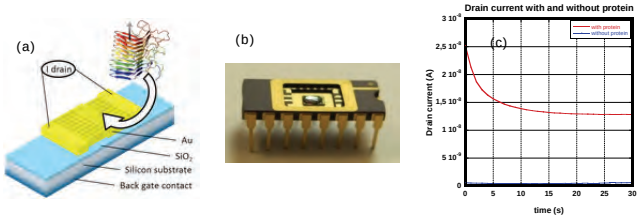


Figure 3: (a) Illustration of the characterization structure featuring gold comb-shaped electrodes on a silicon substrate); (b) Image of the packaged device after amyloid fibers deposition (droplet); (c) Evolution of the drain current as the function of time with and without protein nanowires deposition.

Perspectives

The presented results are part of on-going developments, aiming both at studying these nano-materials for interconnections applications, and in the meantime at improving nanopackaging platforms, and especially for the study of nano-objects electrical properties.

Related Publications

[1] A. Thuaire, G. Le Gac, G. Audoit, F. Aussenac, C. Rauer, E. Rolland, J.-M. Hartmann, A.-M. Charvet, H. Moriceau, P. Rivalin, P. Reynaud, S. Chéramy, N. Sillon X. Baillin, "Nanopackaging: from Nanomaterials to the Atomic Scale", *Advances in Atom and Single Molecule Machines*, Vol. 7, Sept 2015.
[2] M. Kolmer, R. Zuzak, G. Dridi, S. Godlewski, C. Joachim, M. Szymonski, "Realization of a quantum Hamiltonian Boolean logic gate on the Si(001):H surface", *Nanoscale*, 2015.
[3] C. Brun, C. T. Diagne, C. Carmignani, S. Torrengo, P.-H. Elchinger, P. Reynaud, A. Thuaire, A. Filoramo, D. Gasparutto, R. Tiron, X. Baillin, "Development of a statistical approach for DNA-based nanowires electrical study," *European Mircoelectronics and Packaging Conference (EMPC)*, Friedrichshafen, 2015.
[4] C. Carmignani, A. Rongier, L. Altamura, A. Thuaire, P. Reynaud, E. Rolland, N. David, N. Duraffourg, P. Rannou, V. Forge, T. Ernst, S. Cheramy, "First packaging developments on a characterization device for nano bio-inspired objects", *MINAPAD Conference*, Grenoble, 2015.

09

PHYSICAL & CHEMICAL CHARACTERIZATION & METROLOGY

- Correlative 3-D Characterisation
- Synchrotron-Based Laue Microdiffraction for 3D Integration and Solid Oxide Fuel Cell
- In Line High Resolution X-Ray Diffraction for the Characterization of GaN based HEMT
- Measuring the Photo-Carriers Lifetime by Kelvin Probe Force Microscopy and X-ray Photoelectron Spectroscopy
- Microscopic Surface Characterization of Highly-Doped GaN Wires
- In Die High Resolution Nanotopography Measurements for Improvement and Monitoring CMP and Bonding Process

Correlative 3-D Characterisation

Research topics: Characterization of Semiconductor Devices and Interconnects,

J.P. Barnes, V. Gorbenko, A. Priebe, G. Goret, G. Audoit, P. Bleuet, W. Hourani, E. Martinez, M. Veillerot, A. Grenier, F. Bassani (LTM), T. Baron (LTM), J. Laurencin (LITEN), E. De Vito(LITEN)

Partnership : CEA-LITEN, CNRS-LTM
Sponsorship: Labex MINOS, CARNOT Funding

Context and Challenges

The use of 3-D architectures both for devices and the integration of several chips together is a challenge for characterization techniques. Techniques that worked well for planar devices need adapting to 3-D devices such as FinFETs. The data obtained from one technique is often not sufficient and several techniques may be necessary. In order to increase the relevance of the data obtained, analyzing the same sample is desirable, but this poses many challenges in sample preparation.

Main Results

The analysis of III-V heterostructures grown in narrow trenches is one such challenge. A protocol was developed that allows SIMS profiles to be performed on arrays of trenches and the averaged profile extracted. The protocol exploits the fact that the trenches are nominally identical so that if many trenches are profiled at once this will be equivalent to profiling one single trench, but with the advantage of better statistics. The validity of this approach was tested using techniques with higher lateral resolution such as TOF-SIMS, NanoAuger, atom probe tomography and AFM. Fig.1 shows 3-D TOF-SIMS images of arrays of III-V heterostructures grown in 180nm wide trenches.

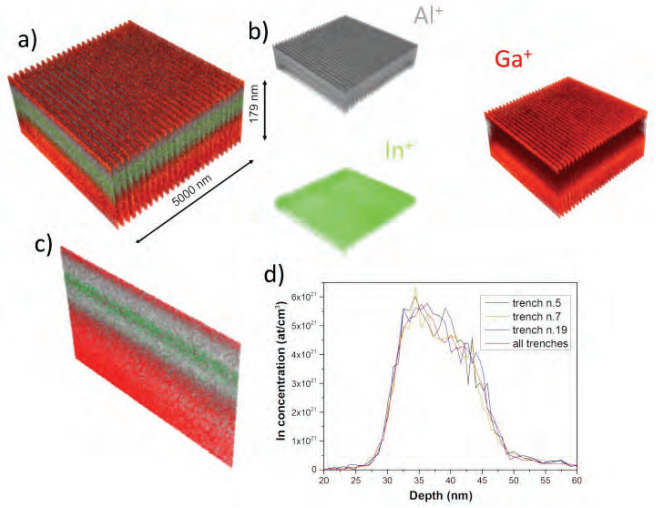


Figure 1: (a) 3-D TOF-SIMS reconstruction of the Al, In and Ga present in the III-V heterostructures selectively grown in 180 nm wide trenches. (b), separate volumes for Al, Ga and In, (c) 3-D reconstruction of a single trench, (d) TOF-SIMS depth profiles extracted from individual and all trenches.

The profile from one signal trench can be seen to be equivalent to that from all the trenches. However the profile from all trenches has better signal to noise ratio and represents the entire trench array and thus is more pertinent to assist process optimization.

The challenge for 3-D characterisation is not only at the nm length scale, but also in the complex, extremely heterogeneous structures found in 3-D integration, solid oxide fuel cells (SOFC) and battery electrodes. Here in order to obtain reliable information on the composition and morphology of such complex structures at the micron scale we have combined X-ray nanotomography and FIB-TOF-SIMS tomography. In order to maximize the advantages of combining the two techniques, a patented protocol was developed to allow both techniques to be performed on the same sample. The data from both techniques can be combined into one data set allowing the user to explore both the morphology and composition of the sample in 3-D. This correlative, multi-modal approach allows morphological artefacts to be corrected and quantification to be improved.

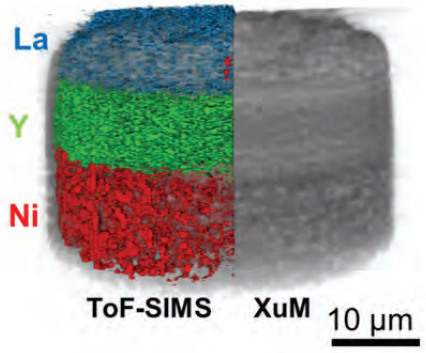


Figure 2: 3-D reconstruction of a SOFC sample. The X-ray nanotomography (XuM) reconstruction is shown in grey scale as a scale field representation. An iso-surface representation of the TOF-SIMS data for La (blue), Y (green) and Ni (red) is superimposed on the XuM data set. For clarity, only half the TOF-SIMS data set is shown.

Perspectives

The analysis protocols developed for the analysis of array structures will allow the high sensitivity of SIMS to provide statistically relevant data on non-planar device architectures. Future work will see the combination of SIMS with AFM and other measurements in the frame of PhD work and several European projects. The development of analysis protocols and data fusion methods will be continued and applied to other characterization techniques.

Related Publications
[1] V. Gorbenko, M. Veillerot, A. Grenier, G. Audoit, W. Hourani, E. Martinez, R. Cipro, M. Martin, S. David, X. Bao, F. Bassani, T. Baron, J.-P. Barnes. "Chemical depth profiling and 3D reconstruction of III-V heterostructures selectively grown on non-planar Si substrates by MOCVD", *Phys. Status Solidi RRL* Vol. 9, 202, 2015.
[2] V. Gorbenko, A. Grenier, G. Audoit, R. Cipro, M. Martin, S. David, X. Bao, F. Bassani, T. Baron, J.-P. Barnes, "Chemical characterization of III-V heterostructures in 3D architecture", *Microelectronics Journal*, 147, 219, 2015.
[3] V. Gorbenko, PhD thesis, Grenoble University 2015.

Synchrotron-Based Laue Microdiffraction for 3D Integration and Solid Oxide Fuel Cell

Research topics: Through Silicon Vias, Copper Pillar, Strain, SOFC, 3D Characterization

D.F. Sanchez, J-S. Micha (Néel/ESRF), J. Laurencin, P. Gergaud, P. Bleuet

Partnership : LITEN, INAC, ESRF
Sponsorship: STMicroelectronics, CATRENE-Master3D, ANR-AMOS

Context and Challenges

In this letter we highlight the potential of synchrotron-based Laue microdiffraction for (i) in-situ 2D study of strain in and around Through Silicon Vias (TSVs) and (ii) 3D grain and strain imaging of a solid oxide fuel cell sample (SOFC). A polychromatic synchrotron microbeam is essential to perform such studies: the brilliant synchrotron x-ray source ensures a characterization at the sub-micrometer level, and the polychromaticity makes it possible to retrieve the orientation, phase and strain (stress) at the grain level. On top of that, there is no need to rotate the sample (except for tomography), which simplifies in-situ studies. The condition for Laue microdiffraction to work is that the grain size must be equal or bigger than the x-ray spot size. At the ESRF beamline BM32, the beam size diameter is about 0.5 µm.

Main Results

In middle-TSV technology, the relatively large mismatch in the coefficients of thermal expansion (CTEs) between Cu and Si can induce thermal stresses in and around the TSV structures and raise serious reliability issues. To investigate this temperature effect, a chip containing TSVs has been backside thinned, and then a region of interest (ROI) has been isolated using plasma-FIB available at the nano-characterization platform (PFNC), see Fig.1 left.

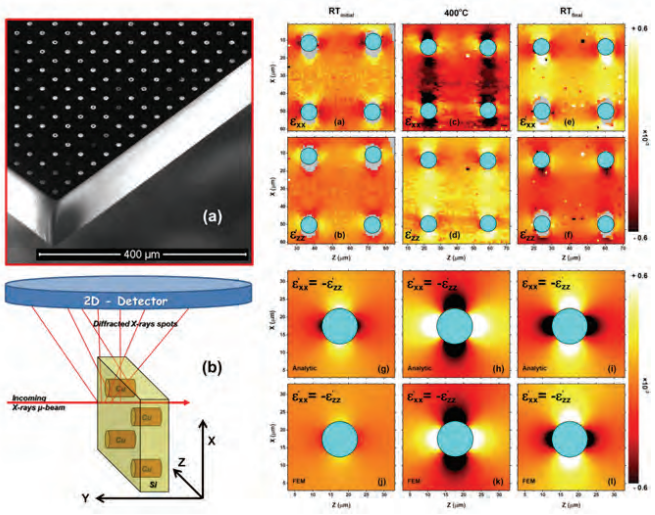


Figure 1: Sample prep (top left) and acquisition geometry (bottom left). Strain results at RT, 400°C and back to RT (top right) and equivalent simulation results (bottom right).

Measurements were then done in-situ, at room temperature (RT), then at 400° C and then back at RT at the French CRG-ESRF beamline BM32. Results are shown on Fig.1, where ε'_{xx} and ε'_{zz} (components of the strain tensor perpendicular to the TSV principal axis) are displayed for the 3 conditions. At RT, it evidences that the TSV is under in-plane tensile stress, i.e. pulling the internal walls of the Si cavity in the xz plane. It can be associated to the expansion and diffusive creep of Cu occurred under the first 400°C process annealing. During the second annealing at 400°C the Cu expands more than Si due to its higher CTE, resulting in the development of a compressive stress in the TSV. After cooling down to room temperature the TSV is again found under tensile stress, however the strain level does not come back to its initial value due to copper extrusion [1].

In the frame of an instrumental development, Laue microdiffraction has been extended to 3D using a so-called Laue tomography approach. Basically, the sample is raster scanned in (z,θ) (Fig.2) while Laue patterns are recorded. Here, it is necessary to rotate the sample for tomography, leading to completely different diffraction patterns from one angle to the other. A grain tracking method had to be developed to allow for grain reconstruction. Although the process is straightforward for a single crystal like Ge [2], it becomes more complex for polycrystalline materials like SOFCs. However, on a single reconstructed slice, SOFC grains could be reconstructed and their local deviatoric strain tensor calculated.

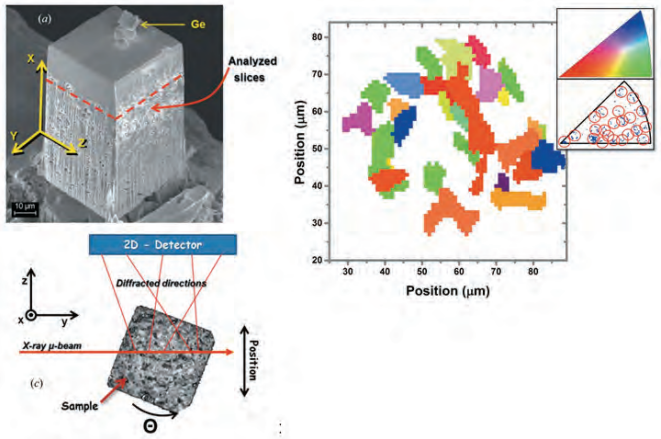


Figure 2: Sample preparation (top left) for Laue tomography and acquisition geometry (bottom left). The right image shows a reconstruction of grains with their color-coded orientation.

Perspectives

Laue tomography is still an exploratory work: it requires sample preparation with FIB, long scanning times and complex data processing. However, it is a unique technique to get depth-resolved strain and grain imaging at the sub-micrometer scale. Future work includes strain measurements for direct bonding.

Related Publications
[1] D.F. Sanchez, S. Reboh, M.L. Djomeni, J-S. Micha , O. Robach , T. Mourier , P. Gergaud , P. Bleuet, "In-situ X-ray µLaue diffraction study of copper through-silicon vias", *Microelectronics Reliability*, Volume 56, January 2016, Pages 78-84.
[2] D.F. Sanchez, J. Villanova, J. Laurencin, J-S. Micha, A. Montani,P. Gergaud, P. Bleuet, « X-ray micro Laue diffraction tomography analysis of a solid oxide fuel cell", *J. Appl. Cryst*. (2015). 48, 357–364.

In Line High Resolution X-Ray Diffraction for the Characterization of GaN based HEMT

Research topics: Metrology, X-Ray Diffraction, Power Electronics, GaN, Epitaxial Layers

A. Salaun, S. Favier, M. Charles, J. Kanyandekwe, A. Torres, E. Nolot

Partnership: BRUKER, STMicroelectronics
Sponsorship: KET-SEA4KET

Context and Challenges

New inline metrology protocols based on high-resolution X-ray diffraction (HR-XRD) must be developed to support the optimization of GaN-based stacks for HEMT applications (Fig.1). Such stacks include thin layers in hexagonal phase epitaxially grown on Si(111) substrate, and feature mosaicity that can impact optical and electrical properties of the films. AlGaN buffer layers, with various composition gradients, have been introduced in between Si 111 and GaN in order to reduce crack formation during cooling. AlN was also used to improve the nucleation on Si (111), which is a dense plane with a hexagonal arrangement, as shown in Fig.1b and elsewhere. The growth of (Al, Ga)N – whose stable phase is hexagonal as well – is thus easier on (111) oriented surfaces. This coherence should avoid the formation of a large density of dislocations, often located at the grain boundaries. The columnar structure of nitride layers along the (0001) direction is characterized by the tilt and twist of columnar domains.

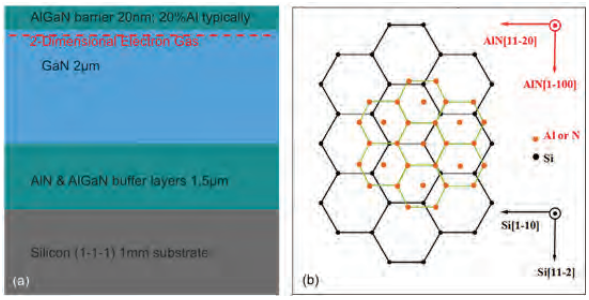


Figure 1. (a) GaN based HEMT stack (b) schematic structure[3] in-plane relationship between AlN and Si.

Main Results

High Resolution X-Ray Diffraction (HRXRD) has been performed to characterize the crystalline quality/density of dislocations of these layers around symmetrical and asymmetrical directions. The full width half maximum (FWHM) of the surface normal rocking curve (ω scan) is highly sensitive to the grain size and the tilt of columns and thus measured to monitor the film quality. The composition of $Al_xGa_{1-x}N$ buffer layers are deduced from $2\theta/\omega$ scan performed around (002) reflection (Fig.2a), assuming that the relaxation rate is close to 100% for GaN and AlGaN buffer layers. Both Al content and thickness of $Al_xGa_{1-x}N$ top layer can be deduced from the fringes at angles below 2θ(GaN).

Moreover, it is necessary to measure symmetric reflections for a large χ angle – i.e. (101), (102) or (204). In ternary materials such as $Al_xGa_{1-x}N$, the 2θ position of $Al_xGa_{1-x}N$[4] depends on both Al content and relaxation rate. As a consequence, Reciprocal Space Map (RSM) was performed around asymmetric $(204)^-$ reflection (Fig.2b). A section along the different spots leads to the corresponding line scan around $(204)^-$ and thus the 2θ positions of different layers. The $Al_xGa_{1-x}N$ barrier is fully strained to GaN, since the corresponding peak is found vertically above GaN peak, as shown in Fig.4. As the growth occurs on Si, the peaks are broad, and not very intense, which makes challenging to find the $Al_xGa_{1-x}N$ barrier in this map. Moreover the concentrations of Al in AlGaN barrier and AlGaN buffer layers are similar, which might explain the difficult distinction between the two peaks.

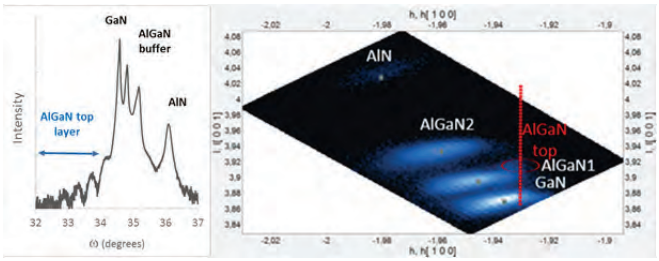


Figure 2 (a) HRXRD $2\theta/\omega$ scan around GaN (002) reflection, (b) RSM (I vs. h scan) around $(204)^-$ reflection.

The analysis of RSM $(204)^-$ in addition to $2\theta/\omega$ (002) makes possible the determination of cell parameters in both directions (a and c-parameters) through the Bragg's relation and thus the tensile strain of each layer. Both measurements are necessary to get strain and concentration.

Perspectives

Future work will include the definition and validation of metrology protocols dedicated to more complex GaN-based HEMT stacks that can include, for instance, thin GaN layer on top of ultrathin $Al_xGa_{1-x}N$ barrier layer. In this case, the unambiguous determination of the top pGaN thickness along with thickness and composition of $Al_xGa_{1-x}N$ barrier layer remains challenging.

Related Publications

[1] A.Salaun, S.Sollier,Y.Bogumilowicz, S.Favier,J.Widiez, T.Baron, M.Martin, S.David, A.Singh, E.Nolot, "Métrologie « in - line » pour le développement des procédés d'épitaxie III - V", *XI*ème *Colloque Rayons X & Matière*, 1-4 Dec. 2015, Grenoble, France.

Measuring the Photo-Carriers Lifetime by Kelvin Probe Force Microscopy and X-ray Photoelectron Spectroscopy

Research topics: Photo-Carrier Lifetime, Work Function

Ł. Borowik, B. Grévin (INAC), S. Pouch, O. Renault, D. Mariolle, N. Chevalier

Partnership : INAC-SPrAM, Università di Modena e Reggio Emilia
Sponsorship: RTB Program

Context and Challenges

Progress in photovoltaic research calls for the development of novel characterization methods providing reliable and direct determination of the physical quantities governing the efficiency of a solar cell, namely: the photocarrier mobility, the photo-carrier lifetime, the absorption coefficient, and the band gap of the active materials. Among these quantities, the photo-carrier lifetime plays an important role in the overall efficiency of a solar cell because it limits the proportion of photo-generated charges collected at the electrodes.

Main Results

It was shown [1] that photo-carrier lifetime can be measured by KFM and XPS using a steady method based on the time-averaged evolution of the surface potential when a modulated illumination is used over a large range of frequency (Fig.1).

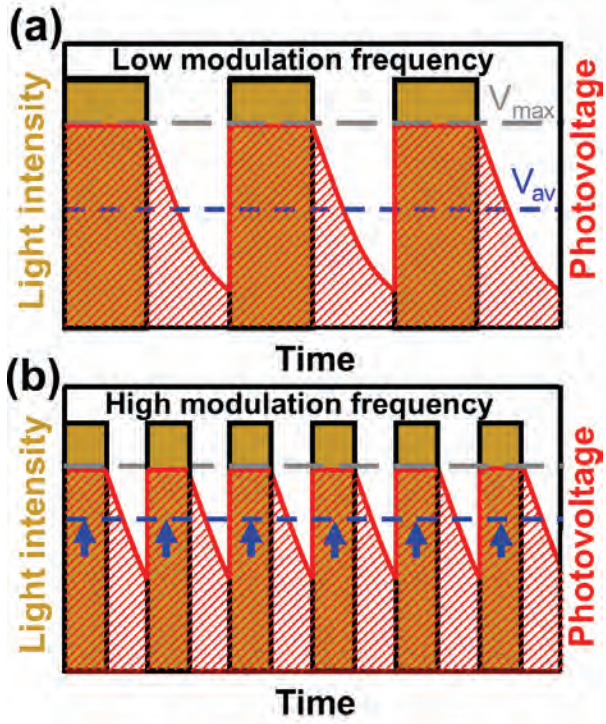


Figure 1: Schematic illustration of the time evolution of the surface photovoltage under modulated illumination. Values we intended to measure: the saturated surface photovoltage Vmax (grey dotted line) and the time-averaged surface potential Vav (blue dotted line). The evolution of Vav is depicted for the cases of (a) low frequency and (b) high frequency.

The experimental data can be fitted with model below where the fit parameter is the value of the photo-lifetime:

$$\frac{\Delta V_{av}}{\Delta V_{max}} = \alpha + \tau \cdot f\left(1 - exp\left(\frac{\alpha - 1}{\tau \cdot f}\right)\right)$$

where Vmax, is measured under continuous illumination, whereas the time-averaged surface potential, Vav, is measured under modulated illumination, f is the modulation light frequency and α is the modulation duty ratio. Accuracy of the lifetime measurement method is directly linked to sensitivity of KFM and XPS which was show to better than 20 meV on silicon germanium heterostructures. [2]

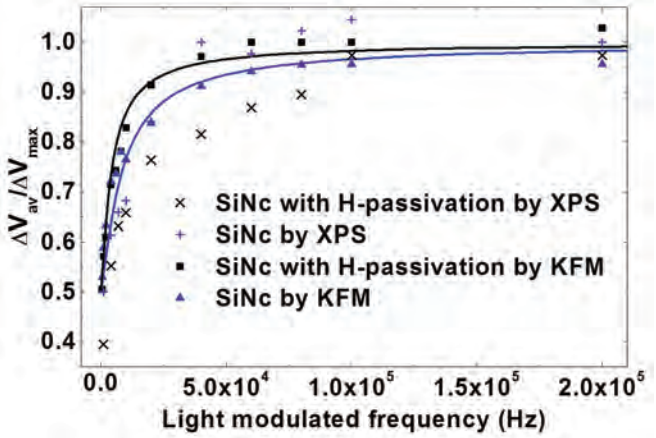


Figure 2: ΔVav/ΔVmax as the function of light modulation frequency. We present the measurements on the Si nanocrystals embedded in 30 nm of SiO2 before and after hydrogen passivation. The fitted curves to KFM data are given by an exponential model using estimated photo-carrier lifetime values.

In the case of Si nanocrystals embedded in 30 nm of SiO2 (Fig.2) we found τ=7×10−5 s and τ = 3.5×10−5 s for the passivated and non-passivated nanocrystals, respectively.
The longer photo-carrier lifetime for hydrogen-passivated nanocrystals can be explained by smaller quantity of defects on the nanocrystal surface. Thus, these results confirm the impact of hydrogen passivation on the photo-carrier lifetime.

Perspectives

Summarizing, we have developed the photocarrier lifetime measurements on silicon nanocrystal-based third-generation solar cells. This analysis gives a perspective on performing KFM lifetime mapping [3] with a higher lateral resolution for the surface potential measurement and with good accuracy. The work on KFM lifetime mapping is scheduled together with INAC institute.

Related Publications
[1] Ł. Borowik, H. Lepage, N. Chevalier, D. Mariolle, O. Renault, “Measuring the lifetime of silicon nanocrystal solar cell photo-carriers by using Kelvin probe force microscopy and x-ray photoelectron spectroscopy”, *Nanotechnology 25*, 265703, 2014.
[2] S. Pouch, M. Amato, M. Bertocchi, S. Ossicini, N. Chevalier, T. Mélin, J-M. Hartmann, O. Renault, V. Delaye, D. Mariolle, Ł. Borowik, “Work Function Measurement of Silicon Germanium Heterostructures Combining Kelvin Force Microscopy and X-ray Photoelectron Emission Microscopy”, . *Phys. Chem. C, 2015,* 119 (47), pp 26776–26782.
[3] S. Pouch, “Nano characterization of materials used in photovoltaics by near-field microscopy and electron spectroscopy: work function and carrier lifetime measurements”. *PhD Thesis*. 2015.

Microscopic Surface Characterization of Highly-Doped GaN Wires

Research topics: GaN, Lighting, Surface Characterization

O. Renault, J. Morin, N. Chevalier

Partnership: Néel Institute, Forschungzentrum Jülich
Sponsorship: RTB Program

Context and Challenges

Semiconducting wires have attracted increasing interest over the past years thanks to the progress of the synthesis methods and the large number of applications in device technology from solid-state lighting to biosensing. Controlling the doping level of the wires is essential for fabricating high-performance devices. The physical characterization of the wires is often challenging because dealing with individual objects, nevertheless reliable methods providing direct information are required. Four-probe measurements are time consuming and with a limited spatial resolution. It is desirable therefore to consider complementary, suitable contactless methods in the study of doped semiconducting wires able to provide direct insights on the doping properties.

Main Results

Here, we have employed a combination of surface-sensitive techniques based to study the Si doping of highly-conductive GaN microwires and complement bulk-sensitive electrical data. Highly *n*-doped GaN wires are of high interest in solid-state lighting and direct measurements of doping by physical characterization methods are desirable on single wires. We considered X-ray photoelectron emission microscopy (XPEEM) for the surface chemistry and Si active doping level, scanning capacitance microscopy (SCM) for the axial doping distribution and uniformity, and scanning Auger microscopy (SAM) for the overall Si concentration. Fig.1(a) shows an XPEEM image of a GaN wire with two zones of different doping levels.

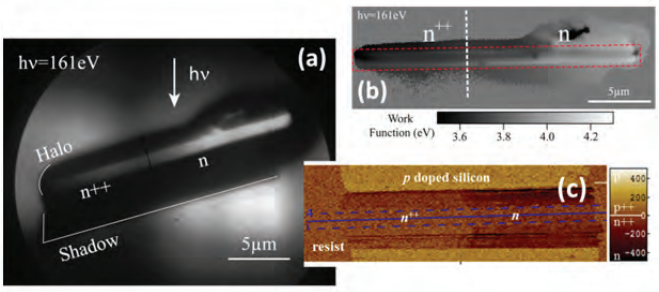


Figure 1: Threshold photoemission XPEEM image (a) and corresponding work function image (b) of a n^{++}/n Si-doped GaN micro-wire on p-Si substrate. Corresponding SCM image (c).

The image contrast is related to the work function difference arising from the doping heterogeneity along the wire axis. This further confirmed by the work function map generated from the XPEEM data, with a smaller work function in the zone of higher nominal doping level. Although band bending affects the work function value (with in particular, a contribution from surface photovoltage), it is stressed here that the image is indicative of a reasonable doping uniformity in each zone. This is also observed on the SCM image of Fig.1(c), from which two distinct and well-defined SCM signal plateaus can be extracted.

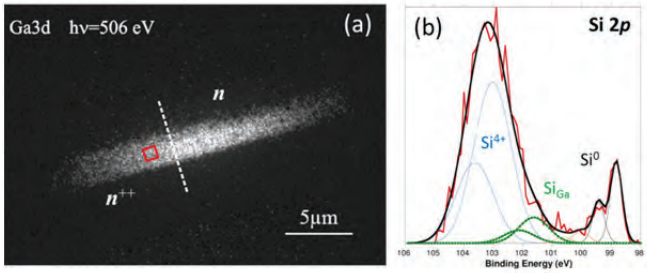


Figure 2: XPEEM image (scale bar: 5 µm) of the Ga surface concentration (a) characteristic of the GaN wire imaged in Fig.1a. (b) Si2p XPS spectrum emitted from the n^{++} zone, revealing the contribution of Si interstitials in Ga sites characteristic of active doping.

In Fig.2, the chemistry of Si incorporation at the GaN wire surface is investigated by core-level XPEEM. The wire is revealed on the image performed with characteristic Ga photoelectrons. Similar images, but of much weaker intensity, are produced using Si photoelectrons, from which core-level spectra emitted from the n^{++} zone (Fig.2b) can be retrieved. The spectrum shows that Si is present mostly in the elemental and oxide form, and to a lesser extent as nitride states assigned to interstitial Si in Ga sites, characteristic of fully ionized, electrically active dopants. With the knowledge of the overall Si concentration determined by SAM, we can determine an upper limit of the active Si-doping level to be 2.10^{21} at/cm^3. This figure is in reasonable agreement with the donor density of up to 710^{20} at/cm^3 derived from independent electrical measurements. Therefore, the combined analysis method presented here enables to extract both qualitative and quantitative information on the *electrically active* doping level in highly-doped GaN wires.

Perspectives

This work paves the way to a combined use of surface-sensitive techniques such as scanning probes, scanning Auger nanoprobe and photoelectron emission microscopy for the study of other semiconducting, highly doped single wires.

Related Publications

[1] O. Renault, J. Morin, P. Tchoulfian, N. Chevalier, V. Feyer, J. Pernot, C.-M. Schneider,"Spectroscopic XPEEM of highly conductive Si-doped GaN wires" *Ultramicroscopy* 159 (2015) 476-481.

[2] J. Morin, "Determination of dopant level in semiconductor nano/microwires by XPEEM (X-ray photoelectron emission microscopy)", *PhD Thesis*, University Grenoble-Alpes, 2013.

In Die High Resolution Nanotopography Measurements for Improvement and Monitoring CMP and Bonding Process

Research topics: Metrology, Nanotopography, Process Control, CMP, Interferometry

N.Ruiz, F.Dettoni, M.Rivoire, V.Balan, C. Beitia

Partnership: STMicroelectronics

Context and Challenges

Today 3D integration is one of the alternative to improves performances and add functionalities to devices. The former is even more true when considering IOT (internet of things) needs for systems integrating sensors, logic, memory, communication and energy harvesting. However to make this possible, 3D integration processes need to be developed and be cost efficient. CMP and Bonding are among the key processes steps needed to make 3D possible. Indeed to stack devices you need to bond them and to do this CMP need to be as good as possible (minimum roughness and maximum flatness). For this reasons nanotopography measurements has appeared in the last year as a challenge for this process steps. In the last years Leti has been developing this metrology [1,2] through interferometry microscopy in phase shifting and coherence scanning modes. However gaps still remains in the parametrization of the pertinent information to process but as well in the fundamental side, concerning accuracy, traceability and reference metrology.

Main Results

One of the first challenges is the amount of information which is gather and need to be summaries in a proper parameter to track and improve the process. Thus, new metrics need to be developed in order to make this measurements useful to the engineers. Several studies have been carried out in this sense [3]. The first step is to separate the global information and the local high resolution one. Fig.1 shows the die high resolution data in nanotopography. Global variation can be observed on the die across the center and edge position. This global view of the die gives immediate input about problematic zones and allows comparison of its variation across the wafer.

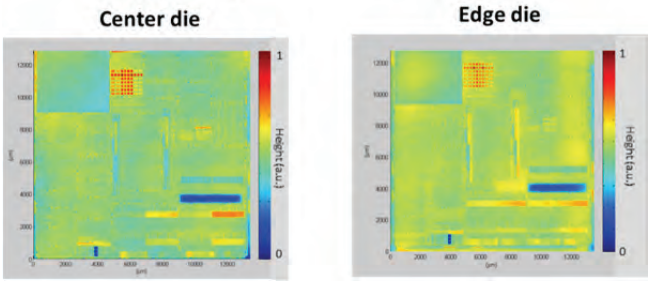


Figure 1: Die nanotopography at center and wafer edge.

In order to go further in the analysis specific parameters are needed to allow a quantitative comparison of those differences. At this level, our studies has demonstrated that height distribution can be a good indicator. Indeed a perfect CPM process will produce a perfect flat surface which will be characterize by a Dirac's height distribution. A more realistic deviation from this perfect behavior will be a unique narrow height distribution, so CMP process will be represented by its half width at medium height and its mean relative position. In addition the presence of two or more distribution will indicate the non-uniformity of the process.

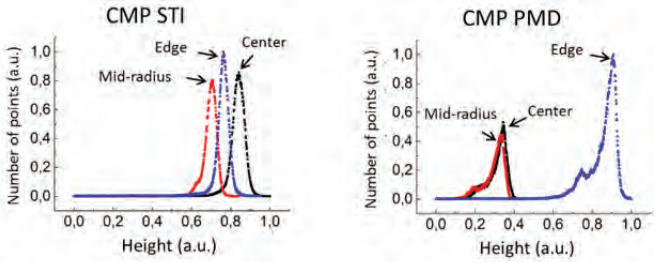


Figure 2: Height distribution across wafer for two different STI and PMD CMP processes.

To illustrate this point, Fig.2 shows examples of distributions for STI and CMP processes. The CMP STI process can be well described by a Gaussian distribution with a negligible secondary population in the lower values side of the distribution, so we can consider that they represent mostly a unique population. In addition all distributions are centered about 0.8 with 0.1 variations. This results indicates that CMP is efficient for the die level uniformity (independent of the different in material and densities inside the die) and this across the wafer. At the contrary, the CMP PMD process has a clear different signature with an important secondary population in the lower values side of the distribution. In this case it cannot be assumed a unique population. Also the mean heights between dies are different. Thus, the distribution center value in the edge die is about 0.9 while middle and center die are at about 0.3. This double population may be attributed to the non-selective nature of this CMP process. These results demonstrate the interest of nanotopography measurement together with appropriate parametrization of the data. This kind of analysis coupled with traditional local profile analysis might be the good strategy to control the CMP process for bonding in 3D applications.

Perspectives

Spite of these good results different challenges still need to be overcome to get an industrial solution. The main important one is the need to use a metallic coating in order to avoid artifact coming from the material heterogeneity of the sample. New approaches to the later issue need to be found to have an industrial solution. The other challenge faced by this measurements is the absence of standards and reference metrology been able to have the best calibration and the best characterization of the instrumental function of the microscope allowing a clear and accurate separation between measurements and process variation as well as tool to tool comparison. All these aspect are current topics of research at Leti and we are collaborating on them.

.

Related Publications

[1] F.Dettoni, M.Rivoire, S.Gaillard, O. Hinsinger, C.Beitia "High Resolution Nanotopography Characterization at Die Scale of Front End CMP Processes", *Microelectronics Engineering*, 113 January 2014.

[2] N. Ruiz, F.Dettoni, M. Rivoire, V.Balan, C. Beitia, " Nanométrologie pour les procédées de polissage mécano chimique dans la micro et nanoélectronique", *4ièmes rencontres annuelles du club de nanometrolgie Français*, Paris Janvier 2015.

[3] N. Ruiz, F.Dettoni, M. Rivoire, V.Balan, C. Beitia, "In-Die high resolution nanotopography data, impact in the CMP process monitoring for advanced nodes", *Proceeding International Conference on Frontiers of Characterization and Metrology for Nanoelectronics* (FCMN), 2015.

10

EMERGING PROCESS

- Fracture Dynamics in Silicon Implanted with Light Ions
- Innovative Substrate : III-V-on-Insulator
- Reliable Four-Point Flexion Test and Model for Die-to-Wafer Direct Bonding
- III-V Process Modules for Nanoelectronics
- Surface Organometallic Chemistry for Molecular Layer Doping (MLD) and the Synthesis of MoS2

Fracture Dynamics in Silicon Implanted with Light Ions

Research topics: Layer Transfer, Smart Cut™, SOI, Fracture Mechanism, Ion Implantation

F. Mazen, D. Massy, F. Madeira, S. Reboh, A. Reinhardt, D. Landru (SOITEC), F. Rieutord

Partnership: CEA-INAC, SOITEC
Sponsorship: EXACT, ECSEL- WAYTOGO FAST

Context and Challenges

The Smart Cut™ technology is currently the industry standard for manufacturing Silicon-On-Insulator (SOI) substrates, widely used in advanced microelectronics devices. It is based on the implantation of a relatively high dose of light (H/He) ions in a thermally oxidized silicon substrate which leads to the formation of a buried weakened layer in the crystal. The implanted wafer is then bonded onto a host substrate using direct wafer bonding. Under annealing, the implanted species evolve into microcracks lying parallel to the surface, and a controlled fracture process finally occurs along the implanted layer.

While direct wafer bonding statics and dynamics are now well understood, the fracture dynamics during Smart Cut™ remains largely a field to be explored. Yet, the ever decreasing thickness and more and more drastic uniformity specs of SOI substrates requested by the microelectronics industry calls for a multiscale understanding and control of the fracture step. In fact, wafer-scale fracture being one of the last key steps of Smart Cut™, it may impacts directly the SOI active layer properties by revealing the underlying crack microstructures and interactions.

Main Results

Fracture waves in brittle solids have a very high velocity which renders tricky the study of their propagation. So, we have developed an original device to study the crack propagation during the fracture step of Smart Cut™.

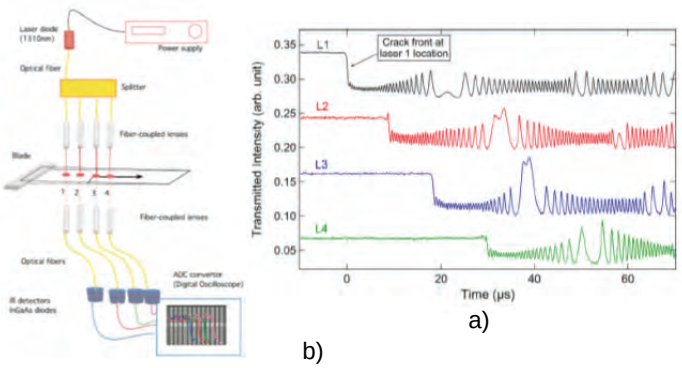


Figure 1: a) Experimental setup for crack front velocity measurements b) Laser interferences due to crack opening gap recorded during the crack propagation.

As shown on Fig.1-a, it is an optical bench based on the transmission monitoring of multiple infrared lasers through the silicon sample. As silicon is transparent at these wavelengths, the infrared beams are collected on the other side of the sample. Fast photodiodes are used to convert the transmitted light into electrical signals which are recorded using a high bandwidth numerical oscilloscope as shown in Fig.1-b. Initially, the intensity received on the detector is constant since the two wafers are still bonded. The opening gap creates two new surfaces where the laser beam can be partially reflected. Therefore, when the crack front reaches the laser location, the signal intensity drops. The following part of the transmitted signal is made of series of periodic oscillations. That specific shape is due to the air gap formation between the two separated wafers, where laser beam experiences multiple partial reflections producing interference fringes.

First, by measuring the time lags between the intensity drops on each laser, fracture velocity in the sample can be directly deduced. Depending on process conditions, we have measured that fracture wave speed is in the km /s range and is constant all along the sample. In the example presented in Fig.1-b the fracture velocity is 1,8 km/s. Among others, we have studied the impact of temperature on fracture velocity and results are presented on Fig.2. We obtained a good agreement of the curve shape with what is expected from the classical expression of fracture speed in brittle materials(1) where Vr is the Rayleigh wave speed, Γ correspond to the energy cost to open uncracked areas and G the “mechanical” energy of pressurized microcracks.

$$V = Vr\left(1 - \frac{\Gamma}{G}\right) \quad (1)$$

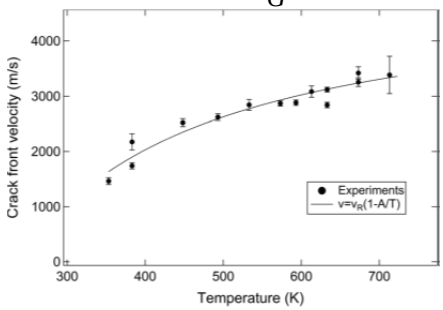


Figure 2: Variation of the crack velocity as a function of split temperature Solid line is a fit according to expression (1).

Second, from the interference fringes signal analysis, we were able to calculate both the wafers displacements in the wake of the fracture front and the released gas quantity (using elasticity theory and thermodynamics). In particular, we found that around 35 % of the implanted ions are released during fracture step which is in quantitative agreement with previous studies performed with mass spectroscopy analysis..

Perspectives

An original way allowing “in situ” study of crack propagation speed and wafer displacement during Smart Cut™ fracture step has been developed. It will allow us to better understand the impact of fracture dynamics on transferred films morphology and then help us to find ways to improve the characteristics of advanced SOI wafers such as flatness, top silicon thickness uniformity, etc.

Related Publications
[1] D. Massy, F. Mazen, S. Tardif, J. D. Penot, J. Ragani, F. Madeira, D. Landru, O. Kononchuk, F. Rieutord, "Fracture dynamics in implanted silicon”, *Applied Physics Letters*, Vol 107, 092102, 2015.
[2] D. Massy, F. Mazen, D. Landru, N. Ben Mohamed, S. Tardif, F. Madeira, A. Reinhardt, A. Barthelemy, O. Kononchuk,, F. Rieutord, “Fracture dynamics in the Smart Cut technology”, *European Materials Research Society fall meeting conference (e-MRS)*, 15-18 sept 2015, Warsaw, Poland.
[3] F. Mazen, D. Massy, F. Madeira, S. Reboh, D. Landru, V. Carron, F. Rieutord, “Extended defects formation and growth mechanisms after light ions implantation in Silicon”, *Advances in Materials and Processing Technologies conference (AMPT)*, 14-17 dec 2015, Madrid, Spain.

Innovative Substrate : III-V-on-Insulator

Research topics: High-Mobility Material, III-V, Bonding, Smart Cut™ Technology

J. Widiez, S. Sollier, T. Baron (CNRS-LTM), M. Martin (CNRS-LTM), G. Gaudin (SOITEC), C. Veytizou (SOITEC), F. Mazen, Y. Bogumilowicz, C. Morales, MC. Roure, P. Besson, H. Grampeix.

Partnership: CNRS-LTM, SOITEC, IBM
Sponsorship: FP7-COMPOSE3, SOITEC

Context and Challenges

III-V compound semiconductors such as InGaAs material are promising candidates to replace Si in n-channel MOSFETs due to their high electron mobility values. A prerequisite in view of their VLSI integration is the formation of high quality III-V heterostructures on a silicon substrate to enable production on large size wafers. III-V integration on Si by direct wafer bonding (DWB) is considered as one of the possible paths towards this objective.

InGaAs-OI (on insulator) substrates using DWB followed by substrate etching, with InGaAs directly grown on bulk InP, have been already demonstrated in literature. This expensive process (due to the loss of the InP wafer) is limited to 4-inch. wafer sizes (maximum InP wafers diameter). Recently, the same technique has been extended to InGaAs layer grown on Si wafer, solving the wafer size issue but maintaining a significant cost. One paper has reported the use of the Smart Cut™ technology but on a 4'' InP substrate. We have successfully fabricated 300 mm InGaAs-OI substrates using the Smart Cu™ technology with III-V layers epitaxially grown on 300 mm Si wafer.

Main Results

The fabrication process of the InGaAs-OI substrates is reported in Fig.1. InGaAs-based III-V layers (InGaAs/InP/GaAs) were grown directly on 300 mm on-axis Si(100) substrate by metal organic chemical vapor deposition (MOCVD). A 20-nm-thick Al_2O_3 layer was deposited on this donor wafer by Atomic Layer Deposition (ALD) at 300°C. Next, the Al_2O_3 is capped with a SiO_2 layer (Fig.1a), and annealed at 600°C under N_2 flow to ensure degassing. The H+ implantation is located inside the InP buffer layer. DWB is realized on a thermally oxidized Si substrate using a SiO_2//SiO_2 bonding after a polishing and cleaning surface preparation (Fig.1c). The splitting is performed by thermal annealing at 350°C (Fig.1d). 300 mm post splitting III-V-OI wafers are obtained without any bonding defects (Fig. 2). TEM image (Fig. 2) confirms the good crystallinity of the transferred InGaAs layer. The remaining InP layer is wet-etched in hydrochloric solution to expose the InGaAs channel. X-ray diffraction analysis reveals high quality of the transferred layer It is found that the Full Width at Half Maximum (FWHM) of the corresponding rocking curve around (004) InGaAs reflection is 1370 arcsec. This value corresponds to a threading dislocation density (TDD) of about 3.10^9 cm^{-2} according to Ayer's model.

This is the first demonstration of fracture in an InP epitaxial layer on Si substrate. We performed H+ implantations in the InP epitaxial buffer layer at different temperatures (from 16 to 90 °C) by using 300 mm Al_2O_3/InP (500 nm)/GaAs/Si wafers.

Optical microscope observations revealed that we were able to obtain blisters and local exfoliated areas after a 300 °C annealing. The buried micro-cracks localized in the InP layer, observed in cross-section scanning electron microscopy images, presage the feasibility of layer transfer, confirmed during the InGaAs-OI fabrication. The low RMS roughness value of 11 nm measured on a 5×5 µm² AFM scan on the post-splitting InP surface reflects the good fracture confinement in the epitaxial InP layer. This study prooves that splitting process in epitaxial InP layer occurs in a large implantation condition ranges on the contrary to bulk InP.

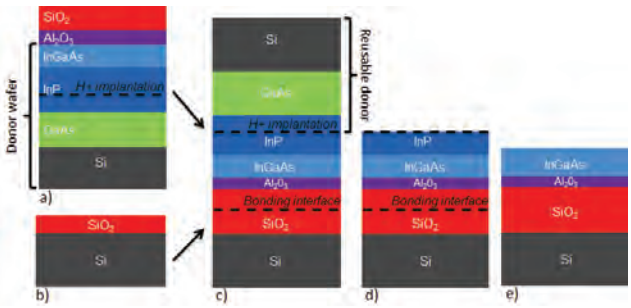


Figure 1: Fabrication process flow of the InGaAsOI substrates using the Smart Cut™ technology.

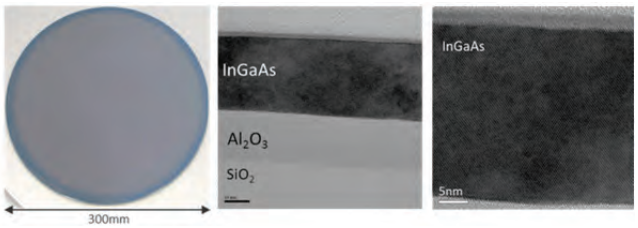


Figure 2: Left: Picture of the InGaAsOI substrate after the layer transfer. Right: TEM and HR-TEM images of the transferred InGaAs layer on the Al_2O_3 buried oxide.

Perspectives

We demonstrated the successful fabrication of 300 mm InGaAs-OI substrates from direct growth of InGaAs on Si substrate and using both the direct wafer bonding process and the Smart Cut™ technology.

The future objective is to transfer a III-V layer on processed CMOS wafers. Using the CoolCube™ technology, we can imagine having high performance top nMOSFET with high mobility III-V active layer, with thermal budgets compatible with bottom SiGe pMOSFET integrity.

Related Publications

[1] J. Widiez, J-M. Hartmann, F. Mazen, S. Sollier, C. Veytizou *et al.*, "SOI-type Bonded Structures for Advanced Technology Nodes", *ECS Trans. (2014)* volume 64, issue 5, 35-48 (Invited talk).

[2] J. Widiez, S. Sollier, T. Baron, M. Martin, G. Gaudin, F. Mazen, F. Madeira, S. Favier, A. Salaun, S. Arnaud, S. David, E. Beche, H. Grampeix, C. Veytizou, D. Delprat, T. Signamarcheix,, "First demonstration of 300 mm InGaAs-On-Insulator substrates fabricated using the Smart Cut™ technology", *Proceedings of SSDM conference*, 2015.

[3] S. Sollier, J. Widiez, G. Gaudin, F. Mazen, T. Baron, M. Martin, M. C. Roure, P. Besson, C. Morales, E. Beche, F. Fournel, S. Favier, A. Salaun, P. Gergaud, M. Cordeau, C. Veytizou, L. Ecarnot, D. Delprat, I. Radu, T. Signamarcheix, "300 mm InGaAsOI substrate fabrication using the Smart Cut™ technology", *Proceeedings of S3S conference*, p.1-2, 2015.

Reliable Four-Point Flexion Test and Model for Die-to-Wafer Direct Bonding

Research topics: Die to Wafer, Direct Bonding, Bonding Energy Measurement, Four Point Flexion Test

T. Tabata, L. Sanchez, F. Fournel, H. Moriceau

Partnership: STMicroelectronics
Sponsorship: IRT Photonic

Context and Challenges

Die-to-wafer direct bonding between heterogeneous materials has gained significant attention in photonics and microelectro-mechanics. Due to the relatively late development of this technology, more studies are needed to understand its mechanisms and fine behavior. For sure, Wafer-to-wafer direct bonding has been already well studied in terms of bonding energy measurement and bonding mechanism comprehension. However, even if the bonded materials are the same, it is not so much clear that die-to-wafer direct bonding has the same behavior as wafer-to-wafer direct bonding especially concerning the bonding strength. Indeed, geometrical effects of die edges should not be neglected. Therefore, it has been strongly required to develop a bonding energy measurement technique which is suitable for die-to-wafer direct bonding interface measurements.

Main Results

Usually wafer to wafer bonding energy is measured by the double-cantilever beam (DCB) technique under prescribed loaded because of the measurement simplicity and result interpretation. A razor blade is inserted at the bonding interface and the resulting debonding length allows calculation of the bonding energy. DCB technique can't be used with die because of die dimensions and the absence of bevel. To overcome this limitation, the four-point flexion test technique (4PT) has been modified and applied for evaluation of die-to-wafer direct bonding strengths [1].

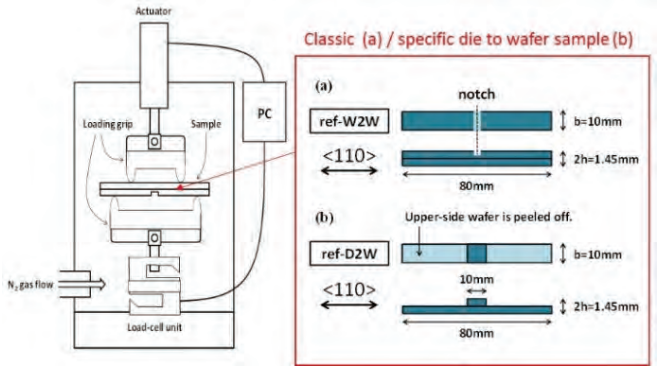


Figure 1: Schematic figure of experimental setup of the four-point flexion test technique in nitrogen atmosphere. The load-cell unit can read the applied load value, while the actuator gives the position of inner loading grips.

Standard SiO_2-to-SiO_2 direct bonding samples are elaborated in wafer-to-wafer (W2W) and die-to-wafer (D2W) architectures in order to compare standard 4PT sample and 4PT die sample. When the standard 4PT technique supposes a step for a pre-crack formation, an alternative modified 4PT technique can propose to skip the pre-crack formation step for the die to wafer measurements having a simple debonding starting from the die edges during the specimen bending.

The water stress corrosion (WSC) effect induced by the humidity of experimental atmosphere could impact bonding energy measurements. It is a very well-known effect especially if siloxane bonds (Si-O-Si) are present at the bonding interface [2]. We have shown that it's possible to avoid WSC effect by the experimental atmosphere and also by the trapped water at the bonding interface by drying the experimental atmosphere and by using an adapted loading speed.

To validate this alternative 4PT approach, 4PT measurement are compared to DCB measurement with samples made from the same wafer bonding. Because loading mode are not the same between DCB (tensile opening) and 4PT (tensile and in-plane shearing opening), classical theory of fracture mechanics has been used to extract the tensile contribution from the 4PT measurement [3]. Thanks to a high flexion-loading speed in the 4PT and a high razor-blade-insertion speed in the DCB test, we have shown that the 4PT and DCB technique give the same bonding energy value (tensile contribution G_I) without WSC. Furthermore, direct bonding energies with either W2W or D2W architectures has been measured using the 4PT technique. We have demonstrated that bonding energy values of D2W samples are effectively measured by our 4PT technique, resulting in a good agreement with the values of W2W samples.

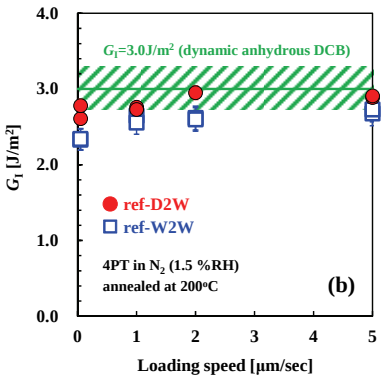


Figure 2: Tensile contribution G_I value versus the applied loading speed in our 4PT measurement of W2W and D2W samples in N_2 (1.5% RH) after 200°C annealing.

Perspectives

This technique will be very helpful to understand die direct bonding mechanisms and to optimize die direct bonding process.

Related Publications
[1] T. Tabata, L. Sanchez, F. Fournel, H. Moriceau, "Reliable four-point flexion test and model for die-to-wafer direct bonding", *Journal of Applied Physics*, 118, 015301 (2015).
[2] F. Fournel, C. Martin-Cocher, D. Radisson, V. Larrey, E. Beche, C. Morales, P. A. Delean, F. Rieutord, H. Moriceau, « Water Stress Corrosion in Bonded Structures", *ECS J. Solid State Sci. Technol.* volume 4, issue 5, P124-P130 (2015).

III-V Process Modules for Nanoelectronics

Research topics: CMOS, Monolithic 3D Integration

J.M. Hartmann, Y. Bogumilowicz, M. Rebaud, Ph. Rodriguez, L. Toselli, E. Ghegin, N. Rochat, N. Chevalier, E. Martinez, F. Nemouchi, M.C. Roure, V. Loup, P. Besson (STM); L. Czornomaz[1], J. Fompeyrine[1], M. Martin[2], T. Baron[2], J.B. Pin[3], E. Sanchez[3]

Partnership: IBM Research GmbH Zürich Laboratory[1], CNRS-LTM[2], Applied Materials[3]
Sponsorship: FP7-COMPOSE3

Context and Challenges

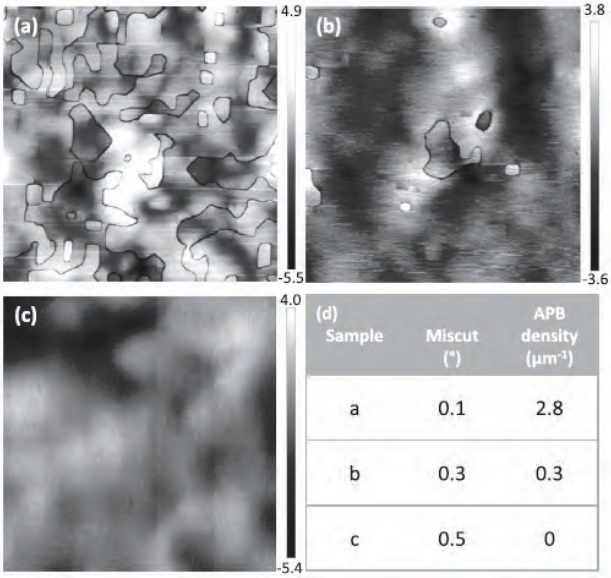
P and As-based cubic III-V semiconductors (such as GaAs, InGaAs or InP) are interesting for the fabrication of n-type Metal Oxide Semiconductor Field Effect Transistors, as they possess superior electron mobilities compared to Si (at room temperature: 8500, 5400 and 40 000 $cm^2 V^{-1} s^{-1}$ in GaAs, InP and InAs compared to 1400 $cm^2 V^{-1} s^{-1}$ only in Si). Their Very Large Scale Integration is far from being easy. Among different process modules required for III-V devices, we focused on 300 mm substrate elaboration and contact technology. GaAs or InP substrates are expensive, hard to come by in large diameters and brittle. Being able to use 300 mm Si(001) substrates as templates for the growth of high crystalline and electronic quality would be a major advantage. Nevertheless, we have to face numerous growth challenges: misfit dislocations and Anti-Phase Boundaries (APB). Moreover, the complete performances of III-V materials could only be achieved with an optimized contact module (surface preparation and metallization) leading to ideal current's injection.

Main Results

In 2015, Leti has evaluated the impact of the misorientation angle of the starting Si(001) substrate on the properties of a GaAs layer grown on top of one micron thick Ge buffer (with almost the same lattice parameter than that of GaAs, which is a boon). We have shown that misorientation angles as low as 0.5° were enough to obtain smooth, APB-free GaAs films with Threading Dislocations Densities slightly above 10^7 cm^{-2} (see Fig. 1) [1]. This was due to the presence on slightly vicinal Ge of a regular array of tens of nm long terraces separated by bi-atomic step edges.

Leti has otherwise provided thick Ge buffers grown on 6°off Si(001) wafers to the IBM Zürich Laboratory. They were used them as templates for the growth of APB-free, high crystalline quality {GaAs/InAlAs graded buffer/InGaAs} stacks. The resulting heterostructures were used later on as donor wafers for the fabrication of InGaAs-On-Insulator substrates then of fin-type FETs (see Fig. 2) [2].

Finally, Leti has shown that HCl, HF, NH_4OH and $(NH_4)_2S$ were efficient in order to remove native oxide on GaAs wafers [3] (although S-passivation was mandatory to minimize oxide re-growth in the air). S-free alternatives have been investigated. Indeed, wet chemical cleaning in concentrated HCl solutions followed by argon or helium direct plasmas is efficient to remove InGaAs and InP native oxides. However, InP surfaces are more sensitive to surface preparation treatments and He direct plasma preceding by diluted HCl solution cleaning appears to be a better surface deterioration / oxide removal compromise [4].



(d)

Sample	Miscut (°)	APB density (μm^{-1})
a	0.1	2.8
b	0.3	0.3
c	0.5	0

Figure 1: 5x5 μm^2 Atomic Force Microscopy images of the surface of GaAs layers grown on Ge buffered Si(001) substrates with three offcut angles: (a) 0.1°, (b) 0.3°, (c) 0.5°. The resulting APB densities are provided in table (d).

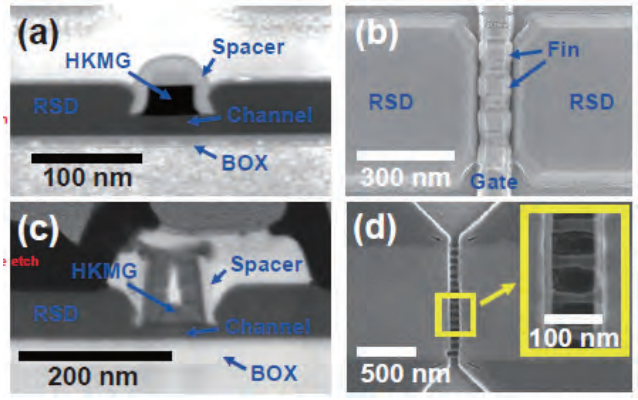


Figure 2: Cross sectional and top view Scanning Electron Microscopy images of "Gate First" (a, b) and "Replacement Metal Gate (c, d) FinFETs built on top of InGaAs-O-I substrates.

Perspectives

Leti will evaluate in 2016 the impact of the Ge buffer thickness on the properties of GaAs layers grown on top, the aim being to identify the right trade-off in terms of wafer bow (which increases with the overall thickness), TDD densities, surface roughness and so on. We will then focus on the properties of InP or graded InAlAs buffers grown on top of such optimized GaAs/Ge/Si(001) 0.5° stacks.

Related Publications

[1] Y. Bogumilowicz, J.M. Hartmann, R. Cipro, R. Alcotte, M. Martin, F. Bassani, J. Moeyaert, T. Baron, J.B. Pin, X. Bao, Z. Ye, E. Sanchez, "Anti-phase boundaries–Free GaAs epilayers on "quasi-nominal" Ge-buffered silicon substrates", , *Appl. Phys. Lett*. 107, 212105 (2015).

[2] V. Djara *et al*, "An InGaAs on Si Platform for CMOS with 200 mm InGaAs-OI Substrate, Gate-first, Replacement Gate Planar and FinFETs Down to 120 nm Contact Pitch", *Proceedings of the 2015 VLSI Technology Symposium*, Kyoto (Japan), June 2015.

[3] M. Rebaud, M.C. Roure, V. Loup, Ph. Rodriguez, E. Martinez, P. Besson, "Chemical Treatments for Native Oxide Removal of GaAs Wafers", *ECS Transactions*, 69 (8) 243-250 (2015).

[4] Ph. Rodriguez, L. Toselli, E. Ghegin, M. Rebaud, N. Rochat, N. Chevalier, E. Martinez and F. Nemouchi, "Cleaning of InGaAs and InP Layers for Nanoelectronics and Photonics Contact Technology Applications", *ECS Transactions*, 69 (8) 251 (2015).

Surface Organometallic Chemistry for Molecular Layer Doping (MLD) and the Synthesis of MoS_2

Research topics: MLD/ALD Organometallic, Molecules, Grafting, MoS_2

T. Alphazan, S. Cadot, F. Martin, N. Chevalier, J-P Barnes, M. Veillerot, D. Rouchon, F. Bertin, B. Grandidier (IEMN), C. Thieuleux, A. Quadrelli (CPE-C2P2), C. Copéret (ETH Zurich)

Partnership : CPE-C2P2, ETH Zurich, IEMN, INAC
Sponsorship: Nano2017

Context and Challenges

Surface functionalization and chemical reactions at the monolayer scale are increasingly present in the more advanced nano-electronic processing, like Molecular Layer Doping (MLD) for nanodevices, and 2D Transition Metal Dichalcogenides (TMD) deposition for emerging applications. LETI has then developed over the past 5 years his partnership with C2P2 Laboratory on the Nano-chemistry platform between CEA and CPE in Lyon. This allows quick synthesis of new molecules and introduction of such disruptive processes. Reaction mechanisms are thus investigated on high surface 3D silica nano-beds (by Diffuse Reflectance IR measurement, Microanalysis, gas chromatography of byproducts). Complementary experiments are also available through collaborations with ETH Zurich and IEMN Lille. We illustrate here the results dealing with Molecular Layer Doping and ALD of MoS_2 on 2D Silicon wafers, supported by this research on 3D Silica and the Nano-Characterization Platform in CEA-Leti.

Main Results

We aim to improve the efficiency of Molecular Layer Doping process. We optimized: i) bulkier Boron precursors to avoid the dopant evaporation during annealing (self-capping, Fig.1) ii) grafting on thin chemical oxide to avoid carbon contamination of silicon. We recently showed the benefit of dichloromethane versus toluene on grafting efficiency on 3D silica [1], giving a remarkably high dopant dose in silicon (Fig.1), i.e ~55% of the deposited boron (2.0E14 cm^2) diffused into the silicon without oxide cap.

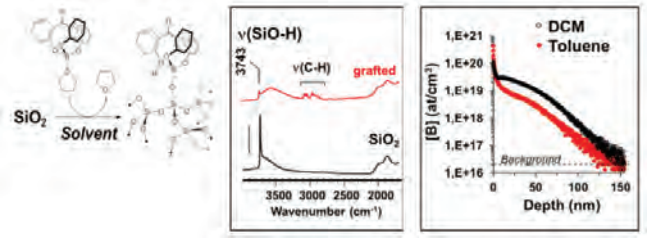


Figure 1 : left: grafting model of Tris(2-hydroxyphenyl)methane-borate Tetrahydrofuran adduct on Silica supported by FTIR on SiO_2 nano-beds (middle); right: Effect of solvent (dichloromethane or toluene) on total Boron dose diffused after anneal without cap.

Large area deposition of emerging 2D transition dichalcogenides (MoS_2, WS_2) by ALD is also a key issue for their future applications. We have screened new pairs of "green" precursors to avoid toxic H_2S reactant [2]. The IR measurements on 3D silica after each demi-cycle show the mechanisms of the ALD reaction between two organic Mo- and S-compounds thanks to the bifunctional 1,2Ethanedithiol molecule (Fig.2). The as formed Sulfur rich compound (S/Mo=3.3) then releases the organic ligand as ethylene during thermal treatment below 340°C as shown by IR measurements coupled with mass spectroscopy (Fig.3). After further annealing at 800°C, Raman spectrum shows ~2 monolayer MoS_2 as a final product, demonstrating the capability of such chemistry to grow emerging 2D TMD films on silica.

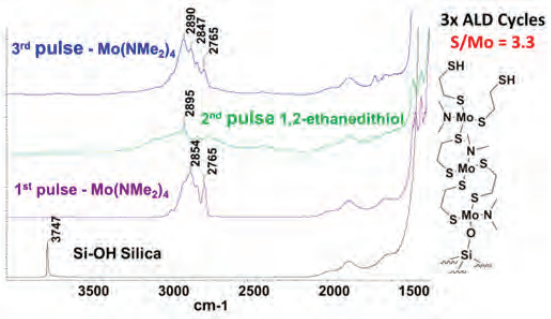


Figure 2: Diffuse Reflectance Infra-Red Fourier transformation (DRIFT) on 3 demi ALD cycles (Mo(NMe2)4 and 1,2-ethanedithiol) on silica. Final product after 3 full ALD cycles (Model).

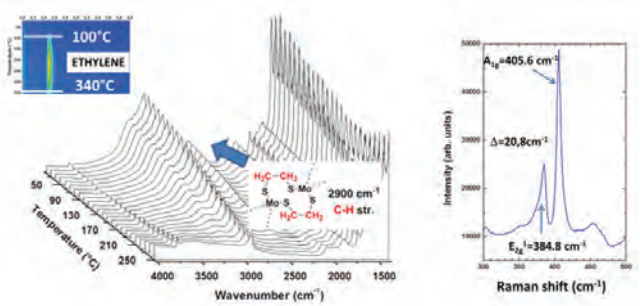


Figure 3: left: IR coupled with mass spectroscopy analysis during low temperature annealing of as grown compound (3 ALD cycles) showing the release of ethylene; right: Raman spectrum of MoS_2 (~2ML) after 800°C Argon anneal.

Perspectives

We are continuing to progress on the deposition of 2D Molecular Layers and films using a thorough understanding of the reaction mechanisms involved between new organometallic compounds and substrates. We are also investigating MLD for N doping on various semiconductors. We are improving our understanding on the effect of the starting substrate on final crystallinity of ALD and MOCVD grown 2D dichalcogenides, looking towards the emergence of microelectronic compatible, environmentally friendly, TMDs deposition for disruptive applications.

Related Publications

[1] L. Mathey, T. Alphazan, M. Valla, L. Veyre, H. Fontaine, V. Enyedi, K. Yckache, M. Danielou, S. Kerdiles, J. Guerrero, J-P Barnes, M. Veillerot, N. Chevalier, D. Mariolle, F. Bertin, C. Durand, M. Berthe, J. Dendooven, F. Martin, C. Thieuleux, B. Grandidier, C. Copéret; "Functionalization of Silica Nanoparticles and Native Silicon Oxide with Tailored Boron-Molecular Precursors for Efficient and Predictive P-Doping of Silicon"; *J. Phys. Chem. C*, Vol 119, 13750, 2015.

[2] S. Cadot, F. Martin, O. Renault, M. Fregnaux, D. Rouchon, E. Nolot, L.Veyre, C. Thieuleux, E. A. Quadrelli; "Low-temperature Atomic Layer Deposition of MoS2 using a novel organometallic precursor", *Extended Abstract of the 15th International Conference on Atomic Layer Deposition*, 29th June-1st July 2015.

PhD Degrees Awarded in 2015

Masahiro KOYAMA

Grenoble Alpes University, France

Electrical characterization of interface properties in nano-scaled MOSFET devices based on low-frequency fluctuations

In this thesis, electrical properties of gate oxide/channel interface in ultra-scaled nanowire (NW) MOSFETs were experimentally investigated by carrier transport and low-frequency noise (LFN) characterizations. NW FETs, which have aggressively downscaled cross-section of the body, are strong candidates for near future CMOS node. However, the interface quality could be a critical issue due to the large surface/volume ratio, the multiple surface orientations, and additional strain technology to enhance the performance.

Omega-gate NW FETs were fabricated from FD-SOI substrates, and with Hf-based high-k/metal gate (HfSiON/TiN), reducing detrimental effects by device downscaling.

Firstly, the most common Id-Vg was characterized in single-channel NW FETs as the basic performance. Reference SOI NWs provided the excellent static control down to short channel of 17nm. Stressors dramatically enhanced on-current owing to a modification of channel energy-band structure. Then, extracted low-field mobility in NWs also showed large improvement of the performance by stressors.

Next, LFN investigated for various technological and architectural parameters. Carrier number fluctuations with correlated mobility fluctuations (CNF+CMF) model described 1/f noise in all our FETs down to the shortest NWs. Drain current noise behavior was basically similar in both N- and PMOS FETs regardless of technological splits. Larger 1/f noise stemming from S/D regions in PMOS FETs was perfectly interpreted by the CNF+CMF model completed with Rsd fluctuations. This observation highlighted an advantage of SGOI NW with the lowest level of S/D region noise. Geometrical variations altered the CNF component with simple impact of device scaling (reciprocal to both Wtot and Lg). No large impact of surface orientation difference between the channel (100) top and (110) side-walls in [110]-oriented NWs was observed. Scaling regularity with both Wtot and Lg, without much quantum effect, could be attributed to the use of HfSiON/TiN gate and carrier transport occurring mostly near top and side-wall surfaces even in NW geometry. Meanwhile, the CMF factor was not altered by decreasing dimensions, while the mobility strongly depends on the impact. Extracted oxide trap density was roughly steady with scaling, structure, and technological parameter impacts. Simple separation method of the contributions between channel top surface and side-walls was demonstrated in order to evaluate the difference. It revealed that oxide quality on (100) top and (110) side-walls was roughly comparable in all the [110]-devices. The density values lie in similar order as the recent reports.

Finally, our NWs fulfilled 1/f LFN requirements stated in the ITRS 2013 for future MG CMOS logic node. Consequently, we concluded that appropriate strain technologies powerfully improve both carrier transport and LFN property for future CMOS circuits consisting of NW FETs, without any large concern about the interface quality.

Onintza ROS BENGOECHEA

Grenoble Alpes University, France

Development and characterization of plasma etching processes for the dimensional control and LWR issues during High-k Metal gate stack patterning for 14FDSOI technologies

In a transistor manufacturing process, patterning is one of the hardest stages to control. Along with downscaling, the specifications for a transistor manufacturing have tightened up to the nanometer scale. Extreme metrology and process control are required and Critical Dimension Uniformity (CDU) and Line Width Roughness (LWR) have become two of the most important parameters to control. So far, to meet the requirements of the latest CMOS technologies, post-lithography treatments such as plasma cure treatments have been introduced to increase photo-resist stability and to improve LWR prior to pattern transfer. However, conventional post-lithography treatments are no more efficient to address the specifications of 14nm gate patterning where more complicated designs are involved. In this work, we have studied limitations of cure pretreatments in 2D gate integrations. In fact, the HBr plasma post-lithography treatment was identified as being responsible of a local pattern shifting that result in a loss of the device's electrical performance. Preliminary results show that, cure step removal helps to control pattern shifting but to the detriment of the LWR. Indeed, if no cure treatment is introduced in the gate patterning process flow, photoresist patterns undergo severe stress during the subsequent Si-ARC plasma etching in fluorocarbon based plasmas. In this work, the mechanisms that drive such resist degradation in fluorocarbon plasmas have been studied and improved SiARC etch process condition shave been proposed. Besides, we evaluate how the state-of-art gate etch process can be improved, by investigating the impact of each plasma etching step involved in the high-K metal gate patterning on both LWR and gate shifting. The goal of this study is to determine if the TiN metal gate roughness can be modified by changing the gate etch process conditions. Our research reveals that addition of N2 flash steps prevents from gate profile degradation and sidewall roughening. In revenge, the TiN microstructure as well as the HKMG etch process has no impact on the gate final roughness. However, the TiN LER is strongly modified during the wet cleaning process. This modification results from the dissolution of TiN sidewall passivation layers that are formed during plasma processing. Although the TiN LER is also modified during wet process, the hard mask patterning process still remains the main contributor for gate roughening.

Alexandre SUBIRATS

Grenoble Alpes University, France

Characterization and modelling of the reliability due to carrier trapping in decananometer transistors and SRAM memory fabricated in FDSOI technology

Nowadays, microelectronic industry is able to manufacture transistors with gate length down to 30nm. At such scales, the variability and reliability issues are a growing concern. Hence, understanding the interplay between these two concerns is essential to guarantee good lifetime estimation of the devices. Currently, the Bias Temperature Instability (BTI), which is mostly due to the carrier trapping occurring in the gate oxide, appears to be the principal source of degradation responsible for the ageing of transistor device. This manuscript presents a complete study of the BTI degradation occurring on small and big transistors and on Static Random Access Memory (SRAM) cells. Thus, as a first step, several electrical characterization techniques to evaluate the BTI degradation are presented. The necessity of fast measurement in order to avoid most of the relaxation effect occurring after the BTI stress is emphasized. Then, using these fast measurement techniques, a complete study of the Negative BTI (NBTI) on large devices is presented. Then, the manuscript focuses on the small devices: transistors and memory cells. First, a modeling of the trapping mechanism in the gate oxide of small transistor is presented. In particular, 3D electrostatic simulations allowed us to understand the particular influence of the traps over the threshold voltage (VT) of the small transistors. Finally, the case of the SRAM is studied. Finally, the impact of the degradation occurring at transistor level and impacting the functioning of the SRAM bitcells is investigated.

Issam OUERGHI

Grenoble Alpes University, France

Study of polycrystalline nanowire based NEMS for detection and ultra-dense 3D heterogeneous integration

Recently, technological advances lead to a very large scale integration (VLSI) of microelectronics components at the nanoscale. Faced with the traditional miniaturization limits, the three dimensions (3D) integration open the door to heterogeneous miniaturized devices, with new chip generations. At the same time, new concepts such as junctionless nanowires and polycrystalline silicon nanowires allow to imagine low temperature processes and low-cost devices for a 3D integration on a stabilized CMOS. Poly-silicon nanowire based NEMS on CMOS for mass detection is a new "More-Than-Moore" opportunity. The NEMS could be arranged in a dense network like memory and image sensor architectures. The individual addressing of each NEMS, the functionalization for the detection of specific molecules within a large area (VLSI), allow the implementation of a new type of Multi-physics sensors, compact and highly sensitive. The purpose of this thesis has been the manufacturing and the performance evaluation of poly-silicon nanowire based NEMS. The challenge was to find the best processes with a back-end compatible thermal budget. A rigorous study of the layer physicochemical properties has been correlated with the electrical, mechanical performances and the yield of poly-silicon NEMS. This allowed us to make a selection of the best fabrication processes. NEMS manufactured at very low temperature with an active layer deposited at room temperature and recrystallized by a laser annealing exhibited high performances in terms of transduction (piezoresistivity) and frequency stability comparable to monocrystalline references. Polycrystalline silicon.

Manuela AOUKAR

Grenoble Alpes University, France

Deposition of phase change materials using pulsed-liquid injection PE-MOCVD for PCRAM based memory applications

Phase change random access memories PCRAM are based on the fast and reversible switch between the high resistive amorphous state and the low resistive crystalline state of a phase change material (PCM). These memories are considered to be one of the most promising candidates for the next generation of non volatile memories thanks to their unique set of features such as fast programming speed, multi-level storage capability, good endurance and high scalability. However, high power consumption during the RESET operation (IRESET) is the main challenge that PCRAM has to face in order to explode the non volatile memory market. In this context, it has been demonstrated that by integrating the phase change material (PCM) in high aspect ratio lithographic structures, the heating efficiency is improved leading to a reduced reset current. In order to fill such confined structures with the phase change material, a highly conformal deposition process is required. Therefore, a pulsed liquid injection Plasma Enhanced-Metal Organic Chemical Vapor Deposition process (PEMOCVD) was developed in this work. First, amorphous and homogeneous GeTe films were deposited using the organometallic precursors TDMAGe and DIPTe as Ge and Te precursors. XPS measurements revealed a stoichiometric composition of GeTe but with high carbon contamination. Thus, one of the objectives of this work was to reduce the carbon contamination and to optimize the phase change properties of the deposited PCMs. The effect of deposition parameters such as plasma power, pressure and gas rate on the carbon contamination is then presented. By tuning and optimizing deposition parameters, GeTe films with carbon level as low at 2 at. % were obtained.

Athanasios KIOUSELOGLOU

Grenoble Alpes University, France

Characterization and design of architectures for phase-change memories based on alternative-to-GST materials

Semiconductor memory has always been an indispensable component of modern electronic systems. The increasing demand for highly scaled memory devices has led to the development of reliable non-volatile memories that are used in computing systems for permanent data storage and are capable of achieving high data rates, with the same or lower power dissipation levels as those of current advanced memory solutions. Among the emerging non-volatile memory technologies, Phase Change Memory (PCM) is the most promising candidate to replace conventional Flash memory technology. PCM offers a wide variety of features, such as fast read and write access, excellent scalability potential,

baseline CMOS compatibility and exceptional high temperature data retention and endurance performances, and can therefore pave the way for applications not only in memory devices, but also in energy demanding, high-performance computer systems. However, some reliability issues still need to be addressed in order for PCM to establish itself as a competitive Flash memory replacement.
This work focuses on the study of embedded Phase Change Memory in order to optimize device performance and propose solutions to overcome the key bottlenecks of the technology, targeting high-temperature applications. In order to enhance the reliability of the technology, the stoichiometry of the phase change material was appropriately engineered and dopants were added, resulting in an optimized thermal stability of the device. A decrease in the programming speed of the memory technology was also reported, along with a residual resistivity drift of the low resistance state towards higher resistance values over time. A novel programming technique was introduced, thanks to which the programming speed of the devices was improved and, at the same time, the resistance drift phenomenon could be successfully addressed. Moreover, an algorithm for programming PCM devices to multiple bits per cell using a single-pulse procedure was also presented. A pulse generator dedicated to provide the desired voltage pulses at its output was designed and experimentally tested, fitting the programming demands of a wide variety of materials under study and enabling accurate programming targeting the performance optimization of the technology.

Sarra SOUIKI
Grenoble Alpes University, France

Reliability study of PCRAM cells : analysis and optimization of the stability of programmed states

Nowadays, new technologies are rising steadily and forming an integral part in the daily lives of everyone. They take advantage of the development of electronic systems for which the complexity requires the use of memory devices more and more efficient and with large storage capacities. Because of some performance degradation, the scaling of Flash technology who was so far predominant in the non-volatile memories market, is today reaching its limits. As a result, different emerging resistive memories are being developed. Among them, the phase-change memory technology PCRAM is very attractive because of its non-volatility, scalability, as well as reduced cost compared to standard Flash. Nevertheless, to compete with other technologies and to address the embedded applications market, PCRAM still face some challenges, such as decreasing the programming current densities, increasing the programming speed and increasing the thermal stability of the two memory states. For that purpose, different solutions have been tried in the literature, including using new device architectures and optimized phase change materials.

In this work, we are interested in investigating the failure mechanisms that affect thermal and temporal stability of phase change memories, in particular the retention of the RESET state and the stability of the programmed states disturbed by the drift phenomenon. The development of alternative materials using an optimized stoichiometry or incorporating doping allows us to achieve high electrical performance devices and to reach the required retention properties of embedded applications and particularly the automotive one. Moreover, thanks to the development of a new pre-coding procedure, these devices allow to keep stable the preprogrammed data on the memory chip during the soldering step of the latter on the electronic circuit. They represent a promising solution for Smart-Card applications. Finally, we have proposed an optimized programming procedure which enables to reduce the drift effect of the resistance of the SET state observed for optimized materials. This drift phenomenon was investigated by using low frequency noise measurements. Therefore, we have shown that this effect is due to the structural relaxation of amorphous parts in the active material. Besides, we highlighted for the first time the major influence of interface defects on the low-frequency noise of this state.

Boubacar TRAORE
Grenoble Alpes University, France

Investigation of HfO2 based resistive RAM cells by electrical characterization and atomistic simulations

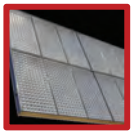
Among non-volatile memory technologies, NAND Flash represents a significant portion in the IC market and has benefitted from the traditional scaling of semi-conductor industry allowing its high density integration. However, this scaling seems to be problematic beyond the 22 nm node. In an effort to go beyond this scaling limitation, alternative memory solutions are proposed among which Resistive RAM (RRAM) stands out as a serious candidate for NAND Flash replacement. Hence, in this PhD thesis we try to respond to many open questions about RRAM devices based on hafnium oxide (HfO2), in particular, by addressing the lack of detailed physical comprehension about their operation and reliability. The impact of scaling, the role of electrodes, the process of defects formation and diffusion are investigated. The impact of alloying/doping HfO2 with other materials for improved RRAM performance is also studied. Finally, our study attempts to provide some answers on the conductive filament formation, its stability and possible composition.

Philippe BEZARD

Grenoble Alpes University, France

Development of innovating plasma etching processes for sub 14nm nodes by coupling conventional lithography with auto aligned approach based on block copolymer

Shrinking transistor's dimensions below 14 nm is so expensive that lower-cost complementary techniques such as Directed Self-Assembly (DSA) combined with 193 nm-lithography are currently being developed. Either organized as trenches for the FinFET's fin or vertical cylinders for contact holes (which is our case study), Polystyrene-b-polymethyl metacrylate (PS-b-PMMA) is a well-studied block copolymer but introduces challenging etching issues due to the chemical similarities between the PS and PMMA blocks. The aim of this thesis is to overcome those etching challenges. In our case where PS is the dominant phase, the principle of DSA is to obtain through self-assembly a pattern of vertical cylinders of PMMA inside a mask constituted of PS. PMMA is then removed either by solvent or plasma, revealing the patterns in the PS mask, which will be used as an etching mask for pattern transfer. In order to allow self-assembly, a thin brush layer of random copolymers PS-r-PMMA is used to neutralize the affinity of each phase with the substrate. One of the main issues with DSA is the control of the dimensions (CD control): usually, PMMA is dissolved in acetic acid bath and the brush layer is etched by an Ar/O2 plasma which increases dramatically the pore's diameter (CD) by laterally etching the PS. Short duration of thermal annealing suitable for the Industry induces some "mushroom" shape at the top of the mask which consequently increases the measured CD dispersion (~ 4-5 nm).Our work shows that CD uniformity can be corrected by faceting the top of the patterns through plasma etching. As a first step, a dry-etch process for PMMA based on H2N2 chemistry has been developed in order to free ourselves from acetic-acid's and O2-based plasma's issues. As far as we know, the discovered kind of defects has never been reported in the literature: few nanometer-thick films made of PS can randomly be found in the PMMA's domain, thus delaying the etching of random cylinders. In order to etch those defects without loosing the CD control, an other process constituted of an acetic acid bath followed by a synchronously-pulsed H2N2 plasma at low duty cycle and high bias power has been developed. This process removes PMMA, facets the top of the PS features (decreasing CD dispersion below 2 nm), etches both the defects mentioned above and the brush layer without increasing the pores' diameters by more than one nanometer. One last etching challenge comes from the aggressive dimensions and the high aspect ratio of the contact holes. In order to limit the lateral etching and the mask consumption overall, passivation's layer are usually deposed on the sidewall of the features during the etching process, but at dimensions below 15 nm, those layers are too thick and cause a CD control loss though they are only few-nanometer thick. The polymerization's capacity of plasmas has to be lowered at this scale and oxidized layer's formation by adding O2 to the plasma chemistry has to be avoided. Last but not least, the techniques based on SEM images to determine the pore's dimensions are not robust enough at those scales. In order to gain in robustness, image reconstruction and anti-aliasing algorithm have been implemented.

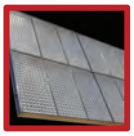


Jonathan LEHMANN

Grenoble Alpes University, France

Electrical characterization of AlGaN/GaN heterostructures for power applications

This PhD is part of the development of HEMT power transistor based on gallium nitride at Leti. Due to their high electron mobility, high breakdown field and good thermal conductivity, AlGaN/GaN HEMT are very promising devices for power electronic applications. The goal of this PhD is, using electrical characterization, to increase the knowledge of the AlGaN/GaN material prior to the fabrication of transistors. First, through measurements of the resistance of the electron gas located at the AlGaN/GaN interface, a trapping phenomenon was evidenced in the material. Then, in order to set a production follow-through of AlGaN/GaNon Si wafers, a method of measuring the sheet resistance of a AlGaN/GaN stack without the fabrication of contacts was developed and patented. Finally, on HEMT transistors fabricated using different epitaxies, a detailed study of the sheet resistance, the mobility and the sheet carrier density in and out of the gated area was carried out.

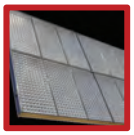


Elena Gusarova

Grenoble Alpes University, France

Flexible devices for energy harvesting based on printed organic piezoelectric P(VDF-TrFE) materials

This work aims to study innovative solutions for energy harvesting applicable to autonomous wireless sensors for IoT (Internet of Things). It is focused on flexible piezoelectric composite materials and a multi-physical approach. The objective is to harvest energy via strain-induced phenomena from both mechanical and thermal sources, and particularly sources neglected so far (slow and low). The main idea is the hybridization of different functional materials with the core of the system being screen printed piezo/pyroelectric microgenerators, mandatory to generate electrical charges. The originality of this work is to realize large area flexible energy harvesting systems by using ink-based piezoelectric copolymers of poly vinylidene fluoride P(VDF-TrFE). This material is very flexible and durable which makes it attractive for applications in systems with complex shapes. Another benefit of P(VDF-TrFE) is that it does not need to be pre-stretched as PVDF and it is now available in inks for printable electronics which can simplify and reduce the price of the fabrication process. We first describe the fabrication process of the screen printed P(VDF-TrFE) microgenerators, followed by ferroelectric and piezoelectric characterizations. For this purpose we have developed optimized methods in open-circuit conditions adapted for flexible systems tested and validated on commercial bulk PVDF. The last step was to realize a lowprofile thermal flexible energy harvester prototype (no radiator). It was done by hybridization of the fabricated microgenerators and foils of shape memory NiTi-based alloy, which is afunctional material sensitive to a given temperature threshold.The key outcomes of this work are: 1) the successful deposition of multilayers of P(VDF-TrFE) and organic PEDOT:PSS electrode, 2) dielectric, ferroelectric and direct piezoelectric constants reported as a function of film thickness, and 3) the g31 direct voltage coefficient, measured for the first time, and showing the record value of 0.15 V·m/N. Also, we have demonstrated that in open-circuit conditions, the microgenerators can produce a useful strain-induced voltage of 10 V with an energy density close to 500 µJ/cm3, these values being limited by the experimental set-up. The concept of thermal energy harvesting composite based on thin film screen printed P(VDF-TrFE) microgenerators was realized and demonstrated to be effective. We conclude with a functional prototype of flexible energy harvester, able to detect non-continuous slow thermal events and producing 37 V (corresponding to 95 µJ) at 65 ºC.

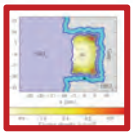


Xavier BLOT

Grenoble Alpes University, France

Processing, characterization and simulation of III-V compound semiconductor wafer bondings for concentrated photovoltaic

The solar photovoltaic is a promising way to support our economical growth while it can reduce the environmental impact of our society. But, to be truly competitive, the sector has to develop more efficient solar cells. An interesting option aims at combining different materials either by epitaxy growth and direct bonding. The Ph.D. was funded by the SOITEC company with the goal to develop the bonding of the gallium arsenide (GaAs) on the indium phosphide (InP) for the SmartCell architecture. We had to optimize its electrical behavior with a numerical model taking into account the bonding interface state. We introduce the study with a wide range of I(V) tools to precisely characterize the bonding interface. Depending on the case, we detail suitable metal contacts to improve the test. A study in deep of the GaAs/InP heterostructure and the GaAs/GaAs and the InP/InP homostructures leads to a better understanding of the bonding mechanisms. After a thermal annealing, the hydrophilic bonding process generates oxyde compounds at the interface which are absorbed in the InP case and are fragmented in the GaAs case. For given parameters, our stacks are electrically and mechanically better than the state of the art. Then we propose innovative processes to control the interface oxyde and thus optimize the heterostructure. Among them, we validate a new approach that leaves surface with a stable oxyde prior to bonding. The interface resistance of the stack is therefore closed to our best results and has great potentials. To conclude, the study focuses on a novel numerical model connecting the bonding process, the interface state and the electrical behavior. For a given annealing, the interface is heterogenous with reconstructed areas (thermoinic conduction) and oxyde areas (tunnel conduction). These regions are preferentially activated as a function of the operating temperature. They are weighted by a criteria determining the level of the bonding reconstruction which will be useful for the future developments of the application.

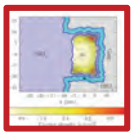


Sébastien GUARNAY

University of Paris Sud, France

Theoretical study of mobility degradation in FDSOI architectures for advanced technological nodes (< 20 nm)

To improve the MOSFET performances, it is necessary to understand the physical phenomena contributing to the apparent mobility of electrons and holes crossing the channel, and limiting the improvement obtained by reducing the channel length. Therefore, a precise study of transport using Monte Carlo simulations was performed. This semi-classical simulation method allows for solving the Boltzmann transport equation, taking into account the quasi-ballistic regime, phonon and Coulomb scattering, surface roughness, as well as the quantum confinement, by randomly generating electrons and their scattering events described by the laws of quantum mechanics. A simple mobility model has been established and validated by the simulations. It is based upon three important parameters: the long channel mobility, the access resistance, and ballistic resistance. This mobility model proved compatible with experimental results, suggesting that the access resistance is determining in the apparent mobility reduction. By the way, the ballistic transport contribution in the mobility was calculated by taking into account the quantum confinement accurately and the distribution functions of the different sub bands, allowing for an improvement of Shur's apparent mobility model, which underestimates (of about 50 Ω.µm) the ballistic resistance. The latter is lower than the access resistance but it could have an incidence on the ultimate devices.



Olivier NIER

Grenoble Alpes University (France) & Universita Degli Studi Di Udine (Italy)

Development of TCAD modeling for low field electronics transport and strain engineering in advanced Fully Depleted Silicon On Insulator (FDSOI) CMOS transistors

It is well known that that CMOS performances improvements in advanced technologies are not simply due to device dimension scaling but also to the introduction of new technological "boosters" such as new transistors architectures (FDSOI, trigate), high-k dielectric gate stacks, stress engineering or new channel material (Ge, III-V). To face all these technological challenges, Technology Computer Aided Design (TCAD) is a powerful tool to guide the development of advanced technologies but also to reduce time development and cost. In this context, this PhD work aimed at improving the modeling for 28/14 and 10FDSOI technologies with a particular attention on mechanical strain impacts. First of all, a review of the main models implemented in state of the art device simulators has been performed. The limitations and assumptions of these models are highlighted and development of the in-house STMicroelectronics solver for low field transport has been discussed. Then, a "top down" approach has also been set-up. It consists in using advanced physical-based solvers as a reference for TCAD empirical models calibration. Simulation has been compared with experiments: calibrated TCAD reproduced accurately split-CV mobility measurements varying the temperature, the back bias, the Interfacial Layer (IL) thickness and the stress configuration. Finally, a description of the methodologies used during this thesis to model stress induced by the process flow is performed. Simulations have been compared to nanobeam diffraction (NBD) strain measurements. The last part deals with TCAD modeling of advanced CMOS devices for 28/14 and 10FDSOI technology development. Mechanical simulations have been performed to model the stress profile in transistors and several solutions to optimize the stress configuration in sSOI and SiGe-based devices have been investigated.

Christophe DIEUDONNE

Grenoble Alpes University, France

Synchronization of a spin-transfer oscillator to a RF current: Mechanisms and characterization at room-temperature

Spin transfer oscillators (STOs) are promising nanometer scaled oscillators (~100nm) for radiofrequency applications. They rely on the steady precession of the magnetization of a thin magnetic layer induced by spin-transfer torque (STT). A STO device based on a magnetic tunnel junction (MTJ) will typically generate an electrical signal with a frequency of the order of ten GHz and an output power of several nW. Compared to voltage controlled oscillators (VCO) used today for microwave generation, STOs have the advantage of having an important frequency tunability with current. However, criteria in terms of the quality of the output signal are not yet fulfilled for STO to be competitive.

To enhance the STO signal properties, two suggestions are proposed: (i) optimization of the magnetic stack within a single STO device and (ii) synchronization of several STOs. The second approach was examined during this thesis: here we look at the electrical synchronization of a STO to a stabilized RF current source, or “injection-locking”. The case of a STO with homogenous magnetization of in-plane precession (IPP) type is investigated.

Interestingly, synchronization of a STO at 2f, i.e. when the frequency of the injected current is close to twice the generation frequency of the STO, is favored compared to synchronization at f. The experimental results from several groups have shown both enhanced synchronization range and a more pronounced linewidth reduction at 2f. This singular behavior is examined first through an analytical study of magnetization dynamics along with numerical macrospin simulations, in order to identify synchronization mechanisms taking effect in the system.

Indeed, current models (in particular the KTS auto-oscillator formalism) describe synchronization of a STO with making a clear distinction between synchronization at f and 2f, and the resulting predictions turn out to be insufficient at 2f. Here, by extension of the KTS formalism, the keys to the synchronization process at 2f are presented: frequency adjustment by adjustment of the oscillation amplitude via the STO non-linearity and modification of the anti-damping term through the phase-difference.

The experimental characterization of the synchronized regime in a MTJ-based STO is also detailed in the manuscript. Utilizing experimental signal processing techniques in both frequency and temporal domain, we extract characteristic quantities for synchronization such as the locking-range and the phase-difference, and we compare these quantities with the analytical predictions. Finally, the effects of current injection on the coherence of the output signal are also discussed.

Ossama EL BOUAYADI

Grenoble Alpes University, France

3D Integration of Wireless Systems at Millimeter-Wave Frequencies

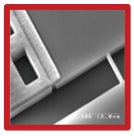
The evolution of semi-conductor technology nodes has led to a significant miniaturization of today’s RF front-ends and to the enhancement of the electrical performance of transceivers at higher frequencies. This leads to the diversification of RF/millimeter-wave (30 – 300 GHz) applications in the fields of telecommunications, multimedia entertainment, automotive and security. More specifically, telecommunications are going through a real revolution with the creation of new standards (such as WiGiG and IEEE 802.11ad) and the introduction of new network architectures based on point-to-point links as the backbone of the 5th generation of mobile networks. In this PhD work, we will focus on integrated wireless and low consumption modules operating in the 57 – 66 GHz band (generally designated as the 60 GHz band). At these frequencies, the free-space wavelength is comparable to the characteristic dimensions of most standard transceiver packages. This opens an opportunity to integrate the antennas as well as other passive components directly to the metal/dielectric stack or in the package. This new generation of electronic devices which are dedicated to the nomad terminal market brings new challenges in terms of electrical performance, mechanical reliability, cost and manufacturability. Microelectronic packaging plays in this case a key role in defining the global performance of the system. Its functions extend beyond the protection of the IC and cover other schemes with opportunities to integrate passive and active devices. This work focuses on the study of an SiP module (System-in-Package) featuring 3D integration on Silicon interposer. The dissertation comprises four chapters and is structured as follows: In the first chapter, a brief introduction of millimeter-waves and their propagation conditions is given. Then, examples of current and emerging civilian and military applications are addressed. State of the art of SiP/mmW modules is then presented according to different technology approaches proposed by industrial and academic contributors. The second chapter is dedicated to the study of a 60 GHz integrated module on a high resistivity silicon interposer chip. We focus on electrical characterization methods which are adapted to different building blocks of the silicon back-end technology. These include interconnects, dielectrics and integrated antennas. The characterization steps also include full-scale and standard compliant tests of two communicating 60 GHz modules. In the third chapter, we propose to improve the existing module with a novel antenna design based on a High-Impedance Surface (HIS) reflector. This design is intended to bring more compactness and higher reliability to the original one while conserving the overall electrical performance. Finally, the fourth chapter deals with the fabrications and experimental validation of the antenna test vehicle as well as the wideband characterization of the dielectrics used for the new stack.

Hélène TAKACS

Grenoble Alpes University, France

Magnetic nanocomposites with zero macroscopic conductivity for RF applications

Ultra-miniaturization of RF components faces a historical paradigm in magnetism: on one hand transition metals (Fe, Co, Ni) display the highest permeabilities but are too conductive. On the other hand, oxides are insulating but their properties are extremely low at high frequency. In that context, artificial magnetic materials based on metallic magnetic nanoparticles embedded in a polymer matrix could be an alternative. In this work, two nanocomposites formulations using sonochemistry were studied: one based on cobalt/polystyrene and the other on nickel/polystyrene. The originality lays on a core-double shell structure. The core is the metallic nanoparticle that provides high magnetization. The first shell is graphene (a few nm) that both ensures an efficient protection against oxidation and serves as a chemical functionalization surface. The second shell is an ultra-thin layer of polystyrene which role is to electrically insulate the nanoparticles and to promote a strong dipolar ferromagnetic order thanks to a well-controlled and short interparticle distance. At last the matrix is also polystyrene for chemical compatibility between functionalized nanoparticles and the matrix. In order to optimize the process, the formulations were first thoroughly characterized with the aim of improving nanoparticles dispersion, increasing interactions between the shells – by covalent or non-covalent grafting – as well as the suspensions stability. These formulations were then used to obtain micron-thick films by spincoating. Grafting is the key of a good mechanical cohesion. Original and reproducible spin-curves are established over a broad range of nanoparticles fraction in order to yield homogeneous and uniform films on 4-inch wafers. Two film deposition-related processes involving surface energy of the nanocomposites were developed for film planarization and transfer objectives. A great effort has been made for precisely understanding structural properties of such complex nanocomposites. A wide number of nanocharacterization techniques were used for determining hydrodynamic, structural, interfacial, thermal and chemical properties. Finally, functional properties – i.e. magnetic, electrical and radioeletric properties – are detailed with comparative analysis. Four results can be highlighted: 1) a high volume fraction of nanoparticles, close to physical boundary (~ 20 vol.%), 2) a unique combination of high magnetization (0.6 T) and high resistivity (1010 µΩ.cm), 3) a dual electrical percolative behavior (ohmic and tunnel) revealing at the same time local conduction defects by clusters, and 4) effective permeability and permittivity of around 1.5 and 3.0 up to ~ 15 GHz, respectively.

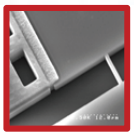


Jaroslaw CZARNY

INSA Lyon, France

Conception, fabrication and characterization of a MEMS microphone

Electret microphones dedicated to consumer electronics and medical applications (hearing aids) have reached the miniaturization limits. Since the release of the first microphone based on Silicon micromachining, electret microphones are constantly replaced by MEMS microphones. MEMS (Micro-Electro-Mechanical Systems) microphones use Silicon that provides exceptional mechanical characteristics along with good electric properties and mature fabrication technology. Regardless of the transduction principle (capacitive, piezoresistive, piezoelectric, optical), all of the MEMS microphones reported in the state of the art literature are based on a membrane deflecting out of the plane of the base wafer. Most of the reported microphones and all of the commercially available MEMS use capacitive transduction. Downscaling of capacitive microphones is problematic, since the sensitivity depends on capacitance value. Moreover capacitive sensors suffer of high sensitivity to parasitic capacitance and nonlinearity. The drawbacks of capacitive detection may be overcome with use of piezoresistive properties of Silicon nanowires. Unlike the classical piezoresistors integrated into silicon membrane, suspended nanowires do not suffer of leakage current. Further improvement of piezoresistive detection is possible since the longitudinal piezoresistive coefficient rises inversely proportional to nanowire section. This thesis presents the considerations of novel MEMS microphone architecture that uses microbeams which deflect in the plane of the base wafer. Signal transduction is achieved by piezoresistive nanogauges integrated in the microsystem and attached to the microbeams. Acoustic pressure fluctuations lead to the deflection of the microbeams which produces a stress concentration in the nanogauges. Accurate simulations of the discussed transducer couple acoustic, mechanical and electric behavior of the system. Due to micrometric dimensions of the MEMS acoustic system, thermal and viscous dissipative effects have to be taken into account. To reliably predict the sensor behavior two acoustic models are prepared: the complete Finite Element Model based on the full set of linearized Navier-Stokes equations and the approximative model based on the Lumped Elements (Equivalent Cirtuit Representation). Both models are complementary in the design process to finally retrieve the frequency response and the noise budget of the sensor. The work is completed by the description of the technological process and the challenges related to the prototype microfabrication. Then the approach to the MEMS microphone characterization in pressure-field and free-field is presented.

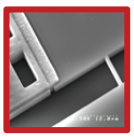


Veronika KOVACOVA

Grenoble Alpes University, France

Study of correlations between microstructure and piezoelectric properties of PZT thin films

MEMS have been developed since 1980, when they appeared as derivatives from the microelectronic industry. They were first used in accelerometers and car airbags. They have diversified since then and expanded. One of the main contributors to this expansion are piezoelectric materials. Among them, PbZrTiO3 (PZT) is widely used for its outstanding piezoelectric performances. Sol-gel PZT thin films fabricated at Leti are worldwide state of the art. In order to stay competitive, several R&D strategies have been developed. One of them is a detailed study of PZT microstructure in order to draw correlations with the piezoelectric effect in PZT films. The goal of this study is to optimize PZT microstructure aiming to reach its best piezoelectric properties. For this purpose, this thesis takes advantage of numerous studies performed on PZT bulk ceramics in order to analyze PZT thin films microstructure and its modifications with voltage. PZT bulk ceramics of morphotropic composition are now well known from the piezoelectric and microstructural point of view. There are several theories explaining the piezoelectric effect at the microscopic level, namely tetragonal and rhombohedral domain switching, rhombohedral nanodomains rearrangement, polarization axis rotation in the monoclinic phase and the phase transition. Morphotropic PZT thin films have emerged more recently. Their microstructure is very different from the bulk PZT. Indeed, sol-gel PZT films studied in this manuscript are stressed and contain preferred oriented nanoscale crystals and Ti/Zr composition gradient through the film thickness. Our goal is to study links between the complex microstructure of these films and their piezoelectric properties using X-ray diffraction (XRD).Thanks to the nano-beam at ESRF, we were able to study the influence of the Zr/Ti chemical gradient on the PZT microstructure. Our observations showed that the composition gradient gives rise to a variation of the tetragonal and rhombohedral phase ratio in the layer thickness. This variation follows Zr/Ti composition oscillations evidenced by SIMS. This experiment shows the sensitivity of PZT microstructure to the PZT chemical composition. At the same time, it suggests the possibility of improving the composition homogeneity of PZT and its performances. The more the PZT composition is homogeneous, the better the piezoelectric coefficients are. Then, we performed in-situ XRD under electric field experiments on a capacitor containing the PZT active layer with an attenuated Zr/Ti gradient. The PZT diffraction pattern was refined using the tetragonal and the rhombohedral PZT phases. At 0V PZT contains 40% of rhombohedral phase and 60% of tetragonal phase. At 30V, no tetragonal phase is observed any more. Results show an electric field induced phase transition from the tetragonal to the rhombohedral phase. Finally, we used in-situ XRD to study the influence of Zr/Ti composition gradient on the amplitude of the phase transition of two PZT samples with different Zr/Ti gradient. We showed that the more the sample is homogeneous in composition, the more phase transition it exhibits and the more it is performant. Finally, to improve the piezoelectric performances of PZT films, we propose to improve PZT compositional homogeneity and slightly increase the Ti content to promote the tetragonal phase in order to amplify the phase transition under voltage.

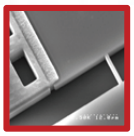


Guillaume LEHEE

Université Paris Saclay, France

Nanogauges based resonant pressure sensor for aeronautic application

The market of pressure sensors for aeronautics is mature but still strongly growing, defined by a strong added value and a large innovation need. Bringing pressure sensors closer to hot parts of the plane, requires, for example, to re-consider the sensor architecture, including the sensitive element. In order to comply with these requirements, we have developed a resonant pressure sensor with motion detection by Si piezoresistive nanowires. A simplified version of the resonator without these nanogauges has been modelled, fabricated and characterized to confirm its good operation. In parallel, electro-thermo-mechanical and noise characteristics of nanogauges coupled to M&NEMS resonators arising from previous works have been studied. We have notably demonstrated that the damped-spring behavior of an harmonically longitudinally stressed nanowire at low frequency could govern the MEMS resonator response, despite its tiny dimensions. Moreover, we have shown for the first time that the resonator response could be tuned “in situ” owing to the piezoresistive back action phenomenon only by acting on the nanowire biasing. Eventually, the theoretical performances of the resonant pressure sensor have been estimated from experimental data on different kind of M&NEMS resonator. These theoretical performances satisfy the sensor specifications; nevertheless they need to be confirmed experimentally.



Jérémy RUELLAN

Grenoble Alpes University, France

Design, fabrication and characterization of a silicon nanowire based thermal conductivity detector

Semiconducting nanowires are nowadays the topic of numerous research for their interesting physical properties. Relying more specifically on the thermal properties of nanostructures, the purpose of this thesis is to demonstrate the feasibility of a thermal conductivity detector based on silicon nanowires for pressure sensing (Pirani gauge) or gas detection. The work presented herein addresses the questions raised by the reduction of the objects size such as the increase of the noise or the thermal conduction in a rarefied gas and tries to bring a solution to those problematics. This work deals with all the steps required for the realization of such devices. That is, the design and simulation of the sensor, based on a detailed study of the physical behavior of the objects, the fabrication of such devices on 200mm wafers by the Leti cleanroom using standard microelectronics processes and finally their characterization as a pressure sensor and gas detector. The work presented here is part of a wider project that aims at developing of a portable gas detection system for air or water analysis.

Simon GOUSSEAU

Mines Paris tech, France

In Operando Characterization of Electromigration-Induced Damaging in 3D Interconnects/ Toward a predictive finite elements model

3D integration, conception mode of chips stacking, aims at both systems densification and functions diversification. The downsizing of 3D interconnects dimensions and the increase of current density rise the hazard related to electromigration. An accurate knowledge of the phenomenon is required to develop a predictive modeling of the failure in order to anticipate the difficulties as soon as the stage of technologies conception. Thus, a hitherto unseen SEM in operando observation method is devised. The test structure with “high density” through silicon vias (TSV) is tested at 350 °C with an injected current density of about 1 MA/cm², and simultaneously characterized. Regular shots of micrographs inform about the voids nucleation, forced in copper lines above the TSV, and about the scenario of their evolution. Islets formation and voids curing are also observed during the tens to hundreds hours of tests. A clear relation is established between voids evolution and the one of the electrical resistance. The different tests, completed by post-mortem analyses (FIB-SEM, EBSD, TEM), demonstrate the impact of microstructure on the depletion mechanism. Grains boundaries are preferential voids nucleation sites and influence the voids evolution. A probable effect of grains size and crystallographic orientation is revealed. Finally, the study focuses on the implementation of a multiphysics modeling in a finite elements code of the voids nucleation phase. This modeling is constituted of the main terms of the migration management.

Olivier GUILLER

Grenoble Alpes University, France

Through silicon capacitor integration on silicon interposer

Integrated circuits density never stopped rising since the discovery of the transistor in 1947, through components size shrinking. However, this miniaturization now encounters barriers and reduction of transistor’s gate size alone no longer allows integrated circuits overall performances increase. Therefore, microelectronic industry turned to new heterogeneous integration solutions aiming to develop the diversification of functionalities offered by the circuits. Among these solutions, 3D integration involving stacking several silicon dies on top of each other with the help of Through Silicon Vias (TSV) appears to be promising. Nevertheless, such structures will take times to reach maturity since they require the evolution of the whole industrial ecosystem. A transitional solution in term of technological maturity lies in the use of the interposer: a thinned substrate placed between the high density silicon dies and the Ball Grid Array acting as an integration platform allowing side by side placement of heterogeneous dies as well as high density interconnections. However, the addition of the interposer in the system leads to the increase of the Power Delivery Network impedance. The integration of a decoupling capacitor on the interposer resolves this issue by ensuring power integrity within 3D structures.

The objective of this PhD thesis consists in the study of different aspects of a new kind of integrated capacitor within the silicon interposer. This 3D Metal-Insulator-Metal (MIM) capacitor has the particularity to cross over the whole silicon interposer's thickness and to be co-integrated with TSV. The first step of this new integrated component study has been the definition of an efficient architecture, achieved through a modeling study allowing the influence evaluation of the numerous geometrical and material parameters coming into play. This modeling study pointed out the low ESR and ESL values achievable by the structure (in the mΩ and fH range respectively). Then, the fabrication of the capacitor required the development of innovative process steps allowing the deposition of a MIM stack in deep vias matrices as well as co-integration with TSV. Finally, component performances have been evaluated through the fabrication of a test demonstrator as well as a finites elements electromagnetic simulation campaign. A capacitance density of 20 nF.mm² has been reached on this demonstrator, showing an increase up to a factor 6 compared to a planar structure.

Sébastien MERMOZ

Grenoble Alpes University, France

Die to wafer assembly with capillarity self-alignment and direct bonding assembly

Among the various techniques allowing assembling both mechanically and electrically stacked chips, the direct bonding of Cu-SiO2 mixed surfaces is the most promising option to date. Thanks to this method, the interconnection density of 106/cm² aimed by the industry is achievable, while providing a low contact resistivity and excellent reliability. Current assemblies' processes are based on Pick&place tools thanks to which the dies are mechanically placed. Nevertheless, these tools have difficulties to council high throughput and high alignment accuracy. This PhD proposes to address this issue through the development of a process of self-assembly assisted by capillary forces and direct bonding. Through the use of capillaries forces, it is possible to achieve spontaneously chips alignment: it is called self-assembly. The first part of this manuscript presents a synthetic analysis of the different assemblies and interconnections technics and decides on the maturity of each process. As the same time, this section allows to introduce the SiO2 -SiO2 bonding mechanisms underlying the assembly method developed in this manuscript. A specific chip design is then established in a second part allowing deploying self-assemblies with SiO2 full sheet chips. The ability of the chip to confine the liquid film appears as the driving element of the self- alignment process. Self- assemblies with alignment values lower than one micrometer are obtained while maintaining a repeatable process. The introduction of numerical simulations to model the self-alignment effect is presented in the third part. This model was then generalized has polygonal shaped chips. Finally the last part presents the transfer of the self- assembly process on SiO2-Cu patterned chips. The use of this kind of chip has enabled to validate the electrical viability of the self-assembly process.

Yann BEILLIARD

Grenoble Alpes University, France

Direct bonding analysis of patterned copper –oxide surface integration, implementation in a 3D-SIC architecture

The context of this work is the three-dimensional integration of electronic devices. Among the various techniques allowing to assemble both mechanically and electrically stacked chips, the direct bonding of Cu-SiO2 mixed surfaces is the most promising option to date. Thanks to this method, the interconnection density of 106/cm² aimed by the industry is achievable, while providing a low contact resistivity and excellent reliability.

The objective of this study is to demonstrate the compatibility of the direct hybrid bonding Cu-SiO2 process with integrations and architectures that mimic real circuits. For this purpose, test vehicles incorporating two-layer and four-layer copper test structures have been specifically designed. Furthermore, finite element simulations of the direct bonding process have been developed within the Abaqus software. First, the 200 and 300 mm chip-to-wafer direct bonding process is validated. Morphological and electrical characterizations show that this stacking method does not deteriorate the integrity and performances of two-layer test structures with respect to a wafer-to-wafer integration. Furthermore, thermal cycling tests confirm the excellent mechanical strength of the bonded dies. The second part of this work focuses on morphological, electrical and reliability characterizations of four-layer test structures. In this case, the 200 mm wafer-to-wafer architecture of the test vehicles is close to an industrial integration. The various observations conducted with scanning and transmission electron microscopy indicate an excellent bonding quality of Cu/Cu and SiO2/SiO2 interfaces. Furthermore, the formation mechanisms of cavities at the Cu/Cu interface and the copper diffusion phenomenon in the silica are investigated. Electrical characterizations show functional yields above 95 % and standard deviations below 3 % after annealing at 200 or 400 °C. Finally, reliability studies including unbiased HAST, thermal cycling, temperature storage and électromigration test prove the resistance to corrosion and the mechanical robustness of this integration.

Finally, the finite element simulations indicate that the cohesive interactions at the bonding interface, combined with the thermal expansion of the copper during the annealing, significantly assist the bonding process of copper surfaces with a dishing effect. In addition, the macroscopic plastic deformation of the copper appears to have a detrimental effect on the sealing of the interface by slowing the propagation of the bonding wave.

Jorge Mario HERRERA-MORALES

Grenoble Alpes University, France

Evaluating biocompatible barrier films as encapsulants of medical micro devices

Miniaturized medical devices are becoming increasingly adopted by doctors and patients because they enable new treatment and monitoring capabilities, minimally invasive surgery, improved portability and ease of use. Recent examples include micro pacemakers, micro cochlear implants and ex-situ micro glucose sensors. However, implantable micro devices employing packaging technologies other than metallic enclosures are yet to be seen. Physiological monitors such as in-situ pressure sensors and BioMEMS could profit significantly from advances in thin barrier films for corrosion protection of silicon micro devices. Coating films that stop the diffusion and permeation of harmful substances are necessary to protect both the patient and the micro device. Ceramic films deposited by chemical vapor deposition techniques are good candidates for this task due to their low permeability to gases, low chemical reactivity and high conformality. However, few studies are available about the corrosion protection offered by biocompatible coatings to microelectronic devices in representative biological environments.Ten materials were selected in this thesis after a bibliographic study: Al2O3, BN, DLC, HfO2, SiC, SiN, SiO2, SiOC, TiO2 and ZnO. Ultra-thin films of these materials (5-100 nm) were deposited by plasma enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD) on substrates commonly found in electronic micro devices: crystalline silicon, copper, tungsten nitride and polyimide. In vitro cytotoxicity tests and degradation tests were performed for several weeks at different temperatures in Phosphate Buffer Saline (PBS) and NaCl supplemented with 10% Fetal Bovine Serum (NaCl/FBS). Changes in thickness and chemical composition were monitored by VASE, XPS and time-of-flight secondary ion mass spectroscopy (TOF-SIMS). It was found that SiO2 and SiN films (generally used for protection in the microelectronics industry) are not stable in PBS and NaCl/FBS at 37°C, even though they act as good hermetic barriers. Al2O3 showed very good stability in saline solution and excellent behavior as gas barrier, but it was rapidly dissolved in NaCl/FBS.In contrast, films of DLC, SiOC and TiO2 showed very low chemical reactivity in both mediums. Finally, it was shown that multilayers of TiO2 on Al2O3 offer the best performance as hermetic and diffusion barriers for corrosion protection of silicon micro systems in saline environments.

Bérenger CABY

Caen Normandie University, France

Development of X-ray Reflectomettry (XRR) and Grazing Incidence Xray Fluorescence (GIXRF) combined analysis for micro and nano electronic applications

Due to recent developments in microelectronics, new in-depth characterization techniques are needed. Combined Grazing Incidence X-ray Fluorescence (GIXRF) and X-ray Reflectivity (XRR) analysis is a promising alternative technique. Indeed, this technique allows to obtain, in a non-destructive way, the depth-profile composition and electron density of multilayered samples. In the literature, only few works using the potentiality of the XRR-GIXRF technique have been reported. Therefore, in order to accelerate the development of its application in materials characterization, a collaborative international group has been set up between laboratories to share expertise, equipment and analysis software. The objective was to apprehend the methodologies for the XRR-GIXRF acquisition, measurements analysis as well as the physical principles along with the possible limitations of the technique. In this work, after a presentation of the analysis protocols and software, the solutions implemented in different software in order to handle instrumental effects and quantification problems, are discussed. Subsequently, applications of the combined XRR-GIXRF technique on samples of interest are presented. In particular, through the investigation of Ultra-Shallow junctions and various multilayers, the qualitative and quantitative depth-profiling capabilities are demonstrated and compared to classical characterization techniques. Finally, limitations of the technique and possible outlooks are discussed.

Viktoriia GORBENKO

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Ion beam characterization of III-V heterostructures for micro- and opto-electronic applications

The integration of III-V semiconductor compounds on silicon should lead to the development of new highly efficient micro- and optoelectronic devices. High mobility InGaAs material is a promising candidate for n-channel metal-oxide-semiconductor-field-effect transistor beyond the 10 nm technology node. Moreover, III-V semiconductors are also suitable materials for fabrication of optical (lasers, diodes) and ultra-high frequency analog devices and their integration on a Si platform will add new functionalities for optical networks and communication. However, the miniaturization of devices and their integration into 3D architectures require the development of advanced characterization methods to provide information on their physico-chemical composition with nanometer scale resolution.

In this thesis, the physico-chemical studies of III-V heterostructures directly grown on 300 mm Si wafers by metalorganic vapor phase epitaxy are addressed. Secondary ion mass spectrometry (SIMS) techniques are used and developed in order to study interface abruptness, chemical composition and doping of III-V thin layers in 2D and 3D architectures with high depth resolution. The accurate quantitative analysis of InGaAs quantum wells (QWs) in 2D and 3D architectures was performed using magnetic SIMS and Auger techniques. To obtain the chemical profiling of narrow and repetitive III-V structures, an averaging profiling method was developed for both techniques. Additionally, 3D reconstruction and depth profiling of individual trenches (less than a hundred nanometers in width) containing thin InGaAs QWs selectively grown in silicon dioxide cavities using the aspect ratio trapping method were successfully obtained using Time-of-flight SIMS and atom probe tomography. Finally, the results were correlated with photoluminescence measurements.

Mathieu VIGOUROUX

Grenoble Alpes University, France

Investigation of nano crystalline materials strain and structure using high spatial resolution precession electron diffraction

Precession electron diffraction (PED) is a recent technique used to minimize acquired diffraction patterns dynamic effects. The primary intention of this PhD work is to improve PED (Precession Electron Diffraction) data analysis and treatment methodologies in order to measure the strain at the nanoscale. The strain measurement is intended to reach a 10-3 strain precision as well as usual microscopy techniques like high-resolution imaging. To this end, measurements were made with a JEOL 2010A with a Digistar Nanomegas precession module. The approach developed has been used and tested by measuring the strain in a Si/SiGe multilayered reference sample with a known Ge Content. Strain measurements reached 1x10-4 sensitivity with excellent finite element strain simulation agreement. This process has been also applied to measure the strain in microelectronic InGaAs Quantum Well and an "Ω-gate" experimental transistor devices. The second approach developed has been made to provide a robust means of studying electron transparent nanomaterial polycrystallinity with precession. Examples of applications of this analysis method are shown on different devices. Key words : Strain, deformation , polycrystallinity, precession electron diffraction (PED), strain relaxation, finite element simulation, Transmission Electron Microscopy (MET), SiGe, InGaAs, "Ω-gate" transistor, Phase-change memory (PRAM).

David LALOUM

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High resolution X-ray tomography - Application to 3D Integration for microelectronics

In microelectronics, 3D integration is a technology where chips are stacked on top of each other using for instance TSVs, copper pillars or bonding. Deep sub-micrometer resolution is therefore needed for failure analysis of such devices. X-ray tomography is a technique of choice because it gives the inner morphology of the sample in 3D in a non-destructive way. However, the resolution is limited to about a micrometer. Here, we propose to use x-ray tomography hosted in a scanning electron microscope (SEM) to analyze 3D integration components. The electron beam of the SEM is focused on a target whose geometry and materials can be tuned to produce an x-ray beam having a very small source size (<200nm) at typical energies of 8-10keV. The x-ray magnifying geometry allows for 3D imaging at sub-100nm resolution in 2D and 100-200nm in 3D. Using Xenon-based plasma-FIB, 100 micrometers samples could be prepared in few hours. The scanning time for tomography has been found to be a limiting factor and reconstruction algorithms based on a priori knowledge (total variation minimization, discrete tomography) have been used. Middle-TSVs, 5-25 micrometers copper pillars and more exotic materials have been used as textbook cases, showing the potential of the technique beyond microelectronics.

Sylvain POUCH

University of Lille, France

Nano characterization of materials used in photovoltaics by near-field microscopy and electron spectroscopy: work function and carrier lifetime measurements

Photovoltaic technologies represent a great hope for actual energetic issues. We are now working with the third generation of solar cells, composed of nano structured devices. At these levels, the performances measured by conventional techniques are averaged. In order to access local physical quantities, advanced characterization technics have to be developed.

The goal of this thesis is the local measurement of work function and carrier lifetime by atomic force microscopy and electron spectroscopy. After a historical overview on photovoltaic technologies and a detailed explanation of the operating principle of the characterization techniques, we present three studies:

1) A work function measurement on silicon-germanium heterostructures by XPEEM and KFM, to demonstrate the complementarity of these techniques. We saw that both are able of imaging small (10 meV) work function variations, and have revealed a contrast inversion effect due to a surface state.

2) A work function measurement by KFM on III-V materials. We saw that the maximum spatial resolution is dependent on a bend bending covering effect, highlighted with a self-consistent simulation of the surface potential.

3) A technique giving access to carrier lifetime mappings, through the acquisition of several KFM images as a function of frequency modulated illumination. This technique has been successfully applied to an PBTFB-PCBM organic solar cell.

Paul RISTERUCCI

University of Southern Denmark, Denmark

Elemental in-depth distribution of technological layered systems obtained from hard x-ray photoelectron spectroscopy peak shape analysis

This thesis tackles the challenge of probing in a non-destructive way deeply buried interfaces in multilayer stacks used in technologically-relevant devices with an innovative photoemission method based on Hard X-ray PhotoElectron Spectroscopy (HAXPES) and inelastic background analysis. In this thesis, a numerical procedure has been implemented to quantify the matching between a HAXPES measured inelastic background and a simulated inelastic background that is representative of a given depth distribution of the chemical elements. The method allows retrieving depth distributions at large depths via a semi-automated procedure. First, this method has been tested by studying an ultra-thin layer of lanthanum buried at depth >50 nm in a high-k metal gate sample. The influence of the parameters involved in the analysis is studied unraveling the primary importance of the inelastic scattering cross section. The combination of HAXPES with inelastic background analysis using this novel method maximizes the probing depth to an unprecedented level, allowing to probe the sample up to 65 nm below the surface with a high sensitivity to a nm-thick layer. Second, the previously-checked inelastic background analysis is combined with that of high resolution core-level spectra in the case of the source part of a high electron mobility transistor. The two analyses are complementary as they allow retrieving the elemental depth distribution and the chemical state, respectively. The result gives a complete picture of the elemental intermixing within the sample when it is annealed at various temperatures.

Tanguy TERLIER

Université Claude Bernard Lyon1, France

Elemental in-depth distribution of technological layered systems obtained from hard x-ray photoelectron spectroscopy peak shape analysis

During the last decade, organic electronics have developed rapidly. However, the production of organic electronic devices is still impeded because of various technological barriers. Such systems have specific analytical needs and time-of-flight secondary ion mass spectrometry (ToF-SIMS) is per se highly relevant, particularly when considering the use of a new type of ion source based on argon clusters (Arn+). The main objective of this work was therefore to understand the ion-matter interactions of such a cluster beam with the organic materials used in organic electronics.

A fundamental study was carried out by comparing sputtering with three different ion beams (Cs+, C60++, Arn+) on organic structured samples (such as PS-b-PMMA block copolymers) and it transpired that although cluster size and energy has little effect on the observable damage to the sample, larger argon clusters induce more roughness during ToF-SIMS depth profiling. This was confirmed by AFM (Atomic Force Microscopy) and XPS (X-ray Photoelectron Spectroscopy) and a geometric model. Next, different devices in organic electronics were characterized by ToF-SIMS. The study of self-assembling PS-b-PMMA block copolymers made possible to evaluate the influence of the annealing duration and of the thickness of the layer. Furthermore, a protocol was developed to analyse stacks of inorganic/organic layers, in particular those contained in OLED devices. It was then possible to characterize the stacks of a complete organic device whilst maintaining molecular signal and a high depth resolution of 2 nm. In parallel we identified the chemical degradation of an organic material in the stack and evaluated the efficiency of barrier layers designed to protect it. More precisely, specific signatures to the hydrolysis reaction of the layer as well as increase in moisture level after encapsulation were identified. This PhD project has contributed to broadening the understanding of the effects of argon cluster ion beams on a wide range of organic materials in organic electronics devices and to demonstrate its potential for their characterization.

Paul GONDCHARTON

Grenoble Alpes University, France

Integration of direct bonding : metal thin films and morphological evolutions

The semiconductor industry is driven by an increasing need of computation speed and functionalities. In the development of next generation devices the integration of more functionalities in an ever smaller volume becomes paramount. So far, classical planar integration was privileged but it is currently reaching its limits. One solution to this technological challenge is to consider the 3D dimension as pathway of integration. To ensure the vertical stacking of circuits, the development and control of assembly processes becomes crucial. Among the different techniques under development, direct bonding of metal thin films is a promising solution. It is a straightforward option that offers both a mechanical and an electrical link between the active strata. Microstructural, physical and chemical properties of deposited metal thin films were widely reported in previous state of art. However, they have not yet been studied in the specific bonding environment. The main goal of our study is to pinpoint the impact of this environment during and after the process of assembly. Direct bonding process consists in putting into contact smooth surfaces at room temperature and ambient air which in appropriate conditions leads to the establishment of attractive forces. Since bonding is not operated under vacuum, adsorbed species are trapped at the interface and the metal bonding suffers from the formation of native oxide. The encapsulation of these species as well as the native metal oxide interfere with the bonding process and the establishment of an electrical contact. In this study, various bonded structures have been realized using an extended set of metals in different thin film configurations. Metal oxide layers impact is clearly highlighted via the monitoring of adhesion properties of the assemblies. In the Cu-Cu direct bonding case, the interfacial water reaction is primordial in the strengthening of bonding toughness at room temperature. At higher temperature, oxide dissolution and vertical grain growth are driving forces in the sealing of bonding interface. The microstructure play a role in all these phenomena since grain boundaries are favorite diffusion pathway in thin films. Considering the temperature limitation imposed by the integration, we also highlight that refractory metal thin films needs another bonding approach compared to the transient metals. The understanding of bonding mechanisms throws new light on the use of direct bonding process in the realization of future electrical components.

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