A VERSATILE SILICON PHOTONICS PLATFORM WITH ADVANCED COMPONENTS

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OUTLINE

1. Silicon photonic: 200mm CMOS core technology towards 300mm
2. Emergent needs vs core process
3. Technological add-on #1: 3D packaging
4. Technological add-on #2: Silicon Nitride circuits
5. Technological add-on #3: Hybrid III-V on silicon laser
WHAT IS SILICON PHOTONIC?

- Silicon photonic aims at integrating in the **silicon microelectronic CMOS technology circuits** and modules initially based on other technologies (InP, InGaAs, LNbO3, SiO2, …)

- Making photonic integrated circuits on Silicon using **CMOS process** technology in a **CMOS fab**.

- Merging photonics and CMOS.

- **Expected benefits:**
  - Higher integration level
  - Low cost, high volume facilities
  - Access to mature packaging and EDA tools
  - WDM and scaling to >1 Tb/s
  - Solving electrical interconnect limits in Data centers, Supercomputers and ICs with higher capacity, lower cost optical interconnects
BUILDING BLOCKS FOR OPTICAL DATA TRANSMISSION

- **Electrical Data Out**
  - Driver
  - Modulator: E to O conversion
  - Multiplexer: Signal combining

- **Electrical Data In**
  - Laser 1
  - Laser 2
  - Laser 3
  - Laser 4

- **De-Multiplexer:** Signal separation
- **Photo-detector:** E to O conversion
- **Optical Data In**
- **Fiber coupler:** PIC to fiber interface
- **Optical Data Out**
  - Fiber Coupler
SILICON PHOTONIC CORE TECHNOLOGY DESCRIPTION

- 310nm SOI
- 193nm DUV lithography
- Multilevel silicon patterning
- Selective Germanium epitaxy
- Silicide

- Metal heater
- Planarized BEOL
- 2 AlCu routing levels
- UBM for Cu pillar assembly
SILICON PHOTONIC CORE TECHNOLOGY DESCRIPTION

- Define all the photonic devices
  - Various waveguide architectures

- Photodetector patterning
  - Germanium selective epitaxy

- Photodetector contact formation

- Si Modulator contact silicidation

- Metal interconnection
  - Metal heater definition for $\lambda$ tuning

CMOS-based process with photonic dedicated optimizations

CMOS standard process
### O-Band Device Library - Example

#### Rib WG
- **Width**: 400 nm
- **Prop. Loss**: 0.2 dB/cm

#### Deep rib WG
- **Width**: 320 nm
- **Prop. Loss**: 0.7 dB/cm

#### Strip WG
- **Width**: 350 nm
- **Prop. Loss**: 1.1 dB/cm

#### 2D GC
- **Ins. Loss**: < 4 dB
- **1dB BW**: 30 nm

#### AWG
- **Ins. Loss**: 2-3 dB
- **Xtalk**: > 20 dB
- **1dB BW**: 1.5 nm

#### Crossing
- **Loss**: < 0.25 dB
- **Xtalk**: > 35 dB

#### MMI
- **Loss**: < 0.5 dB
- **Balance**: ±3%

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### Si Modulators
- **Length**: 2 mm
- **$V_{fL0}$**: ≈ -2 V
- **Loss @ -0 V**: 0.8 dB/mm
- **NRZ Modulation**
  - ER > 4.5 dB
  - SNR > 7

### Ge Photodiodes
- **Width**: 0.8 µm
- **Length**: 15 µm
- **Responsivity**: > 1.05 A/W
- **Dark Current @ -2 V**: 5 nA
- **BW @ -2 V**: > 40 GHz
EMERGENT NEEDS VS CORE PROCESS

- Co-integration with complex « host chips »
  - FPGA or switches with optical IOs
  - Manycore computer architectures

- Silicon Photonics address circuits of increasing complexity
  - Hundreds of optical functions on a chip
  - Ease routing using multilayer photonics
  - Requires dedicated PDK in EDA tools
  - Broadband coupling required for WDM modules
  - Thermal constraints

- Laser source integration
  - Several competing technologies
  - Direct bonding requires CMOS compatibility
ADD-ON #1 : 3D PACKAGING

- High data rate silicon photonics based module must be considered as an RF module with an E/O or O/E convertor: RF packaging solutions are needed
  ⇒ Si photonic platform must integrate Microbumps/Micropillars and/or TSV

MicroBump/Micropillars

- 50 µm pitch
- Copper pillar with eutectic solder
- C2W or C2C assembly
- Low parasitics

Reflective Tx for FTTH (EU FABULOUS project)

- QAM16 transmission on a single fiber
- Dedicated MZM segmented CMOS driver

Sraullu et al., ECOC PDP, 2016
Menezo et al., JLT, 34,10,2016

Low power 25Gbps photoreceiver

- 50µm pitch microbump
- 170 fJ/bit
- -15 dBm sensitivity
- TIA design : Caltech

Saaedi et al., J. Lightwave Tech., 2015

High DataRate Modules

4 x 25Gbps receiver module

- WDM and SDM versions
- < -12dBm sensitivity at 10⁻³ BER
- EIC with 4pJ/bit consumption
- TIA design : ST microelectronics

Bernabé et al., OIC 2016, Paper MB3
Castany et al., ESTC 2016
ADD-ON #1 : 3D PACKAGING

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L. Fourneaud, Internal report

"System-in-package"
ADD-ON #2: SILICON-NITRIDE AS A PHOTONIC LAYER

**Why Silicon nitride:**
- Low refractive index \( n_{\text{SiN}} = 1.88 \)
  - less sensitive to roughness and fabrication imperfections
  - lower propagation losses
- Low thermo-optic coefficient ( \( \sim 2 \times 10^{-5} \text{ K}^{-1} \))
  - Temperature quasi-insensitive devices for data center environment

**Objective: CWDM transceiver in the O-band (1260-1340nm)**
CWDM: Coarse Wavelength Division Multiplexing. 4 channels (= 4\( \lambda \)) with 20nm spacing. No temperature control of the lasers.

**Si-SiN platform:**
Active properties of Si and passive properties of SiN

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Q. Wilmart *et al.*, in Proc. of SPIE Phot. West 2018
SI-SIN FABRICATION & PERFORMANCE

SOI 300nm
BOX 2µm

Oxide deposition 200nm

SiN deposition (600nm PECVD 300°C) + patterning (DUV 248nm)

Final encapsulation

• Low temperature deposition of SiN → Si doping compatibility
• SiN waveguide propagation loss : 0.8 dB/cm
• SiN thermo-optic coeff. : 1.7x10^-5 K^-1 (in Si 2x10^-4 K^-1 )

Q. Wilmart el al., in Proc. of SPIE Phot. West 2018
MULTIPLE PHOTONIC LAYER INTEGRATION

Low thermal sensitive SiN Mux/DeMux

High-efficiency & wide bandwidth Si-SiNx grating coupler

Si-SiN transitions for 3D photonic

0.09 dB/transition

side view (BPM simu)

C. Sciancalepore et al., SSDM 2017

Q. Wilmart et al., in Proc. of SPIE Phot. West 2018
ADD-ON #3: III-V INTEGRATION ON SI-PHOTONIC CHIP

- Growth of the III-V wafers (2”, 3”, 4”)
- Processing of SOI wafers 8” or 12” (modulators, detectors, passive devices, etc.)

III-V bonding on processed SOI & InP substrate removal

- III-V material patterning,
- Metallization of lasers, modulators and detectors

CMOS fab compatible processes needed to avoid wafer downsizing and maximize the functional SOI wafer surface.
HETEROGENEOUS III-V INTEGRATION

Components
• Laser
• Electro-absorption modulator
• Semiconductor optical amplifier

To use the advantage of each material properties:
• Optical gain is provided by the III-V (InP/InGaAsP –QWs or AlGaInAs)
• The high resolution laser cavity as well as the PIC is fabricated in a 200/300mm Silicon platform (CMOS planar technology)

To localize III-V by die-to-wafer bonding
• Highly flexible approach (multiple laser-λ in the O+C+L bands / PD / EAM)
• Equivalent to multiple localized epitaxies
INTEGRATED HYBRID III-V/SI LASER PAST RESULTS

**Hybrid DBR @ 1,55µm**
- CW operation (>60°C)
- $I_m$: 17-60mA (0.8-2.5 kA/cm²) for T: 10 to 60°C
- Rs = 7.5 Ω
- Lasing turn-on voltage : 1.0 V
- $P_{Si-waveguide}$ > 14 mW (20°C)
- $P_{fiber}$ > 4 mW (20°C)
- SMSR > 40 dB

A.Descos et al., ECOC 2013

**Hybrid DFB @ 1,31µm**
- CW operation (>55°C)
- Ith: 30-50mA
- Rs = 15 Ω
- Lasing turn-on voltage : 1.2 V
- $P_{Si-waveguide}$ > 20 mW (20°C)
- $P_{fiber}$ > 3 mW (20°C)
- SMSR > 40 dB


**25Gb/s laser + MZM transmitter**
- 25Gb/s transmission at 1.3µm up to 10km.

T. Ferrotti et al., SSDM, (2016)
III-V INTEGRATION ON SI: TOWARD LSI CMOS COMPATIBLE PROCESS

1. Process & Materials
   - Patterning
   - Contact on III-V
   - Multi level BEOL
   - III-V Die Bonding

2. Laser Topography
   - III-V stack thickness=4µm
     vs.
   - PMD thickness=1µm

3. SOI Substrate
   - SOI for laser: 500nm
     vs.
   - SOI platform: 310nm

4. Laser integration impact
   on other devices
**LARGE SCALE INTEGRATION CMOS FRIENDLY PROCESS**

- Ohmic contacts on III-V materials
- Collective III-V die bonding
- Localized silicon thickening
- III-V patterning
- Multilevel planar BEOL

B. Szelag et al., IEDM 2017
LARGE SCALE INTEGRATION CMOS FRIENDLY PROCESS

Ohmic contacts on III-V materials

Multilevel planar BEOL

III-V patterning

Silicon localized thickening
FIRST DEMO ON 200MM SOI WAFER OPTICAL CHARACTERIZATION

- Only 1 metal layer for this design
- Ni-based N & P contacts

- Ith: 55-65mA
- Rs = 10 Ω
- Max P-Si-waveguide > 3 mW
- Max P-fiber ≈ 1 mW
- SMSR > 40 dB (best 50dB)

@room temperature
COLLECTIVE DIE BONDING WITH SILICON HOLDERS

- Efficient cleaning
- Very high transfer rate >95%
- Bonding Yield~100%
- CAD2MASK Holder mask generation during PIC design
- Additional cost for holder fabrication
COLLECTIVE DIE BONDING WITH SI HOLDER - EXAMPLE

After die Bonding  |  After InP grinding  |  Acoustic characterization

- Transferred die:
  - 99 %
  - 99%
  - 99%
  - 70%

- Transferred die without defects:
  - 75 %
  - 73%
  - 73%
  - 52%

- Transferred die & bonded on more than 99% of their surface:
  - 87 %
  - 84%
  - 88%
  - 62%

- Transferred die & bonded on more than 95% of their surface:
  - 91 %
  - 85%
  - 90%
  - 64%
BACKSIDE INTEGRATION (BSI) CONCEPT

Problems:
1. III-V based device integration with not change on the baseline photonic platform (BEOL)
2. III-V based device integration compatible with a co-integration of SiN devices

Solution:
⇒ III-V post processing on the backside of the full silicon photonic platform
HYBRID LASER BSI DEMONSTRATION

- Integration scheme compatible with any photonic platform
- No impact on the Silicon photonic platform
- Modular integration
- Si photonic platform and laser integration can be done in 2 different fabs
- Only way to have ‘3D photonic’ (SiN or Si level on top of SOI) and laser on the same die
- EIC and Laser @ opposite sides of the PIC
- Demo: Passive + BSI DBR laser done with 100mm process (J. Durel et Al, IEDM 2016)
CONCLUSION

- Silicon Photonics CORE process
  - 3D Photonics (SiN/Si, Si/Si)
  - III-V on Silicon (FSI or BSI)
  - 3D packaging
- 200mm III-V CMOS compatible process
- Large scale die to wafer bonding
Thank you