3D TECHNOLOGIES: SEVERAL DISRUPTIVE TECHNOLOGIES TO LOOK AHEAD

Leti Devices Workshop | Olivier Faynot | December 4, 2016
SOMMAIRE

1 Top Challenges for Computing
2 How 3D Can Help?
3 Our Options Towards Fine Pitch
4 Summary
Traditional exponentially growing “laws” are running into physical and cost limits.

**TOP CHALLENGES FOR COMPUTING**

1. **Cost**: Disruptive Architecture and Integration Technologies are Required
2. **Performance**: Disruptive Technologies are Required

### Scaling within Cost Limits

- **2015**: 0.1 EFLOP/s, 200pJ/FLOP
- **2020**: 1 EFLOP/s, 2pJ/FLOP
- **> 2020**: 10 EFLOP/s, 200pJ/FLOP

### Scaling within Power Limits

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- **2020**: 1 EFLOP/s, 2pJ/FLOP
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LETI’S ROADMAP FOR COMPUTING

> 2020

Computer Architecture Paradigm Shift
- Quantum Computing
- Neuromorphic Architectures

2020

Technological Shift
- New Memory Materials and Architecture
- 3D VLSI and High-Density 3D
- Integrated Silicon Photonic Dies
- Neuromorphic for Advanced Chiplet Architecture

Integration Shift
- 3D Integrated Circuits
- Interposer Integrated Chiplets
- Integrated Photonic Links

2015
3D TECHNOLOGIES EVOLUTION

CHIPLET DEVELOPMENT AXIS

INTERPOSER DEVELOPMENT AXIS

2015
LOGIC-ON-LOGIC
3D Interconnect

2016
MICRO-SERVER
3D Partitioning

2017
SERVER
Active Interposer

2018-19
HPC
Photonic Interposer

2022
2022 VISION
HIGH DENSITY 3D: A REAL ALTERNATIVE TO SCALING

Self Assembly
Pitch : 1-5 µm

10^8 3DC/mm²
⇒ Transistor level

M3D (CoolCube™) [3]
Pitch : 0.05-0.1 µm

TSV + µBump [1]
Pitch : 20 µm

~10^5 3DC/mm²
⇒ Logic Bloks
⇒ Logic Gates

HD-TSV [2]
Pitch : 1-3 µm

~10^5 3DC/mm²

Cu/Cu [2]
Pitch : 2-5 µm

~10^3 3DC/mm²
⇒ Entire core

HIGH DENSITY 3D: A REAL ALTERNATIVE TO
SCALING

HOW 3D CAN HELP?

Network-on-Chip 3D Asynchronous

- Multi core applications, high bandwidth
- Serial links
- Logic on Logic stack
- Faults tolerance, repair

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Georgia Tech ISSCC'2012</th>
<th>Kobe Univ. ISSCC'2013</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process &amp; 3D technology</td>
<td>130nm F2F CuCu</td>
<td>90nm F2B TSV</td>
<td>65nm F2B TSV</td>
</tr>
<tr>
<td>3D Bandwidth</td>
<td>277 Mbps</td>
<td>200 Mbps</td>
<td>326 Mbps</td>
</tr>
<tr>
<td>3D I/O Power</td>
<td>-</td>
<td>0.56 pJ/bit</td>
<td>0.32 pJ/bit</td>
</tr>
</tbody>
</table>

- BEOL top die
- μ-bump
- TSV AR 1:8
- BEOL bottom die
- C4 bump
- Package ball

3D Link Performances

- Fastest Link, +20% (326 Mflit/s)
- Best Energy Efficiency, +40% (0.32 pJ/bit)
- Self-Adaptation to Temperature, a Strong 3D Concern

[P. Vivet et al. ISSCC’16]
HIGH DENSITY 3D : A REAL ALTERNATIVE TO SCALING

Self Assembly
Pitch : 1-5 µm

Cu/Cu [2]
Pitch : 2-5 µm

~10^5 3DC/mm²
⇒ Logic Blocs
⇒ Logic Gates

Pitch : 1-5 µm

WAFER TO WAFER OR CHIP TO WAFER?

**Wafer-to-wafer**
- Objectives:
  - Ultra Fine Pitch
  - Throughput

**Chip-to-wafer**
- Objectives:
  - Heterogeneity
  - Multi Dies Stacking
  - Low Yield Devices Stacking
CU/CU BONDING: PRINCIPLE

Maximize chip-to-chip connection density

- No adhesive (underfill), No pressure, Room $T^\circ$ process: high throughput
- From 200°C to 400°C annealing
- Pitch: $5-10\mu$m (2015) => 1-2µm (2017)

L. Benaissa et al, EPTC 2015
Lacourbe S.et al,, ECT2016

Demonstration done on Wafer to Wafer
WAFER TO WAFER OR CHIP TO WAFER?

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CHIP-TO-WAFER INTEGRATION PROCESS

FC300 bonding machine with ± 0.5μm post-bonding accuracy

BEST ALIGNMENT : 200nm

Y. Beillard, 3DIC 2013
SELF-ASSEMBLY FOR CHIP TO WAFER APPROACH

PRINCIPLE OF SELF-ASSEMBLY USING CAPILLARY FORCE

Phase 1: Self-Alignment
- Leti’s choice: capillary driven alignment
- Minimization of surface tension with capillary force

Phase 2: Hybridation
- Leti’s choice: Direct bonding

1 – LIQUID DEPOSITION ON SUBSTRATE OR DIE
2 – ROUGH PRE-POSITIONNING USING MECHANICAL TOOL
3 – REMOVAL OF THE TOP DIE
4 – SPONTANEOUS ALIGNMENT THANKS TO CAPILLARY FORCE
5 – LIQUID EVAPORATION AND HYBRIDATION

High Throughput
High Alignment Accuracy (< 1 µm)
Collective Bonding
Direct Bonding Compatibility

S. Mermoz, EPTC 2013
OUR ROADMAP FOR THE FUTURE

… Based on closed partnership with equipment suppliers

WtW alignment (@ 3σ)

+/-40nm

+/-100nm

+/-200nm

+/-1000nm

2015

2016

2017

2018

CtW alignment (@ 3σ)

+/-500nm

+/-1000nm

+/-2000nm

Highly depend on throughput
HIGH DENSITY 3D: A REAL ALTERNATIVE TO SCALING

M3D (CoolCube™) [3]
Pitch: 0.05-0.1 µm

$10^8$ 3DC/mm$^2$ => Transistor level


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COOLCUBE™ TECHNOLOGY

This work: 65nm
D > 2x10^7 /mm²

14nm
D > 10^8 /mm²

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SUMMARY

• Yes, 3D Can Help the Computing Roadmap!
• Early Demonstrations Done!
• LETI is Working Towards Several Disruptive Options Devoted to Fine Alignment and Fine Pitches
  • Cu/Cu Hybrid Bonding to Achieve 1µm Pitch on Wafer to Wafer Approaches
  • Self-Assembly for Die to Wafer and high Throughput
  • Coolcube™ Technology for Transistor Level Connections

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Thank you for your attention