3D INTEGRATION, A SMART WAY TO ENHANCE PERFORMANCE
OVERAL GOAL OF THIS TALK

3D VLSI technologies
(3D VIA Pitch <5μm)

How these technologies can boost

Hybrid bonding

3D sequential

Image sensor

HPC
OVERVIEW

1. 3D VLSI technologies: from hybrid bonding to 3D sequential integration
2. 3D imagers
3. High Performance computing
Hybrid bonding flow:

Various options: Wafer to Wafer, Die to Wafer, Die to Die
3D VLSI: 3D SEQUENTIAL INTEGRATION

Bottom MOSFET process with or without interconnects
Top active creation: Future MOSFET channel
Top MOSFET process
3D contact BEOL

Also named 3D monolithic

THERMAL BUDGET CONSTRAINTS

... CoolCube™
3D VLSI: HYBRID BONDING VERSUS 3D SEQUENTIAL

**Hybrid bonding**
Alignment made during bonding
3σ min = 250nm

**3D sequential**
Alignment by lithography
3σ = 5nm (28nm stepper)
3D VLSI: HYBRID BONDING & 3D SEQUENTIAL OPTIONS: VIA DENSITY

3D via density

3D partitioning options

1-Entire core
2-Logic bloc
3-Logic gates
4-Transistors

[1]: L. Brunet et al., VLSI 2016,
[2]: I. Sugaya et al., ASMC 2015,
[3]: J. De Vos, 3DIC 2016
[4]: L. Peng et al., EPTC 2016
[5]: D. Zhang et al. TSM 2015
OVERVIEW

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3D IMAGERS: CURRENT PARTITIONING TRENDS

Current Imager system

Form & Fill factor gain wrt 2D
Energy efficiency and performance[1]

Sony [2]
“Motion Eye™”

Parallel access to pixel array
1 ADC / 10x16 pixels

Conversion and processing at column level
1 ADC + 1 PE / column

HYBRID CU BONDING (WTW)

Alignment

Co-development equipment/process

Advanced bonding tool generation (Gemini)

→ Alignment performance: $3\sigma = 195\text{nm}$

1\text{µm} pitch Hybrid Bonding

[1] A. Jouve, S3S 2017
3D IMAGERS: NEW PARTITIONNING OPPORTUNITIES

Partitioning at the pixel level

Increased Photodiode area
(44% for 1.4µm node [1])

Smart 3D pixel
In pixel processing (Adaptation, calibration, pre-processing…)

Pixel array
3D IMAGERS: NEW PARTITIONNING OPPORTUNITIES

Hybrid bonding can be used to connect the 3D pixel to the DSP and RAM.
3D IMAGERS: NEW PARTITIONNING OPPORTUNITIES

<1μm 3D contact pitch  ➔  3D sequential integration

300 mm industrial clean room demonstration
Max TB budget is relaxed for a photodiode (700°C) \[1\] vs MOSFET (500°C)

Critical process modules are now below 500°C

Cold 28nm FDSOI devices in line with high-temp. POR
OVERVIEW

1  3D VLSI technologies: from hybrid bonding to 3D sequential integration

2  3D imagers

3  High Performance Computing
Complex SOC for HPC application

Leti’s roadmap: Chiplets on active interposer

Huge die size (4cm$^2$) (yield issues)
Complexity wall (co-integration of technologies)
Memory wall

**Cost reduction:**
Smaller chips (improved Yield)
Known good die (pre bond test)
Each technology at the right silicon cost

**Performance:**
Best technology for each chip
Compatible with HBM

[1]: P. Vivet et al., ISSCC 2016 (leti)
Die-to-Wafer bonding flow

1. CMP
2. Top die dicing
3. Holder placement
4. Cleaning
5. Die-to-Wafer stacking

FC1 Results
- Precision: ± 1 µm
- Throughput: 500 dph

3 µm pitch DTW hybrid bonding demonstrated

THE ULTIME IMBRICATION OF MEMORY AND COMPUTING

→ 3D sequential is an opportunity to break the memory wall

Computing immersed in memory

X 1000 gain in consumption expected with computing near memory

Neuromorphic computing

- High contact density mimics the high interconnectivity of neurons
- RRAM mimics the synapses

N³XT Computing system [1,2]

CONCLUSION: LETI 3D OFFER

- Every application requiring a high number of interconnections or reconfigurability of the interconnections deserves to be explored in 3D.

- Leti is your partner to evaluate the gains for your applications using 3DVLSI.

- Demonstration of prototypes & Architecture partitionning.
Thank you for your attention