Hybrid III-V/Si DFB laser integration on a 200 mm fully CMOS-compatible silicon photonics platform

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Outline of Presentation

- Introduction & Objectives
- Hybrid III-V/Si DFB laser – Process description & Fabrication
- Hybrid III-V/Si DFB laser – Optical characterization
- Result discussion
- Conclusion & Perspectives
What is silicon photonic?

- Silicon photonic aims at integrating in the silicon microelectronic CMOS technology circuits and modules initially based on other technologies (InP, InGaAs, LNbO3, SiO2, ...)

- Making photonic integrated circuits on Silicon using CMOS process technology in a CMOS fab.

- Merging photonics and CMOS.

- Expected benefits:
  - Higher integration level
  - Low cost, high volume facilities
  - Access to mature packaging and EDA tools
  - WDM and scaling to >1 Tb/s
  - Solving electrical interconnect limits in Data centers, Supercomputers and ICs with higher capacity, lower cost optical interconnects
Silicon Photonic Building Blocks

Silicon Photonic Links

Transmitter

Receiver

Photo-detector: E to O conversion

De-Multiplexer: Signal separation

Fiber coupler: PIC to fiber interface

Modulator: E to O conversion

Multiplexer: Signal combining

Electrical Data Out

Optical Data In

Optical Data Out

Ge photodiode

Si waveguide
Hybrid III-V/Si laser – Current process

- CMOS compatible process for silicon part
- III-V substrate bonding on silicon
- Si wafer downsizing to 100mm

Laser process steps using III-V fabrication line:
- Noble metals
- Lift-off
- RIE etch

⇒ Not CMOS compatible process
⇒ Not planarized BEOL
⇒ Cost advantage of silicon photonics based the use of CMOS platforms and large wafer format is no more valid
Hybrid III-V/Si laser – Targeted process

Final objectives:
- CMOS compatible process for silicon part
- III-V die bonding on silicon
- 200 or 300mm Si wafers
- Compatible with mature silicon photonic platform
- Laser process steps cmos compatible process:
  - No noble metals
  - Conventional patterning steps
- Planarized multi-metal level BEOL

In this work:
- Modular integration of hybrid laser on 200mm mature Si platform
- III-V substrate bonding
- III-V patterning on 200mm CMOS fab
- CMOS compatible contacts on III-V
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Hybrid III-V/Si DFB laser structure & integration scheme

- Silicon waveguide patterning
- Localized silicon thickening
- Bragg grating patterning
- III-V wafer/die bonding
- III-V patterning
- III-V contact metallization
- Tungsten Plug
- Planar BEOL

Transversal views of the laser

Longitudinal view of the laser
Preliminary studies: CMOS compatible contacts on III-V

- Best choice: Ni2P wo annealing for n-InP and Ni with 350°C annealing for P-InGaAs
- Integration constraint & process cost => use the same contact for n-InP and P-InGaAs
Hybrid III/V on Si DFB laser fabrication description

- Silicon photonic platform – Encapsulated passive device
Hybrid III/V on Si DFB laser fabrication description

- Cavity patterning
Hybrid III/V on Si DFB laser fabrication description

- Amorphous silicon deposition
Hybrid III/V on Si DFB laser fabrication description

- Silicon Chemical Mechanical Polishing (EPD on SiO2)

  Localized silicon thickening – no changes in the photonic core process
Hybrid III/V on Si DFB laser fabrication description

- Bragg reflector patterning – silicon partial etch
Hybrid III/V on Si DFB laser fabrication description

- Oxide encapsulation and planarization
- Surface preparation for bonding
Hybrid III/V on Si DFB laser fabrication description

- III-V wafer bonding
- Substrate removal
- Laser GAIN: PECVD SiN Hard mask deposition
Hybrid III/V on Si DFB laser fabrication description

- Laser GAIN: Hard mask patterning
Hybrid III/V on Si DFB laser fabrication description

- Laser GAIN: InGaAs/InP dry etch with EPD on MQW
Hybrid III/V on Si DFB laser fabrication description

- Laser GAIN: PECVD SiN deposition
Hybrid III/V on Si DFB laser fabrication description

- Laser GAIN: SiN spacer patterning
Laser GAIN: Remaining MQW wet etch (diluted H2SO4/H2O2), highly selective vs. InP
Hybrid III/V on Si DFB laser fabrication description

- Laser MESA: PECVD SiN Hard mask deposition
Hybrid III/V on Si DFB laser fabrication description

- Laser MESA: Hard mask patterning
Laser MESA: InP dry etch
Hybrid III/V on Si DFB laser fabrication description

- Oxide encapsulation & planarization
Hybrid III/V on Si DFB laser fabrication description

- Contact window patterning
Hybrid III/V on Si DFB laser fabrication description

- Ni or Ni2P deposition & annealing
Hybrid III/V on Si DFB laser fabrication description

- AlCu Deposition
AlCu patterning
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Optical Characterization
Optical Characterization: LIV characteristics
Optical Characterization: Spectrum

![Optical Spectrum Graph](image)

- **Optical Power [dBm]**
  - Range: -80 to 0 dBm

- **Wavelength [nm]**
  - Range: 1288 to 1308 nm

- **Inset Graph**
  - Shows variation in Optical Power [dBm] with Wavelength [nm] with a peak at around 1298 nm.
Result discussion: Impact of a-Si on laser operation

- Standard model (Si mono only)
- Same model Si-Amo / Si mono
  - Si Amo 200nm
    77% coupling => Cavity instability
  - Si Amo 220nm
    Adiabatic coupling failure
    Mode less confined on the QW => less power
  - Si Amo 180nm
    Adiabatic coupling almost achieved
    Good mode confinement

- With the same design, the thickness of amorphous silicon must be reduced to take into account the index difference of Si-amo (3.523 @ 1310nm) and Si-mono (3.506 @ 1310nm)
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Conclusion & Perspectives

- The monolithic integration of a fully **CMOS compatible** hybrid DFB laser on a 200mm silicon photonics platform has been demonstrated.

- Amorphous silicon is used to **locally thickened the silicon with a damascene process** to build the laser with no impact on the photonic core process.

- The conventional Au-based contacts used in III-V laser are replaced by **Ni-based alloyed contact** with no penalties on the series resistance.

- Single wavelength behavior demonstrated with **SMSR reaching 50dB**.

- Lasing threshold around 60 mA with an output power in the waveguide > 3mW at 160mA
Conclusion & Perspectives

- New iteration with design optimized for Si stack including part of amorphous silicon.
- W-plugs and multi-level planar BEOL
- Integration on the full platform (with active devices)
- Process with III-V die bonding instead of wafer bonding