"L’avenir est comme le reste il n’est plus ce qu’il était’

Paul Valery, “Notre Destin et Les Lettres”, 1937)"

Yan Borodovsky

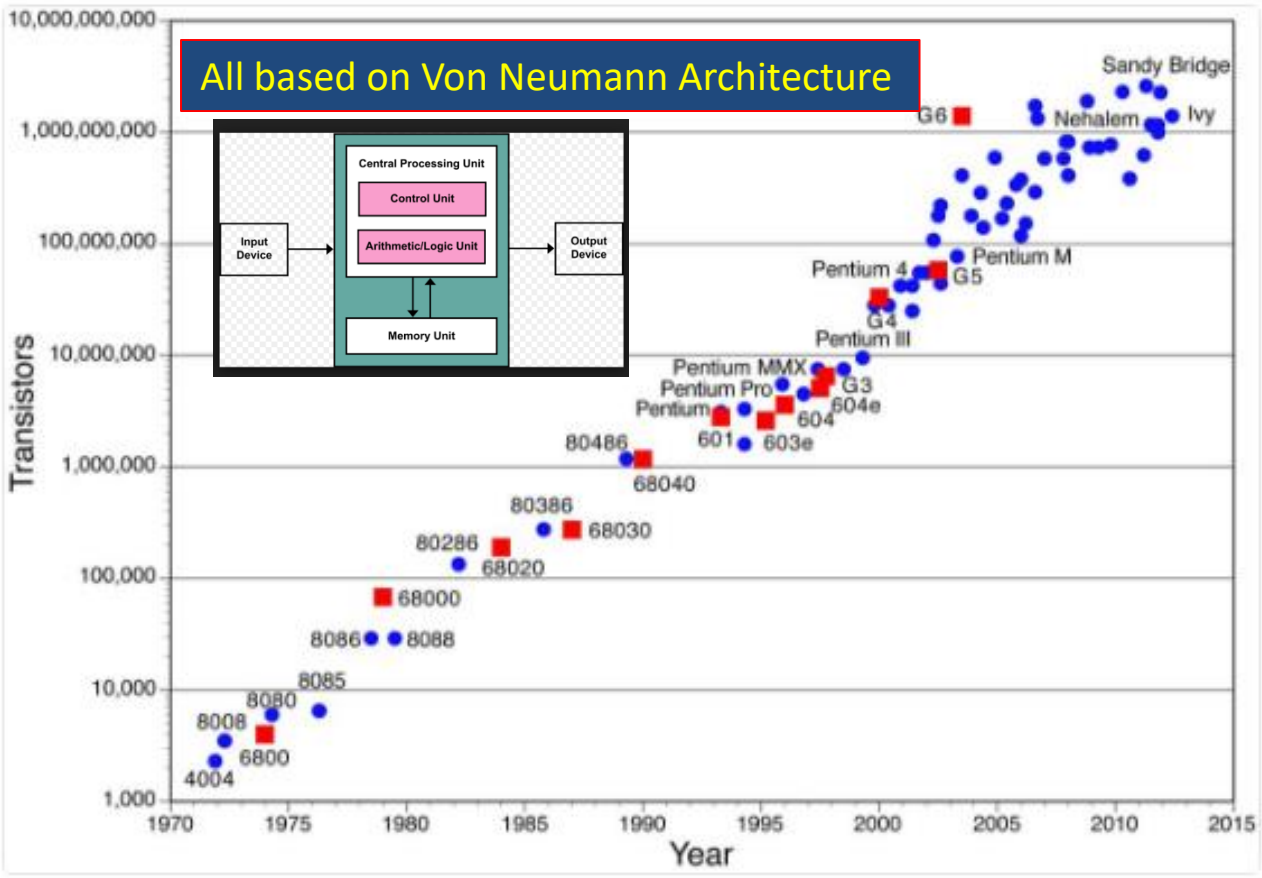
SPIE Fellow

Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

The Future isn't what is used to be

Yan Borodovsky
SPIE Fellow

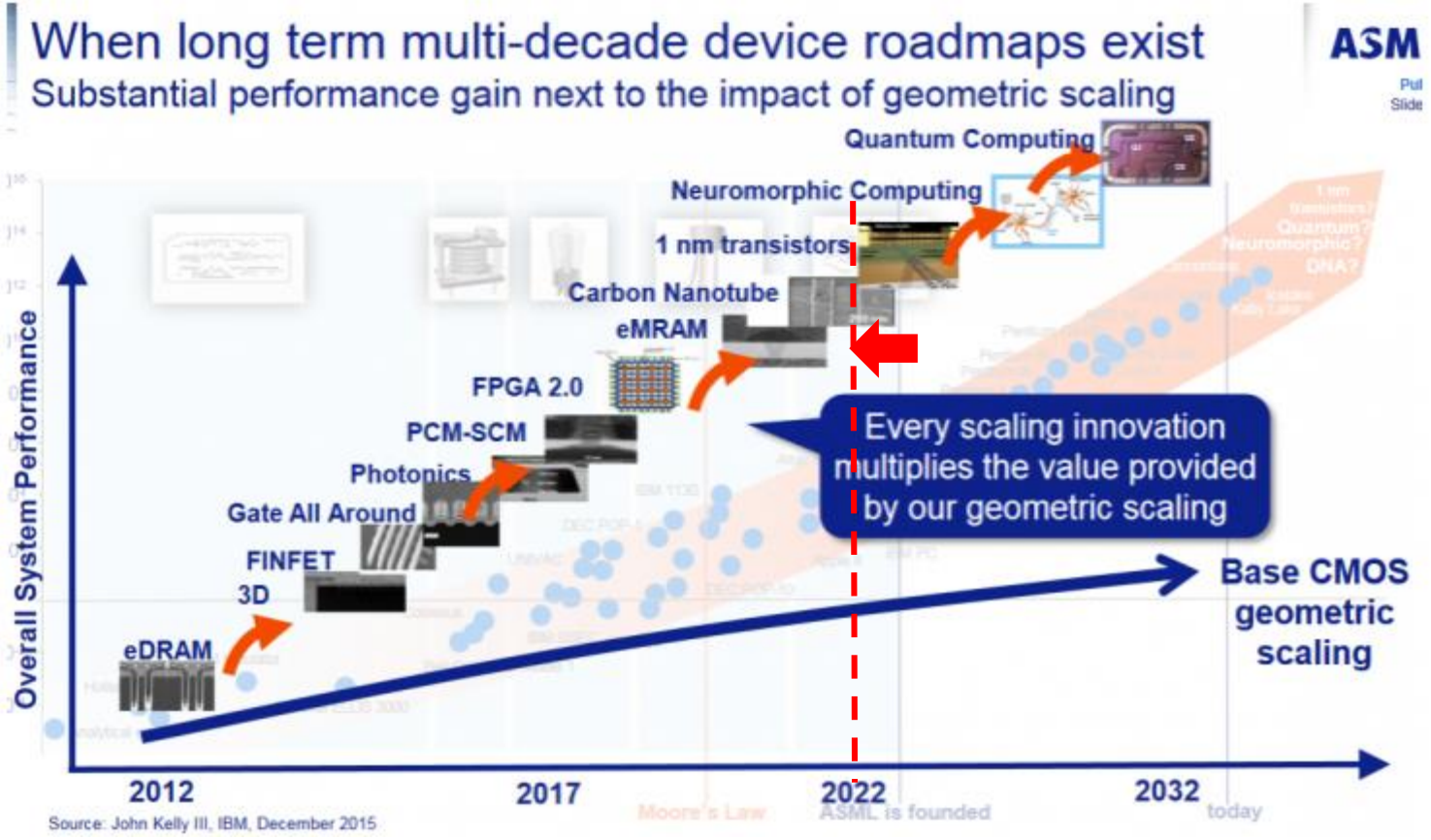
Moore's Law that used to be…



Moore's law Graph Source: **"What lies beneath? 50 years of enabling Moore's Law", Mike Czerniak, Solid State Technology , Nov. 17, 2015**

Moore's Law to be

Von Neumann AND Non-Von Neumann



2022-2024 Computing Platforms

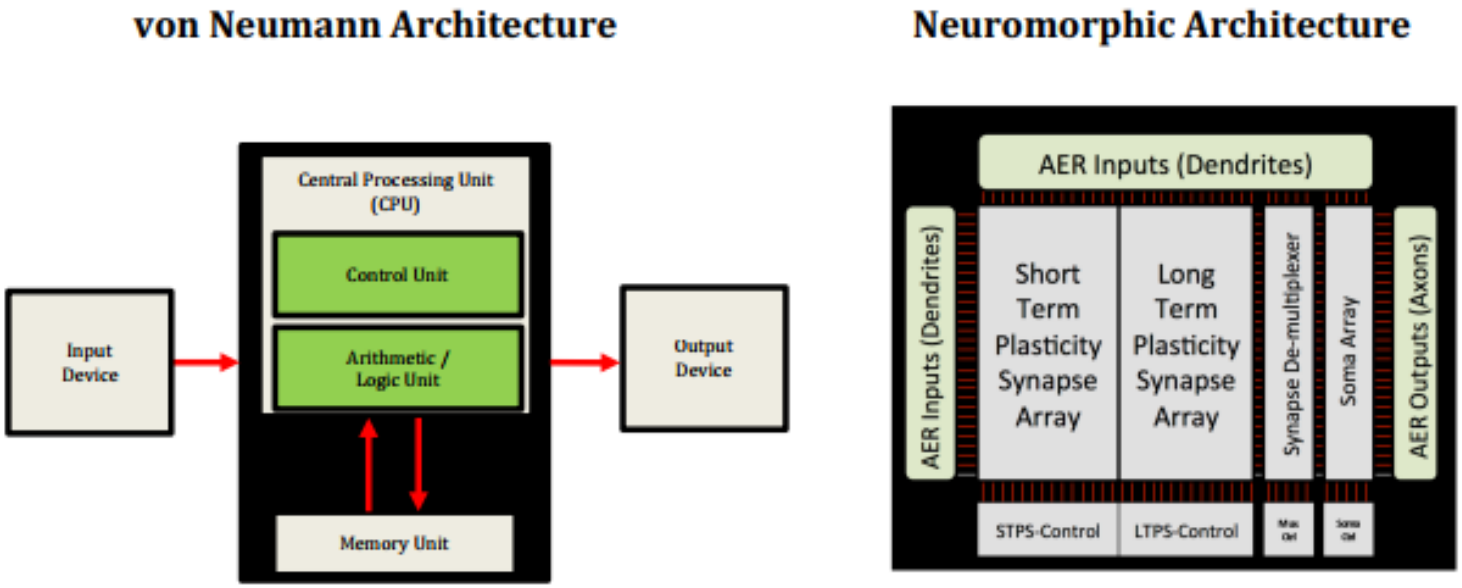


Figure 1. Comparison of high-level conventional and neuromorphic computer architectures. The so-called "von Neumann bottleneck" is the data path between the CPU and the memory unit. In contrast, a neural network based architecture combines synapses and neurons into a fine grain distributed structure that scales both memory (synapse) and compute (soma) elements as the systems increase in scale and capability, thus avoiding the bottleneck between computing and memory.

Source: "Neuromorphic Computing: From Materials to Systems Architecture"

Report of a Roundtable Convened to Consider Neuromorphic Computing Basic Research Needs, October 29-30, Gaithersburg, MD, USA, US DOE, Office of Scince

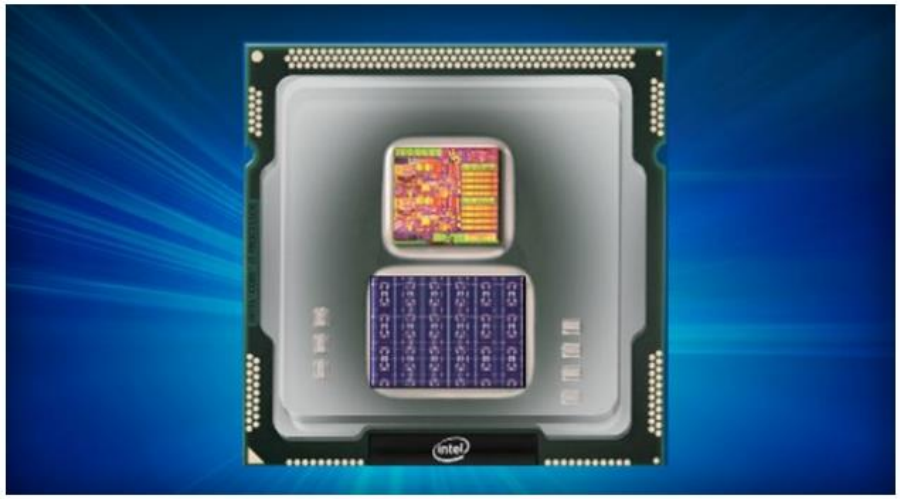
https://science.energy.gov/~/media/bes/pdf/reports/2016/NCFMtSA_rpt.pdf

Von Neumann AND Non-Von Neumann already here

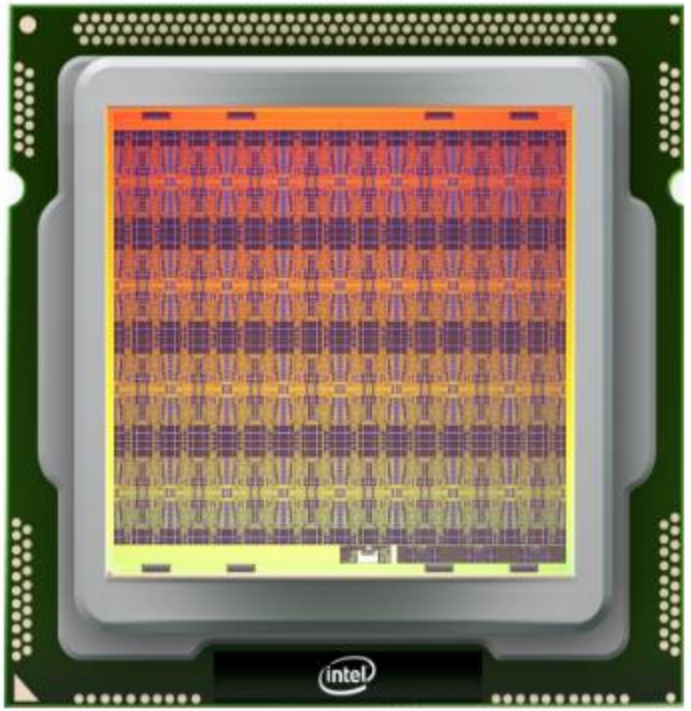
Intel Unveils Neuromorphic, Self-Learning Chip Codenamed Loihi

By Joel Hruska on September 27, 2017 at 9:18 am | 14 Comments

1.1K shares



Loihi simulates a total of 130,000 neurons and 130 million synapses, all capable of communicating with each other… comparable to some small insects. For example, a common fruit fly, an insect studied for AI research, has about 250,000 neurons and 10 million synapses. …human brain - 100 billion neurons,



https://www.extremetech.com/computing/256467-intel-unveils-new-neuromorphic-self-learning-chip-codenamed-loihi

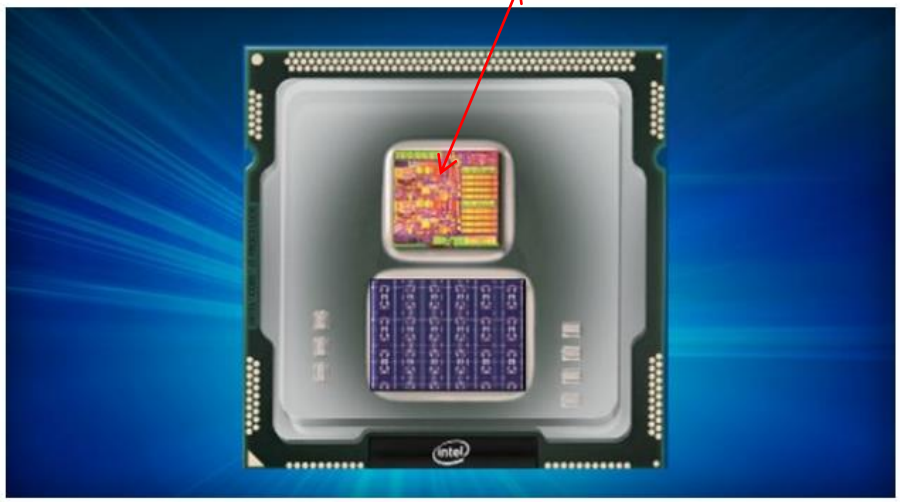
Von Neumann AND Non-Von Neumann already here

Intel Unveils Neuromorphic, Self-Learning Chip Codenamed Loihi

By Joel Hruska on September 27, 2017 at 9:18 am | 14 Comments

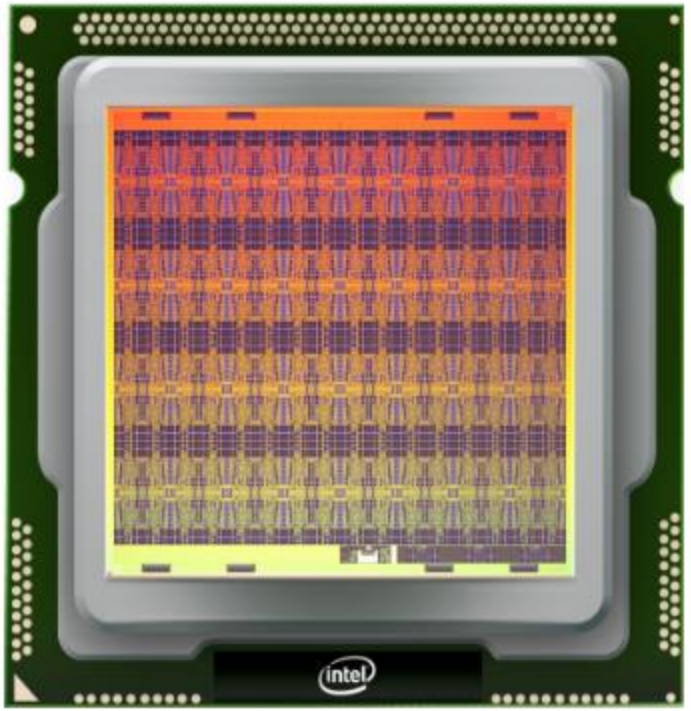
This is Control Programming Unit

>50% area is defect intolerant



Loihi simulates a total of 130,000 neurons and 130 million synapses, all capable of communicating with each other… comparable to some small insects. For example, a common fruit fly, an insect studied for AI research, has about 250,000 neurons and 10 million synapses. …human brain - 100 billion neurons,

This is Neuromorphic Part and it is (or will be) defect tolerant



https://www.extremetech.com/computing/256467-intel-unveils-new-neuromorphic-self-learning-chip-codenamed-loihi

Big 2017 Story – EUV Ecosystem status gives enough confidence to customers to place multiple tools orders

EUV shipments ramp in support of customers' production plans

ASML

Public
Slide 16
January 17, 2018

Customers
show commitment to insert EUV in volume manufacturing by ordering systems

- 4 EUV systems shipped in Q4, 5 recognized in revenue
- Of the 12 EUV shipments planned in 2017, we shipped 10 during the year, 1 shipment is in progress, 1 shipment planned in January 2018
- 10 orders received, EUV backlog increased to 28
- Planned shipments of 22 systems in 2018, back-end loaded, and plan at least 30 systems in 2019

ASML
commits to securing system performance, shipments and support required for volume manufacturing

For volume manufacturing of logic and memory, ASML remains committed to deliver:

- Throughput of >125 wafers per hour
- Availability of >90% on average
- Shipments on time in sufficient volume
- Ability to support a growing installed base

Source: https://staticwww.asml.com/doclib/investor/financial_results/2018/asml_20180107_presentation.pdf

Foundries – 7nm (+, ++) EUV

EUV layer adoption - logic 7nm example

Addressing majority of critical layers at initial insertion

ASML

Public
Slide 17
July 19, 2017

Layer	
Active	
Gate	
LI	
Contact	
Metal 0	
Via 0	
Metal 1	
Via 1	
Metal 2	
Via 2	
Metal 3	
Via 3	
Metal 4	
Via 4	
Metal 5	

Initial EUV layers
Other candidate EUV layers

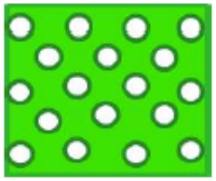
Metal layers patterning types

2D pattern
(1 EUV exposure)

or

1D pattern
(1 ArFi spacer exposure
+ 1 EUV cut exposure)

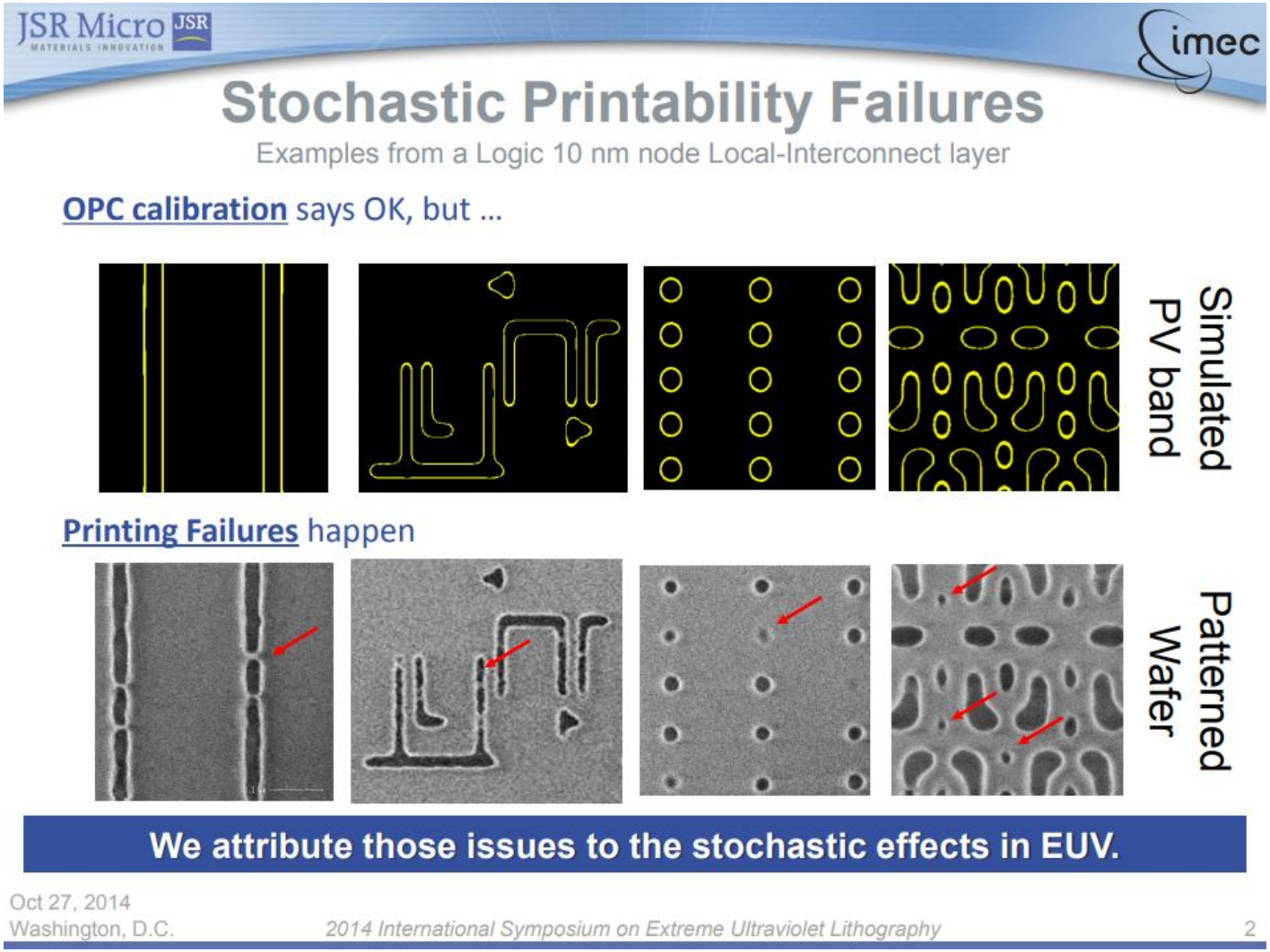
Via / Contact example



(1 EUV exposure)

Source: ASML 2017 Second-Quarter Results Webcast Presentation

Stochastic Patterning Failures must be eliminated for EUV HVM

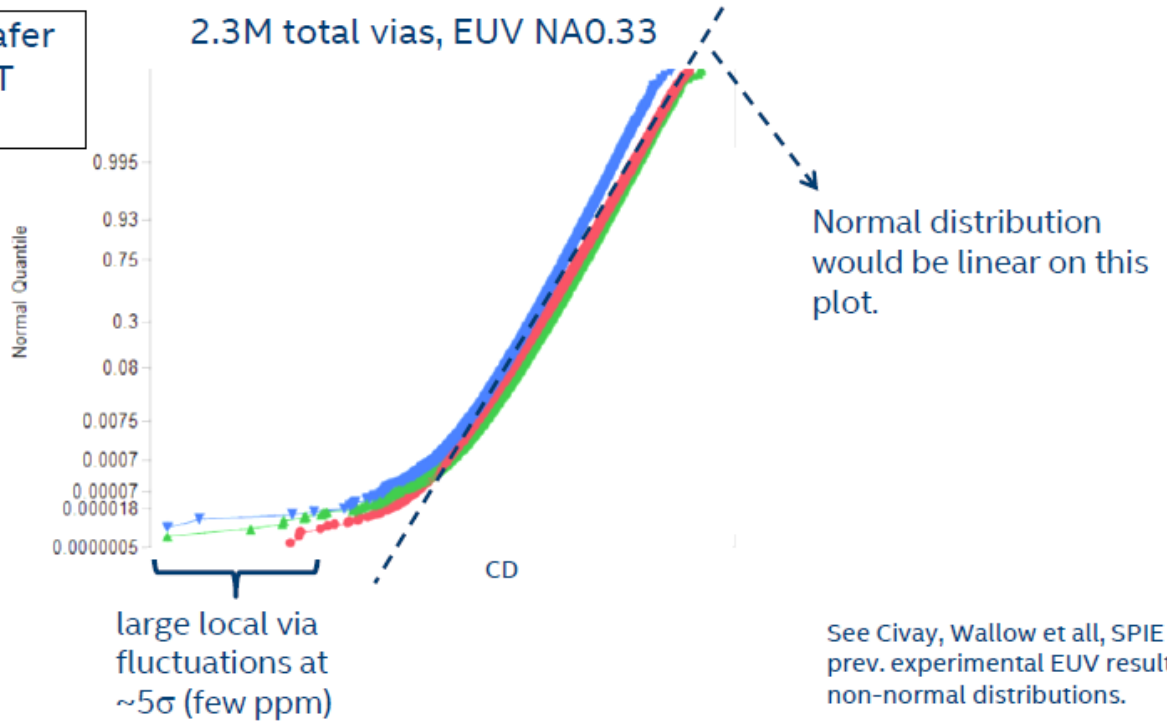


Yan Borodovsky, "The Future isn't what is used to be", Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

With 10B Via/Cuts per chip 5σ process will kill every chip – zero yield

2.3M measured vias: Non-normal CD distribution.

Actual in-fab on-wafer measured vias, NOT simulated results.



See Civay, Wallow et all, SPIE 2014 for prev. experimental EUV results showing non-normal distributions.

Yan Borodovsky, "The Future isn't what is used to be", Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

Via Patterning with EUV

Stochastic requirements for vias

Required failure rate for 99% die yield

26X32mm die

NA = 0.33 Illum. quad with σ=0.2

0.33 NA Limit

0.55NA Limit

YB 2/26/2018

HP_{min} (nm)	*Via count*	*Fail.rate*	
26	0.18×10^{11}	55×10^{-14}	~7 σ
18	0.39×10^{11}	26×10^{-14}	
11	1.03×10^{11}	10×10^{-14}	
8	1.95×10^{11}	5×10^{-14}	~8 σ

Berkeley Lab | MSD Materials Sciences Division

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Measuring and Modeling Stochastic Limitations in EUV Resists

P. Naulleau,
W. Chao, O. Kostko, F. Ogletree, Berkeley Lab
S. Bhattaria, A. Neureuther, UC Berkeley

BERKELEY LAB
CXRO

Photopolymer Japan, Chiba, Japan, June 26 - 29, 2017

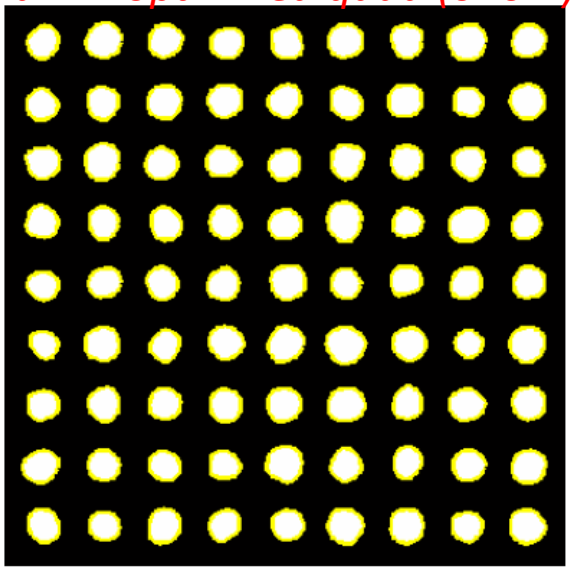
Photon Shot Noise AND Resist Inhomogeneity produce Stochastic Noise in Litho Channel

Modeling Via stochastics: resist conditions

16-nm HP contacts ; NA = 0.33
Illum. - optimized quad (σ=0.1)

Baseline Chemically Amplified Resist used in subsequent slides:

- Esize = 79 mJ/cm^2
- E0 = 15.7 mJ/cm^2
- QE = 3
- PAG = 0.2/nm^3
- Quencher = 0.085/nm^3
- Protecting groups = 2/nm^3
- Absorptivity = 4.2/um
- Thickness = 35 nm
- Acid diffusion range = 12 nm



Developed resist

Measuring and Modeling Stochastic Limitations in EUV Resists

P. Naulleau,
W. Chao, O. Kostko, F. Ogletree, Berkeley Lab
S. Bhattaria, A. Neureuther, UC Berkeley

Photopolymer Japan, Chiba, Japan, June 26 - 29, 2017

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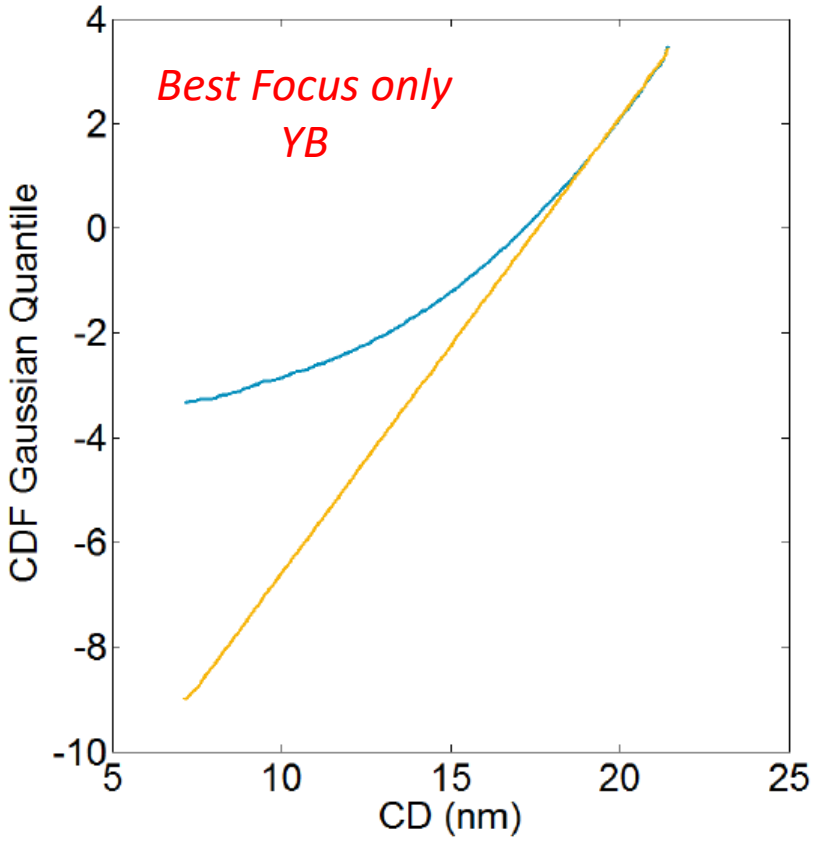
Stochastic Noise in the Channel is Significant - parts per several millions

CDF shows large variations at 4σ frequency

CDF of stochastic resist model

Gaussian CDF



Yan Borodovsky, "The Future isn't what is used to be", Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

Via Patterning with EUV

Stochastic requirements for vias

Required failure rate for 99% die yield

Year	Node	EUV
2019	~7nm	1X
2020	5nm	2X
2022	3nm	3X
2026	1.5nm	?

26X32mm die

HP_{min} (nm)	Via count	Fail. rate	
26	0.18×10^{11}	55×10^{-14}	~7 σ
18	0.39×10^{11}	26×10^{-14}	
11	1.03×10^{11}	10×10^{-14}	
8	1.95×10^{11}	5×10^{-14}	~8 σ

YB

Berkeley Lab | MSD Materials Sciences Division

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Measuring and Modeling Stochastic Limitations in EUV Resists

P. Naulleau,
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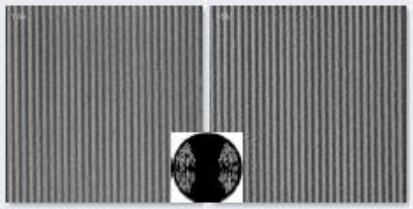
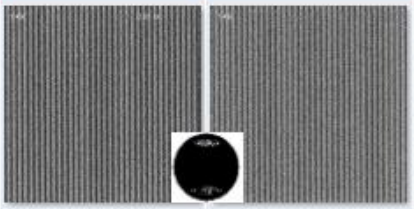
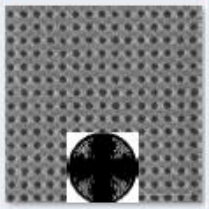
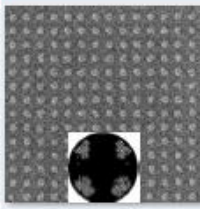
BERKELEY LAB
CXRO

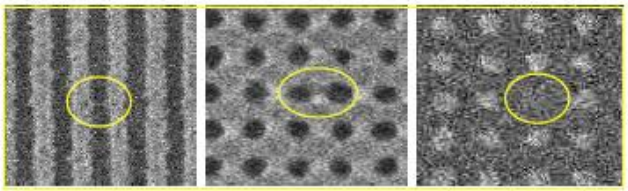
Photopolymer Japan, Chiba, Japan, June 26 - 29, 2017

EUV RESIST PERFORMANCE

LOW DOSE IS ACHIEVED, BUT LIMITED BY STOCHASTICS

Feature	32nm pitch dense line-space / Vertical		32nm pitch dense line-space / Vertical		26nm pitch dense line-space / Horizontal		36nm pitch regular dense contacts	38nm pitch regular dense pillars
Resist type	CAR	NCAR	CAR	NCAR	CAR	NCAR	CAR	NCAR
SEM top-down image @ BE/BF								
Dose mJ/cm²	30.5	31.4	21	20.9	39	37.3	31	30
LWR/LCDU nm	4.7	4.6	5.4	5.2	4.5	4.2	3.5	3.9

Challenge #1: Stochastic Failures



imec

Source:

EUV DEVELOPMENTS AT IMEC

DANILO DE SIMONE, PETER DE BISSCHOP, IVAN POLLENTIER, WAIKIN LI, EMILY GALLAGHER, VICKY PHILIPSEN, VINCENT WIAUX, RYOUNG-HAN KIM, ERIC HENDRICKX, GEERT VANDENBERGHE, KURT RONSE, GREG MCINTYRE

ON BEHALF OF IMEC PATTERNING

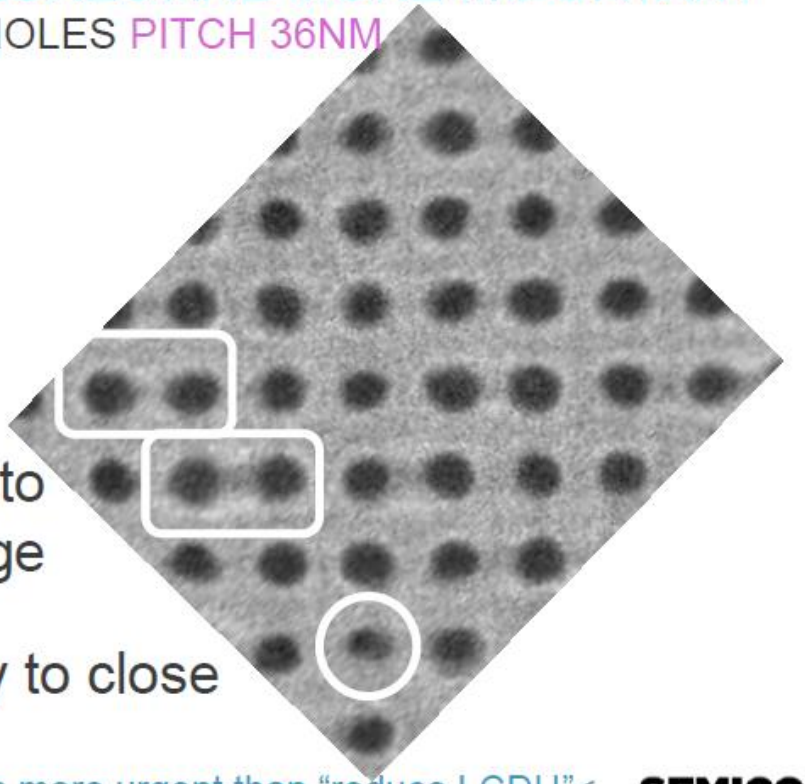
15 JUNE 2017, EUVL WORKSHOP, BERKELEY, CA

Features Patterned with NXE 3300 NA=0.33

Stochastic Nanofailures

BUT, (AGAIN) NANO FAILURES ARE MORE IMPORTANT

DENSE REGULAR CONTACT HOLES PITCH 36NM



CHs with tendency to merge

CH with tendency to close

>To get rid of nano failures is more urgent than "reduce LCDU"<

imec

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D. DE SIMONE

SEMICON EUROPA 14-17 NOV 2017 MUNICH GERMANY

Yan Borodovsky, "The Future isn't what is used to be", Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

Yield and Stochastic Failures
5nm Node

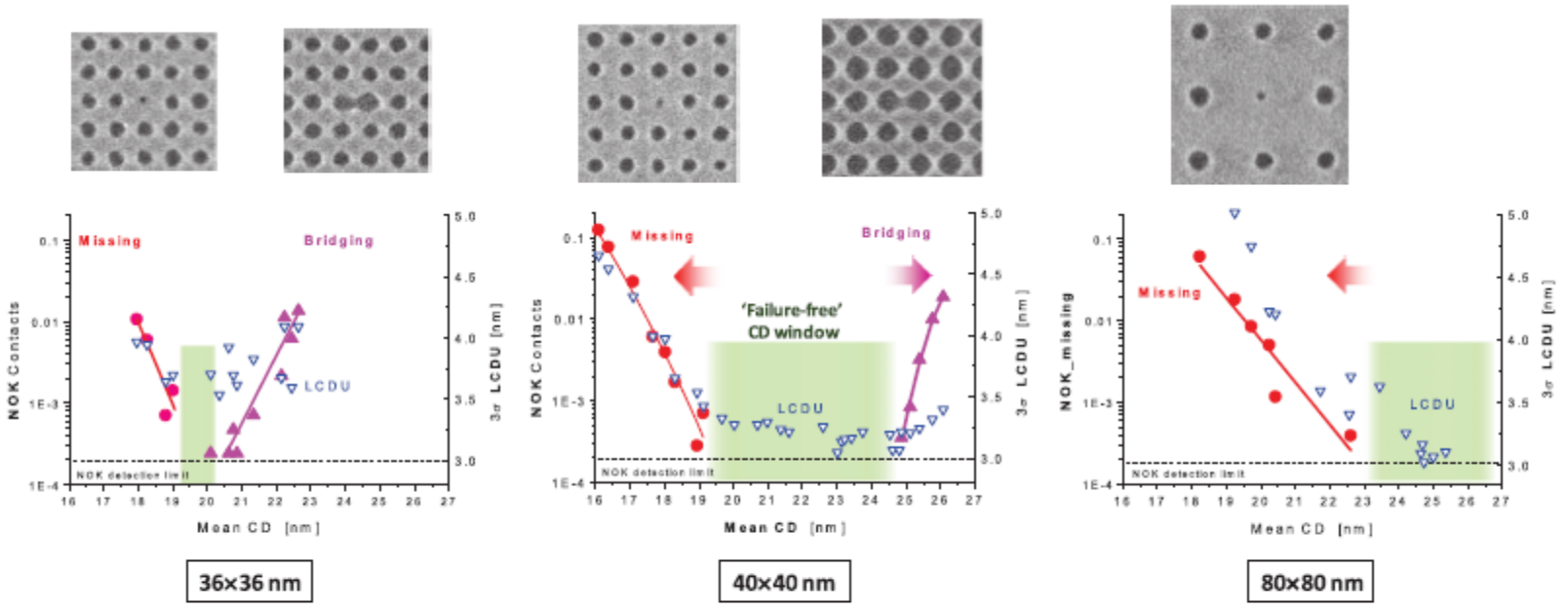

Fig. 5 Measured LCDU and NOK values for square contact arrays as a function of the measured mean contact CD (postlitho, PTD-CAR, resist thickness 30 nm, 25-deg opening angle Quasar™ illumination source, dose-meander wafer). The onset of printing failures defines "patterning cliffs." The target CD should be chosen in the failure free CD windows, i.e., in the CD-interval where failures are absent (shaded in green). Postlitho data.

Source: Peter De Bisschop, "Stochastic effects in EUV lithography: random, local CD variability, and printing failures," J. Micro/Nanolith. MEMS MOEMS 16(4), 041013 (2017), doi: 10.1117/1.JMM.16.4.041013.

Defectivity Intolerance of Von Neumann Computing will eventually result in end of viable area scaling.

Patterning Holy Grail

Moore's Law = Density+Cost Per Transistor

$CPT_{n+1/n} = Wafer\ Cost_{n+1/n} * AreaScale_{n+1/n}$

(Assuming equivalent yield)

	n+1/n	
Wafer Cost	Area Scale	CPT
1.1	0.55	0.6
1.2	0.50	0.6
1.3	0.46	0.6
1.4	0.43	0.6
1.5	0.40	0.6

5nm Node and below will be progressively defect prone due to impact of Stochastic effects in EUV Litho.

Defects ↑ = Yield ↓

~50% of Wafer Cost is Patterning now

$CPT_{n+1/n} = 2 * PatternCost_{n+1/n} * AreaScale_{n+1/n}$

Lowest PatterningCost*AreaScale solution is Litho Holy Grail.

intel

Y.Borodovsky, Alternative Lithographic Technologies VII, Conference 9423, 23 February 2015, San Jose, CA, USA

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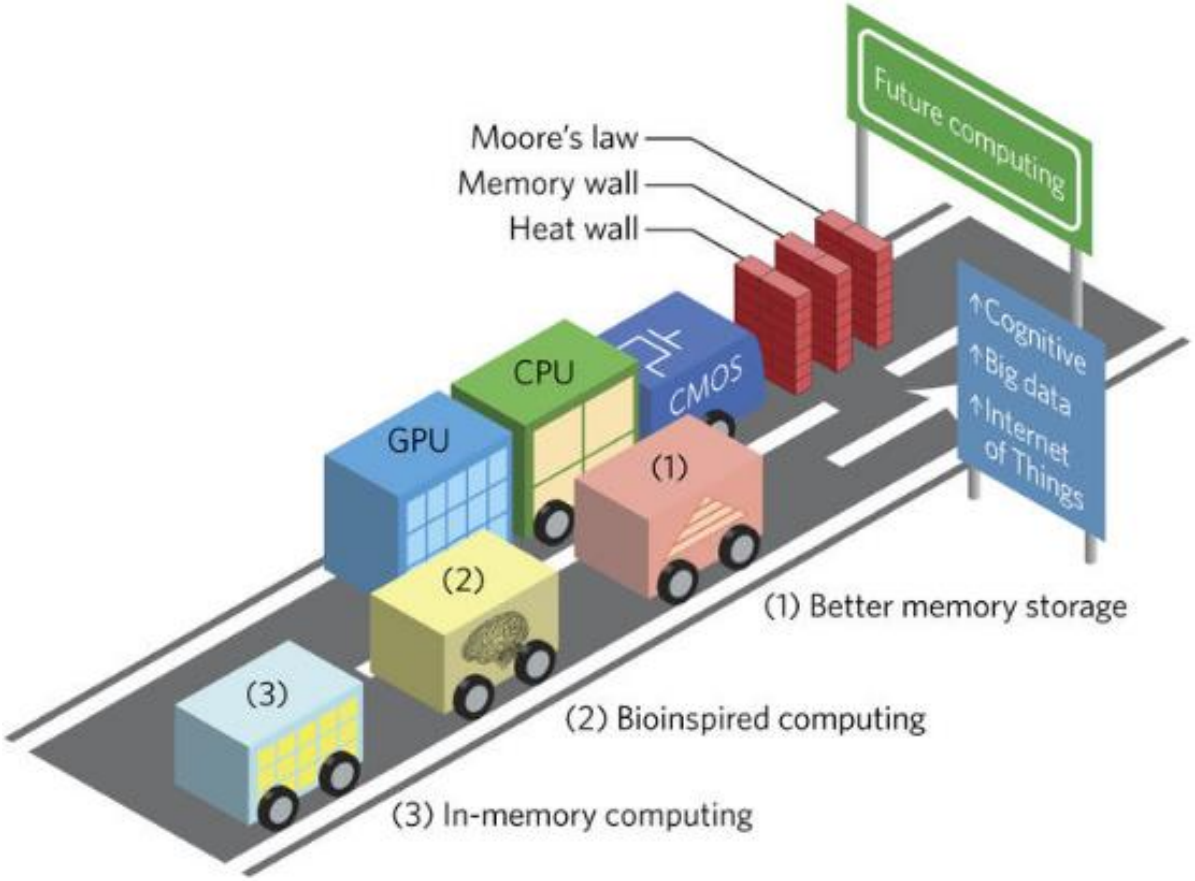
Yan Borodovsky, "The Future isn't what is used to be", Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

Bioinspired Computing will be a vehicle to get Through Defect Limiting Moore's Law Wall

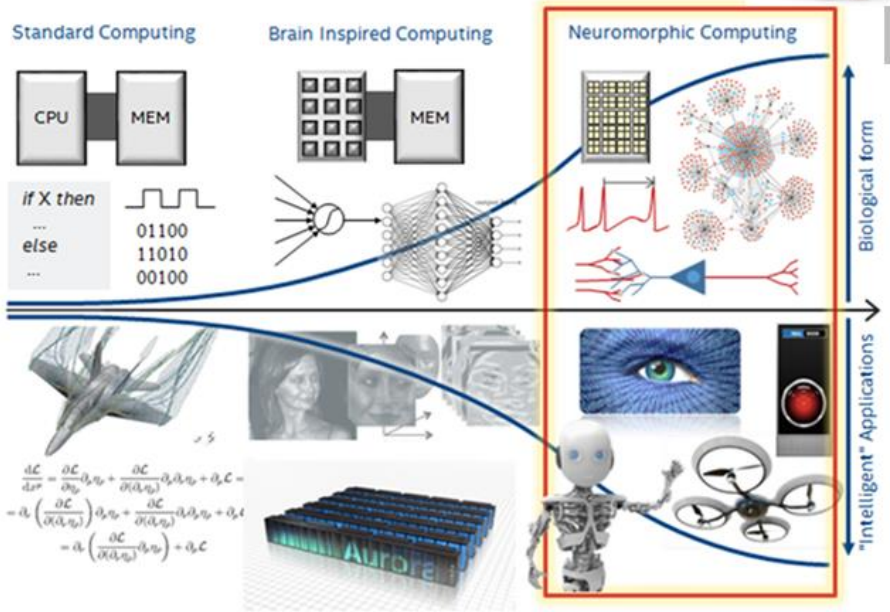


Source "The future of electronics based on memristive systems"
Mohammed A. Zidan, John Paul Strachan & Wei D. Lu
Nature Electronics **1**, 22–29 (2018),doi:10.1038/s41928-017-0006-8

Beyond von Neumann Computing – Opportunity for further scaling with 10^X defect density

Efficient & Scalable Neuromorphic Systems

Neuromorphic Circuit – circuit that in its structure mimics organization of the brain



Implementation Features

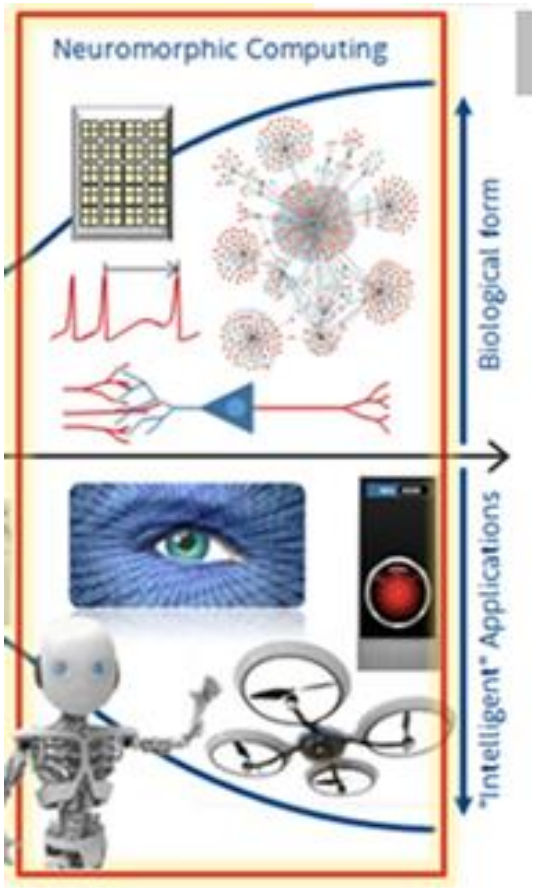
- Spatio-temporal encoding
- Distributed memory/compute
- Complex & efficient network
- Dynamic connectivity
- Asynchronous/event-driven
- Continuous learning
- Synaptic plasticity
- Homeostasis
- Stochasticity
- Recurrent
- Adaptive & resilient

Exploit integration, spike timing, sparsity, plasticity & resiliency

"Challenges and Opportunities for Efficient & Scalable Neuromorphic Systems", Vivek De, Intel, DAC54, 6/18-22/2017. Austin, TX USA

Yan Borodovsky, "The Future isn't what is used to be", Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

Bioinspired Computing might be a vehicle to get Through Defect Limiting Moore's Law Wall



Neuromorphic Circuit mimic in its structure organization of the brain

Figures 1 illustrate the quantitative data for the neuromorphic model of AND, NAND, OR, NOR, XOR and XNOR gates. The graph shows the relationship between R_p and probability (assurance) of reaching the correct solution, which is the supposed output of logic functions f. The stochastic perturbations ξ are modeled as uniformly distributed discrete random noise. For $R_p \in [0\ 0.4]$, the correct output f for AND, NAND, NOR and OR gates is achieved within ~100% requiring 400 iterations. In contrast, gates XOR and XNOR achieve the correct f from 80% to 100% requiring ~450 iterations. As R_p increases, the required number of iterations to achieve stability increases. Figure 1.b illustrates the number of iterations for the network to evolve to a stable state for different R_p.

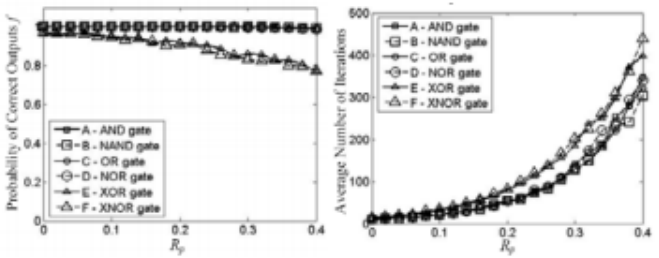


Figure 1. Fault-tolerance of the neuromorphic model of elementary logic gates in the presence of disturbances for $R_p \in [0\ 0.4]$ (5000 runs)

The superposition of inherent noise, interference and other disturbances are considered as stochastic perturbations $\boldsymbol{\xi}$. We use the perturbed-to-unperturbed ratio R_p which characterizes the *strength* of the $\boldsymbol{\xi}$. In general, $\boldsymbol{\xi}$ is a mapping of all ξ_i which are hardware-dependent. Continuous and discrete distributions of random ξ_i result in probability functions $\gamma(\xi_i)$ as well as distribution functions. Normal, binomial, hypergeometric, Poisson and other distributions affect $\boldsymbol{\xi}$.

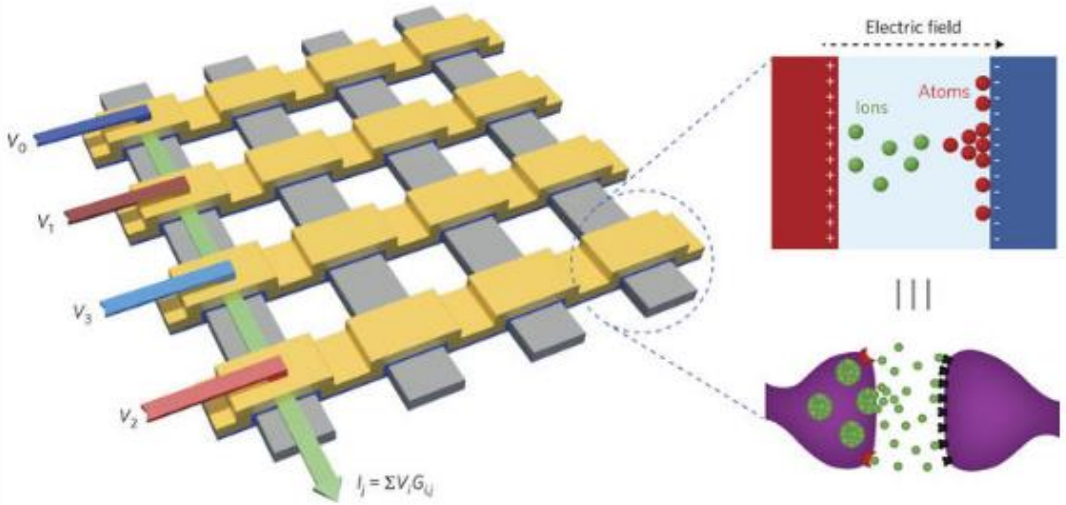
We simplify the analysis by using $R_p \in [0\ 1]$.

For an ideal unperturbed model R_p=0, while for a completely faulty cell, R_p=1.

Neuromorphic Logic Networks and Robust Stochastic Computing Under Large Perturbations and Uncertainties

RRAMs, Spin-Torque and other technologies are actively pursued as neuromorphic computing fundamental building blocks

Hardware implementation of artificial neural networks in a memristor crossbar.



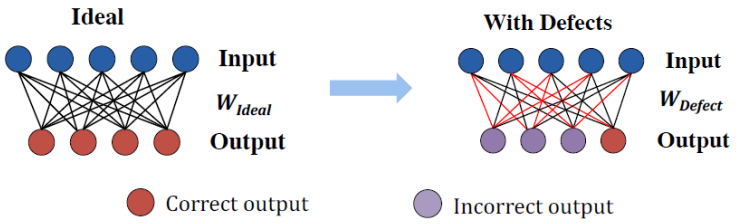
A memristor is formed at each crosspoint and can be used to simultaneously store data and process information. In this approach, vector-matrix multiplication can be obtained through Ohm's law and Kirchhoff's law through a simple read operation. In addition, the internal dynamics of memristors can be utilized to faithfully emulate underlying processes in biological synapses. V_i, voltage applied at row i; I_j, current through column j; $G_{i,j}$, conductance of the memristor at the intersection of row i and column j.

The future of electronics based on memristive systems"
Mohammed A. Zidan, John Paul Strachan & Wei D. Lu
Nature Electronics **1**, 22–29 (2018),doi:10.1038/s41928-017-0006-8

Neuromorphic computing as enabler to break through next Moore's Law Wall

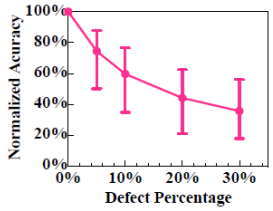
Impact of Memristor Defects

- An illustration of the defects on neural network



- Impact of the defects
  - Two-layer network for MNIST recognition
  - Large accuracy degradation:

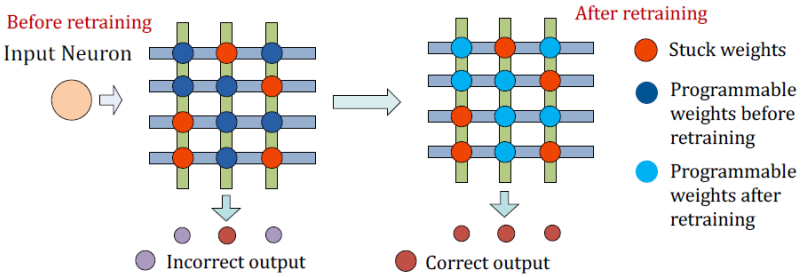
    59.7% at 10% defects, 44.2% at 20% defects



6

Rescue: The Network Retraining

- Tune the network for the self rescue



- Two major considerations in the retraining
  - Weight initialization:

    Pre-training → W_{Ideal} → Inject defects information → W_{Defect}
  - Weight updating:

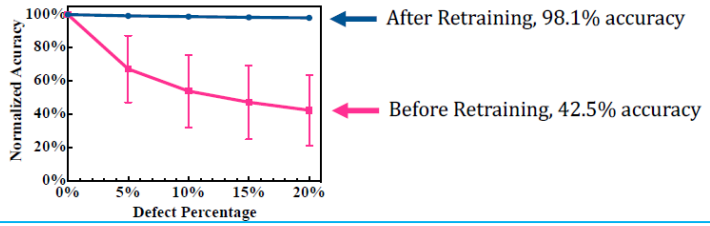
    $\Delta w_{ij}\,(defect) = 0$

    The amount of weight that each synapse needs to be updated in backpropagation

8

Evaluations: Robustness of the Retraining

- Feed-forward neural networks for MNIST recognition
  - Recognition accuracy before and after retraining



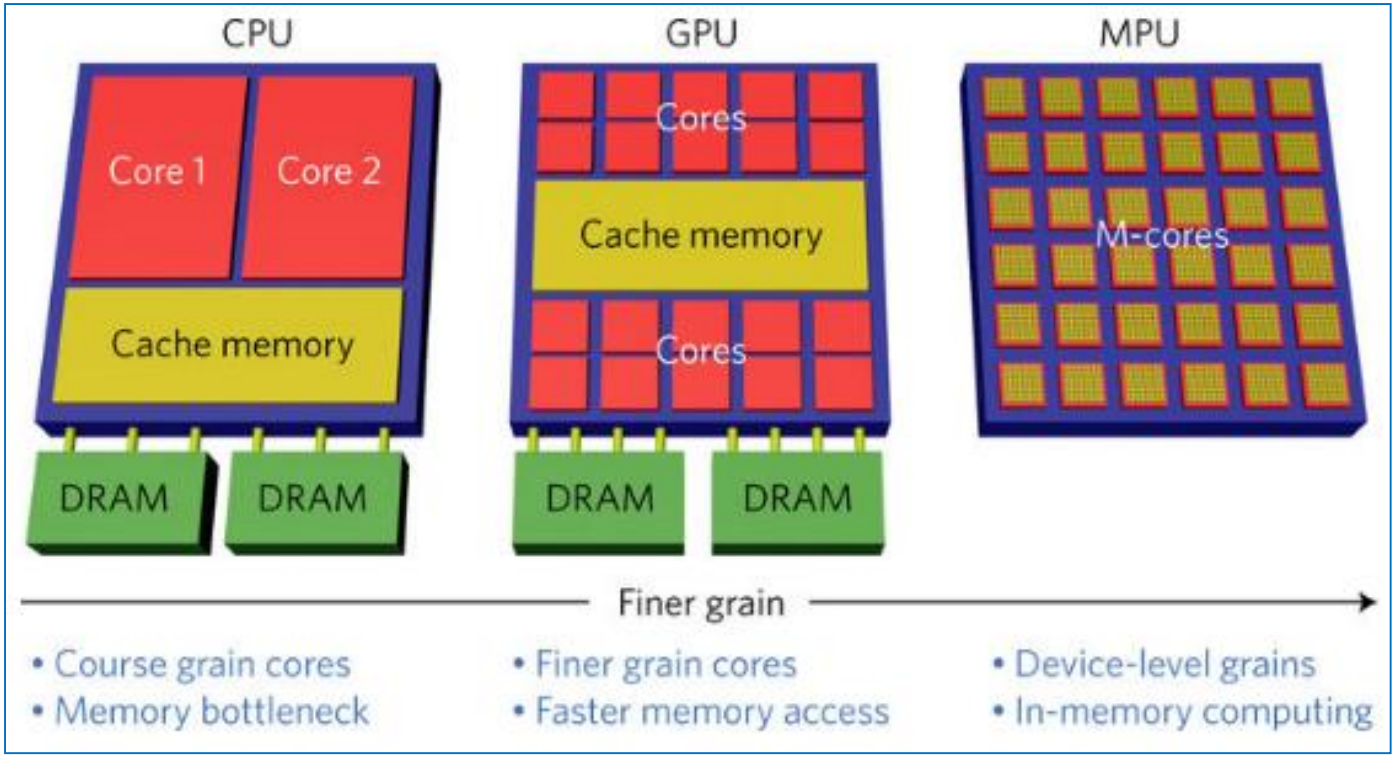
Source: Prof. Chenchen Liu Presentation at DAC 17

"Rescuing Memristor-based Neuromorphic Design with High Defects"

Chenchen Liu, * Miao Hu, * John Paul Strachan and † Hai (Helen) Li; Clarkson University*Hewlett-Packard Labs †Duke University

Full Paper: DAC '17, June 18-22, 2017, Austin, TX, USA
c 2017 ACM. ISBN 978-1-4503-4927-7/17/06. . . $15.00
DOI: http://dx.doi.org/10.1145/3061639.3062310

Proposed MPU Architecture



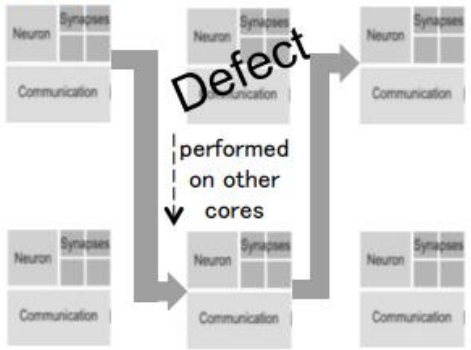
Source: "The future of electronics based on memristive systems"
Mohammed A. Zidan, John Paul Strachan & Wei D. Lu
Nature Electronics **1**, 22–29 (2018),doi:10.1038/s41928-017-0006-8

Proposed MPU Architecture shall support defect prone IC scaling

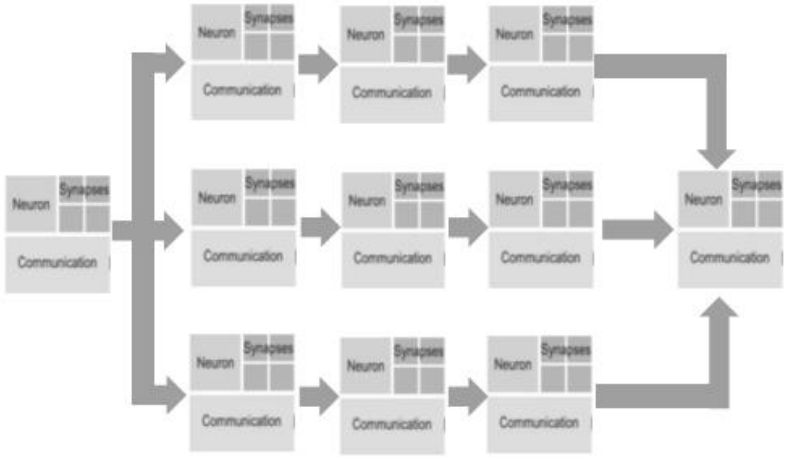
IBM

High defect tolerance And reliability

- Defect tolerance – Treatment at the defective core is performed on other cores



- Reliability – The majority voting system can be configured by programming



From [11] "Neuromophic device for Automotive" by Yoshifumi Sakamoto, Engineering and Cognitive Innovation, IBM Japan, LTD, email: sakay@jp.ibm.com

Putting it all in Perspective

Von Neumann Computing will eventually hit scaling wall as defectivity required to support it will reach < 10^{-14}/die features for overall 10^{-2}/cm2 defects per wafer/per print.

Neuromorphic Computing can tolerate up to $4*10^{-1}$ defects per network.

Multiple technologies that were under development and commercialization efforts for >10 years but were not adopted for Logic will become viable alternatives to EUV to drive parts density and cost as per Moore's Law

NanoImprint for Logic

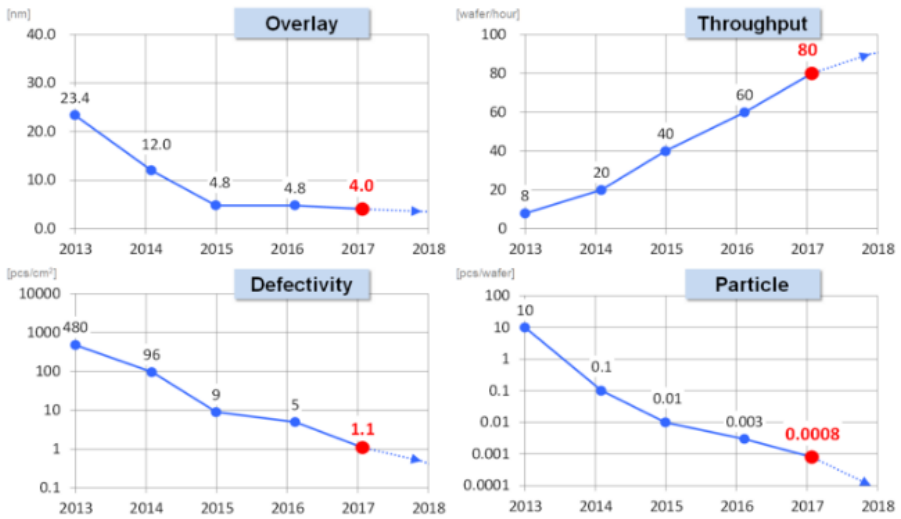


Figure 1. Historical overview of defectivity, particle generation, overlay and throughput, starting in 2013.

From "**A review of nanoimprint lithography for high-volume semiconductor device manufacturing" by Douglas J. Resnick/Jin Choi,**
Advanced Optical Technologies, Volume 6, Issue 3-4, 2017

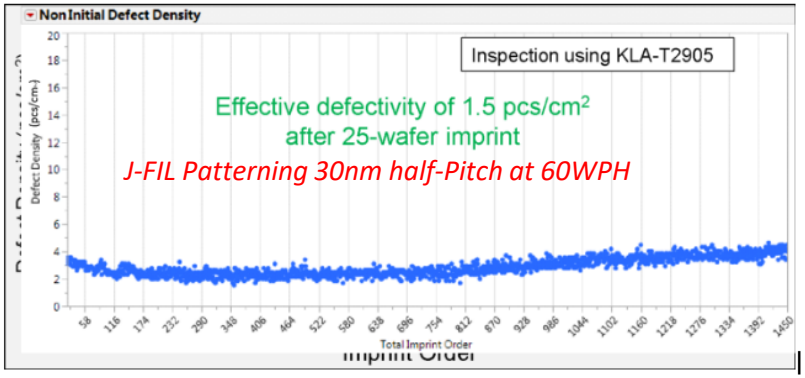


Figure 10. Defect density across a 25 wafer run. Overall defectivity increased by 1.5 defects/cm².

NIL – OK to support Neuromorphic parts manufacturing now?

How will it scale during next 10 years?

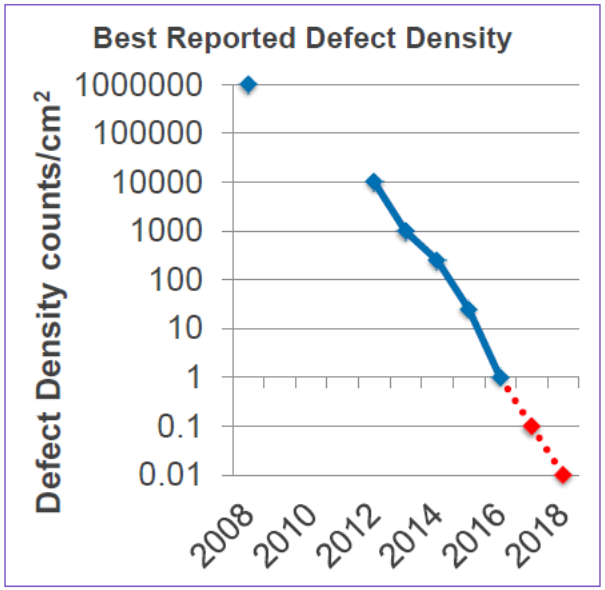
DSA Defectivity – OK to support Neuromorphic Products now?

DSA Defectivity

Source:"**DSA: How far have we come and how much further is left to go?" Darron Jurajda ,** Brewer Science, 2016

Defectivity Industry Milestones

- 2008 – 0.01% or 10^6 cm^{-2}
- 2012 – >10,000 cm^{-2}
- 2013 – Process monitor data first reported, 979 cm^{-2}
- 2014 – ~200 cm^{-2} (LiNe flow), 270 cm^{-2} (LETI contacts)
- 2015 – 24 cm^{-2} (LiNe flow golden performance)
- 2016 – ~0 cm^{-2} (LETI, hole open yield, 0.01 mm^2 inspection area)
- Two more orders of magnitude needed to hit industry target of 0.01 defects cm^{-2}



SEMICON TAIWAN

Tada, et. al., Macromolecules, 41, 9267-9276, (2008)
Benchera, et. al, SPIE 2012
Caoa, et. al, SPIE 2013

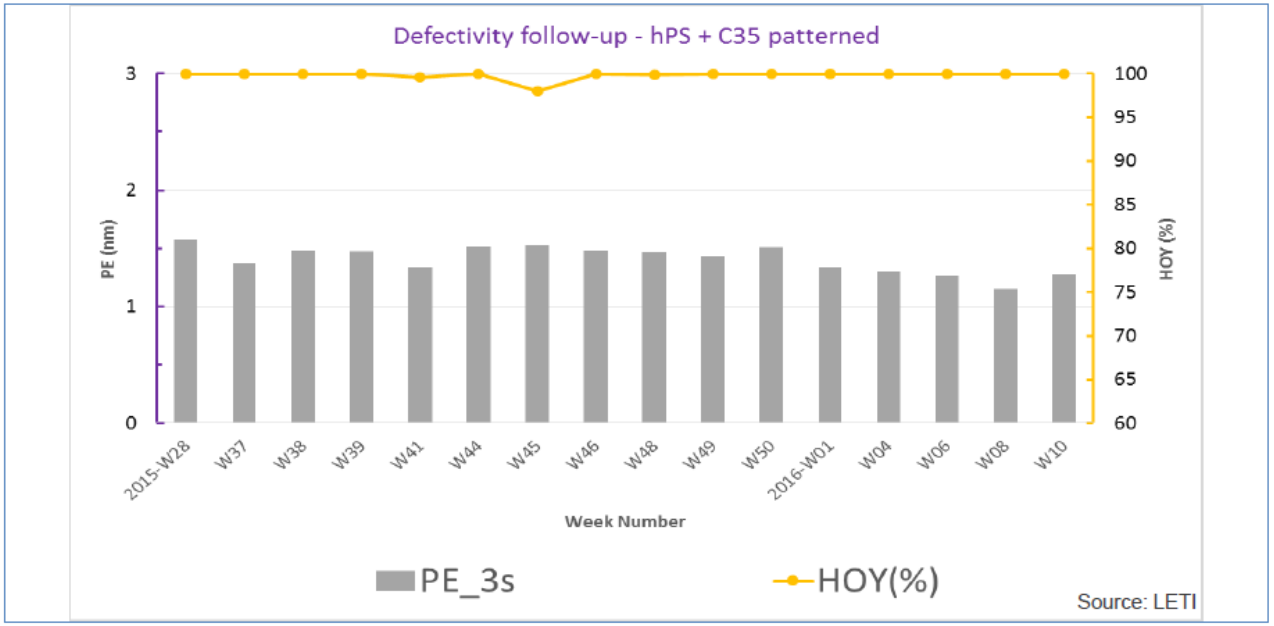
Gronheid, et. al, SPIE 2014
Argoud , et. al, SPIE 2014
Pathangi, , et. al, SPIE 2015

semi

Yan Borodovsky, "The Future isn't what is used to be", Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

DSA Defectivity– OK to support Neuromorphic Products now?

DSA Pattern Placement and Hole Open Yield

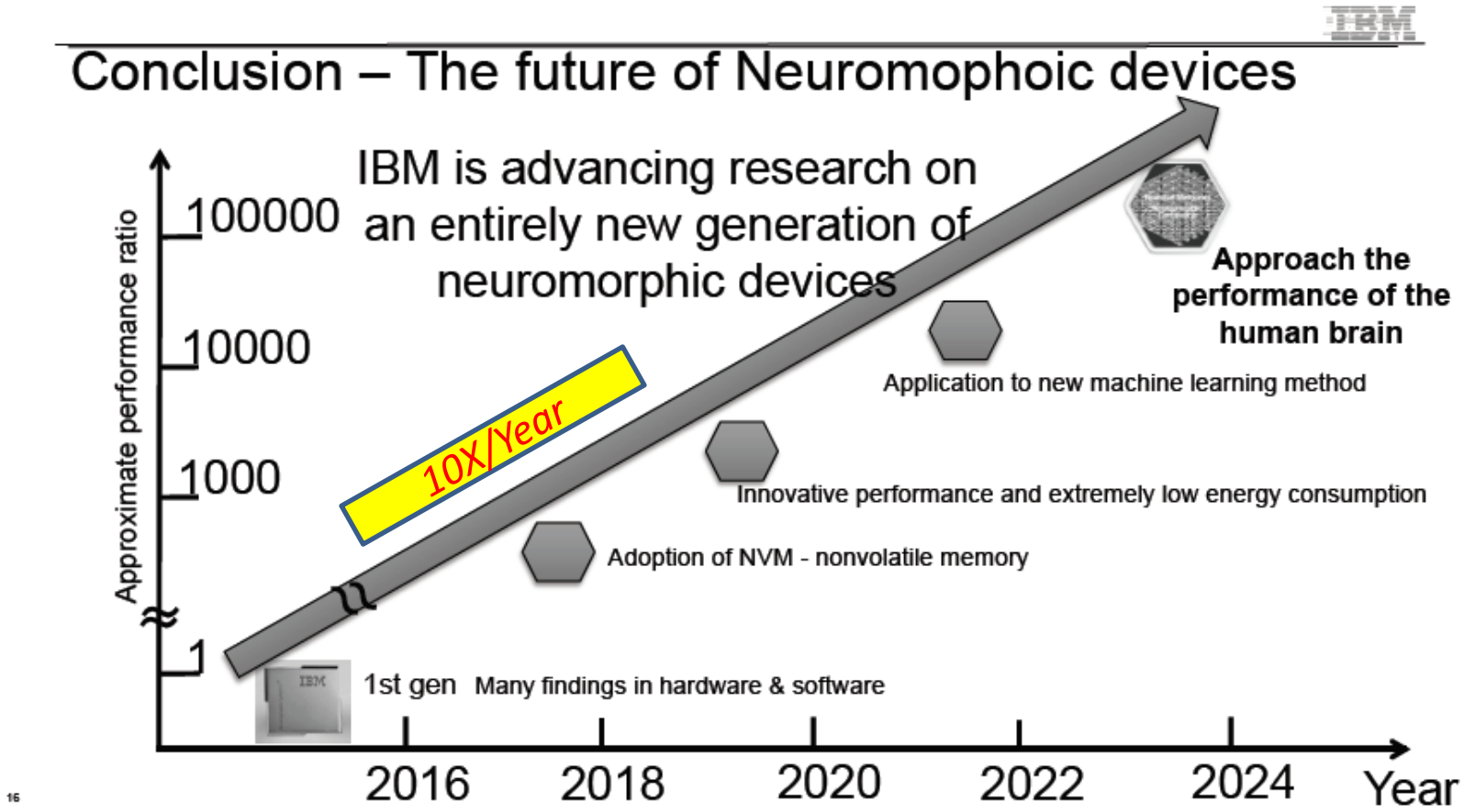


Consistent placement error (PE) and hole open yield (HOY) week to week

Source:"**DSA: How far have we come and how much further is left to go?" Darron Jurajda ,** Brewer Science, 2016

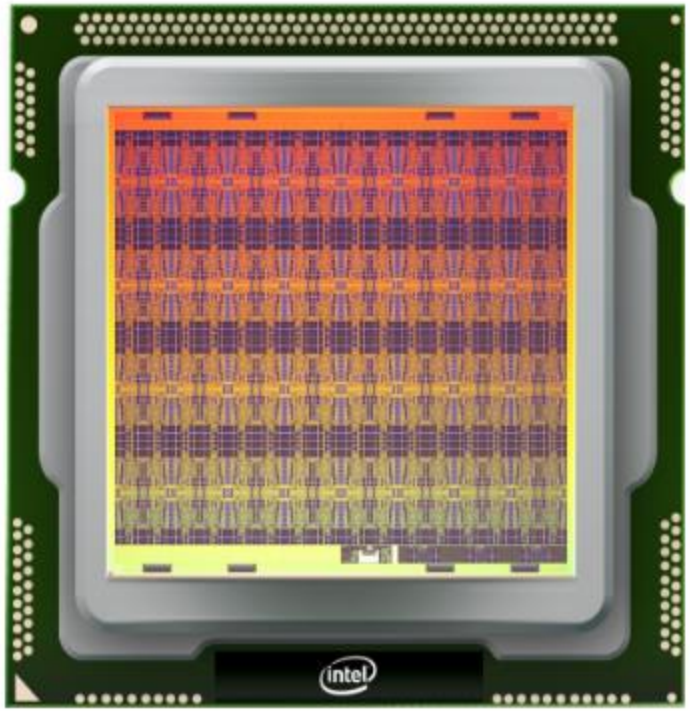
Yan Borodovsky, "The Future isn't what is used to be", Leti Alternative Lithography Workshop, March 1, 2018, San Jose, CA, USA

2024 - WOW!



From "Neuromophic device for Automotive" by Yoshifumi Sakamoto, Engineering and Cognitive Innovation, IBM Japan, LTD, email: sakay@jp.ibm.com

Defects – If you cannot beat them – Join them

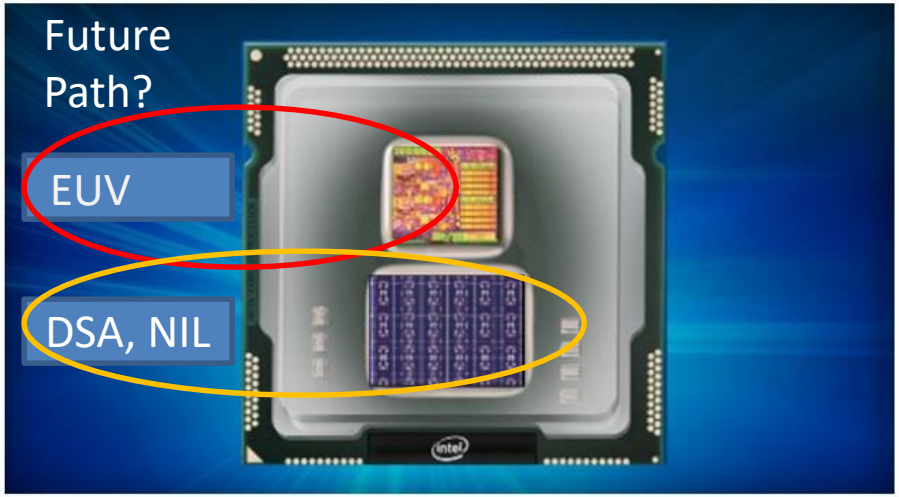


Loihi simulates a total of 130,000 neurons and 130 million synapses, all capable of communicating with each other… comparable to some small insects. For example, a common fruit fly, an insect studied for AI research, has about 250,000 neurons and 10 million synapses. …human brain - 100 billion neurons,

Intel Unveils Neuromorphic, Self-Learning Chip Codenamed Loihi

By Joel Hruska on September 27, 2017 at 9:18 am | 14 Comments

1.1K shares



https://www.extremetech.com/computing/256467-intel-unveils-new-neuromorphic-self-learning-chip-codenamed-loihi

CPU – Defect Intolerant – Traditional Litho
NMU- Defect Tolerant – Minimal Cost Litho

Defects: If you cannot beat them – join them

Von Neumann Computing will eventually hit scaling wall as defectivity requirements will reach < 10^{-14}/chip features for overall 0.01/cm^2 defects/layer on a wafer.
Neuromorphic Computing can tolerate up to $4*10^{-1}$ defects per network.
Neuromorphic Computing defect tolerance will enable continuation of Moore's Law by augmenting Von Neumann Control parts on the same 2 chip part.

Neuromorphic Computing is expected to be Artificial Intelligence workhorse.

IDC forecasts Global Revenue for Cognitive and AI Systems going from $18B in 2017 to $46B in 2020 and Global Cognitive and AI Systems Spending annual growth rate (CAGR) of 54.4% through 2020 . *Word of caution: AI is at the top of Gartner Hype Cycle now.*

Collaboration between Technologists and Computer Architects is needed to create compelling computing products that take advantage of defect tolerant manufacturing.

Directed Self Assembly and NanoImprint Lithography are in a good position to support Neuromorphic Computing parts patterning to provide necessary means to enable Moore's Law beyond capabilities of conventional Lithography

Thank you for
your attention!

Time for
Questions

Presentation Format

- Most of the information to be presented are from my previous public talks approved by my former employer, Intel, for external presentation and publications. Those foils will be copied “as is” and will have Intel logo, colored background and information on where and when those were presented.
- Foils made for this presentation will be on simple white background and will have no Intel logo.
- Multiple foils will be using materials presented or published by others during 2015-2018 and will have its source shown on the foil. My additions to those, if any, will be in italic red.